Proposal for Transmitter Timing Jitter Specification

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Overview

- Purpose
- Objectives
- Proposed Jitter Specification
- Conclusion

Purpose

- Specify Maximum Allowable Jitter Introduced by Slave in Loop-Timed Mode
  - Loop timing introduces jitter that can affect interoperability
  - Transmitter linearity specifications do not account for loop timing jitter

Objectives

- Make Accurate (< ±1 ps) Measurement of Jitter at the Slave MDI Output
  - Accurate jitter measurement requires direct measurement at MDI output
  - Test clock jitter may differ from the MDI output jitter by many picoseconds
  - Accurate jitter measurement requires use of precision analog laboratory equipment, such as spectrum analyzers

Objectives

- Operate Slave in Loop-Timed Mode
  - Requires that Slave be connected to Master
  - Choice of test cable unimportant since 10G PHYs are relatively insensitive to linear distortion
    - Poor impedance matching not required
  - Master transmits waveform suitable for Slave loop timing function (PRBS training pattern)
  - Slave transmits waveform suitable for accurate jitter measurement (narrowband signal)

Objectives

- Isolate Slave Test Output from Master Synchronization Waveform
  - High isolation (> 60 dB SNR) required for accurate jitter measurement (< ±1 ps)
  - Attenuating Master output signal provides up to 15 dB of isolation
  - Balance of required isolation obtained through pair-to-pair isolation (> 30 dB) and frequency selective filtering (~ 20 dB for 2 MHz filter)
  - Passive isolation elements introduce negligible distortion and noise

Objectives

- Make Jitter Specification Consistent with SNDR Required for Interoperability
  - The following SNDR requirement has been proposed

$$\mathrm{SNDR} \geq \min\left\{48, 58 - 20 \cdot \log\left(f_{\mathrm{MHz}} / 25\right)\right\}$$

  - SNDR requirement of 40 dB at 200 MHz corresponds to 8 ps RMS equivalent jitter at 200 MHz
  - Allocate portion of 8 ps RMS equivalent jitter to clock jitter (50%), remainder to other sources of noise and distortion (50%)

Proposed Jitter Specification

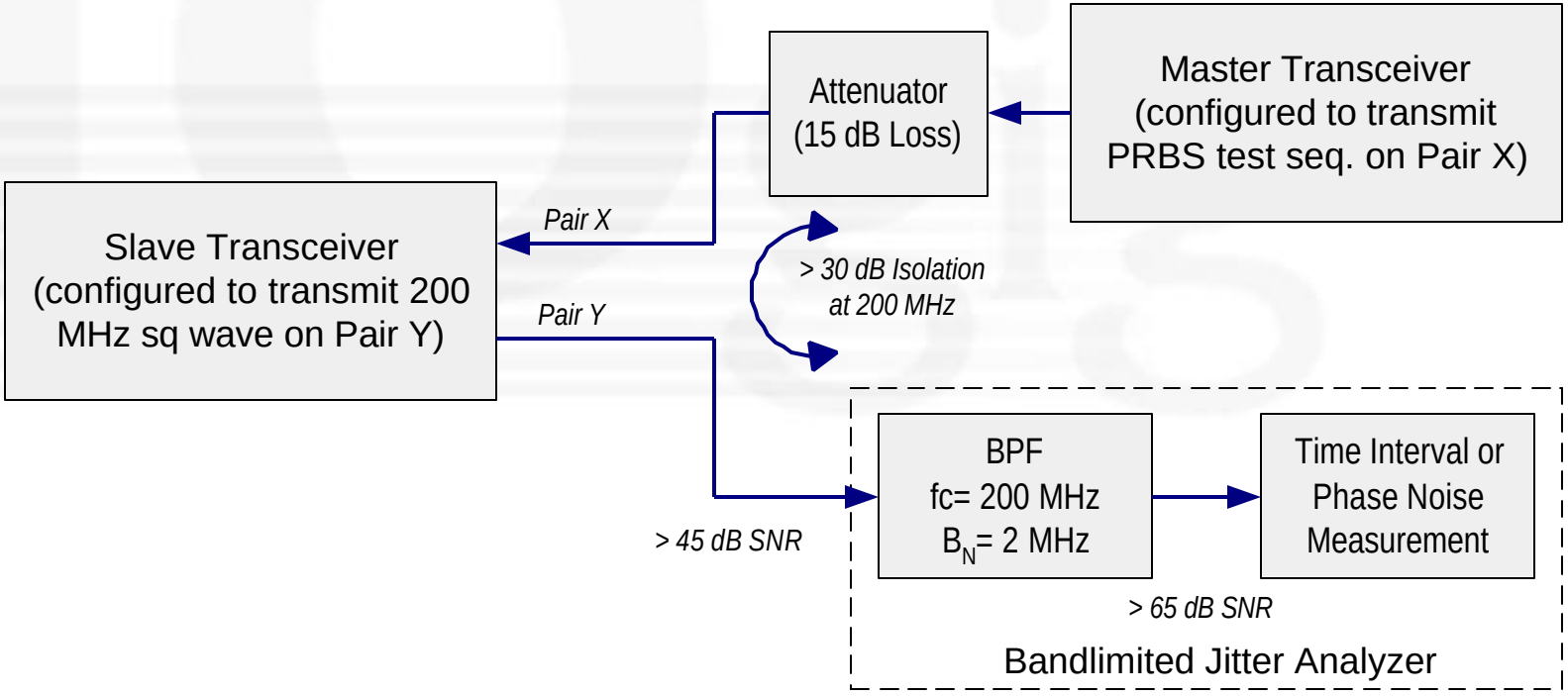
55.5.6 Transmitter Timing Jitter

When in Test Mode x, the Master PHY shall transmit the PMA training pattern (PRBS 33) to the Slave PHY on one channel (pair X) and the Slave PHY shall transmit a full-power, 200 MHz square wave to the Master PHY on a different channel (pair Y). In Test Mode x, the Slave PHY shall operate in the loop-timed mode, synchronizing its transmit clock on pair Y to the signal received from the Master PHY on pair X.

When in Test Mode x, with the Master PHY connected to the Slave PHY per the text configuration shown in Figure 55-x, the absolute (i.e., accumulated) jitter measured at the Slave PHY MDI output shall be less than 5.5 ps RMS. The absolute jitter shall be measured over an integration time interval of 1 msec ±10%.

- Note: 5.5 ps RMS jitter allocated to clock jitter, remaining 5.8 ps RMS jitter allocated to noise and other distortion (8 ps RMS equivalent jitter required for interoperability)

Proposed Jitter Specification



- Note: Circuit as shown provides sufficient Master/Slave isolation to ensure << 1 ps RMS measurement error (> 65 dB measurement SNR)

Specification Summary

- Slave Synchronizes Transmit Clock of Test Channel/Pair to Signal Received on a Different Channel/Pair
  - Non-standard mode of operation
  - Necessary to ensure sufficient isolation for accurate jitter measurement
  - Alternatives have significant disadvantages:
    - Much narrower jitter measurement bandwidth (600 kHz vs. 2 MHz), or
    - Narrowband Master output waveform (sine wave)

Conclusion

- Proposed Transmitter Timing Jitter Specification Meets Outlined Objectives for:
  - Compatibility with Interoperability Requirements.
  - Measurement Accuracy (< ±1 ps), and
  - Operation of Slave in Loop-Timed Mode
- Proposed Transmitter Timing Jitter Specification Splits 8 ps RMS Equivalent Jitter Budget Between Clock Jitter (5.5 ps RMS) and Other Noise and Distortion (5.8 ps RMS)