
**10GBASE-T
Transmitter SNDR
Definition
(System ID Approach)**

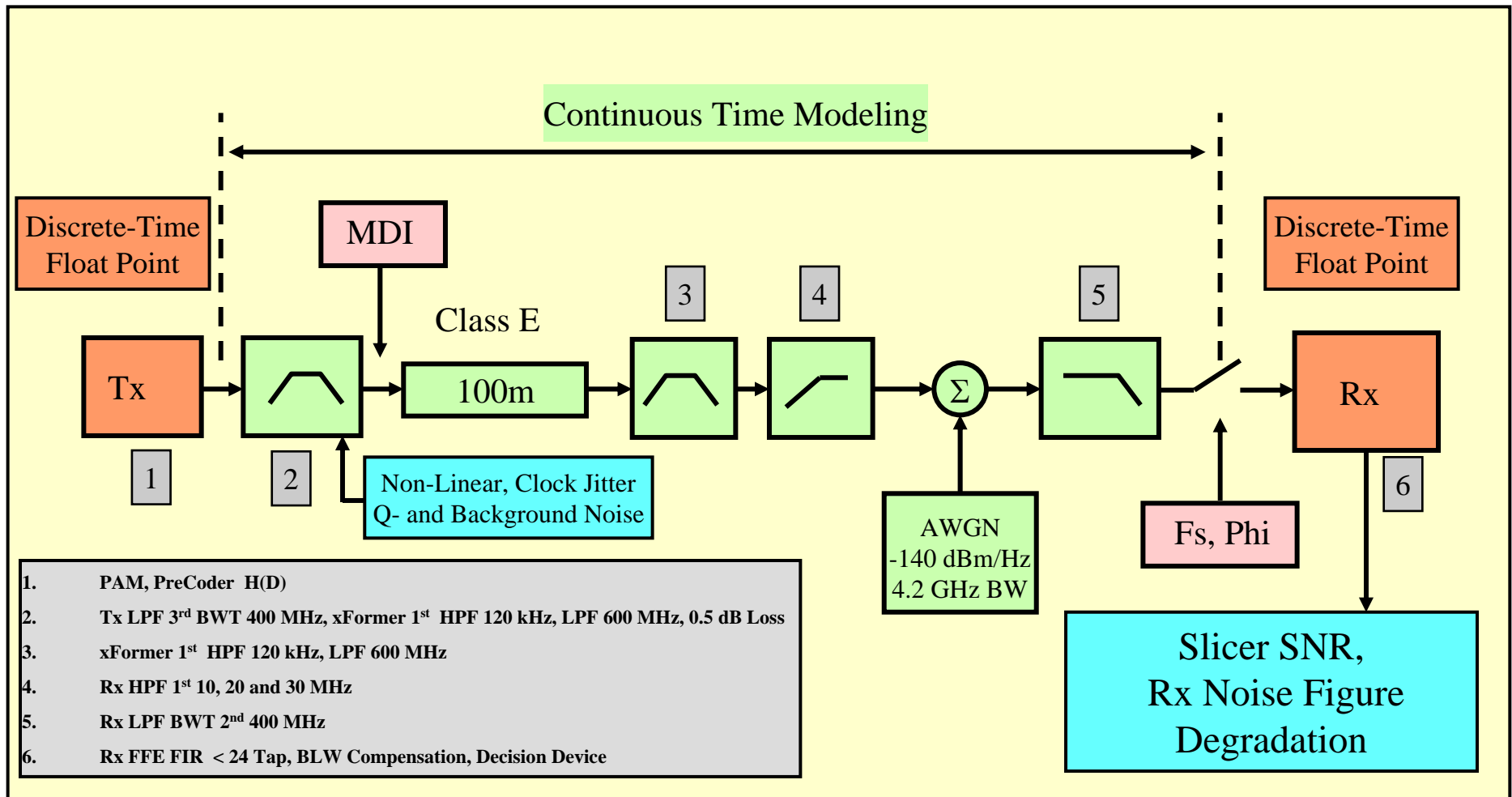
**IEEE P802.3an Task Force
Santa Clara, Feb 2005**

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OUTLINE

- **Transmitter Performance Evaluation Block Diagram and Example Tx Impairment Walk-through**
 - **System ID Methodology: Transmitter Characterization Metric Definition**
 - **10GBASE-T Transmitter Compliance Specification at MDI: Estimated Signal-to-Total-Noise and Distortion Ratio (SNDR) in a given Bandwidth**
 - **Conclusion**
-

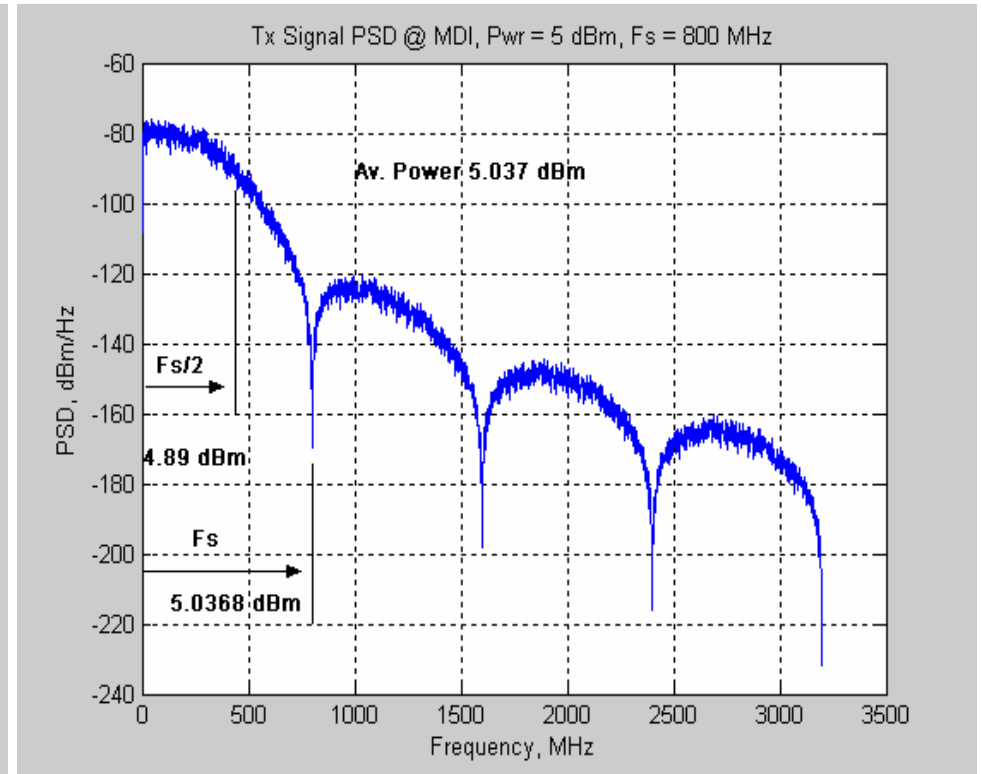
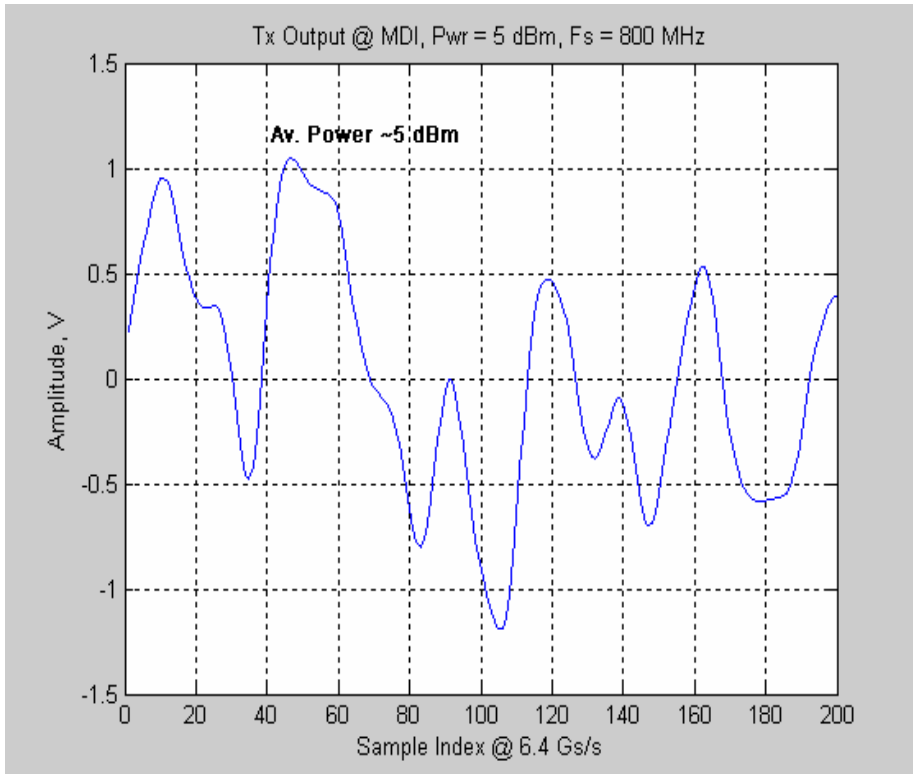
Transmitter Performance Evaluation Block Diagram



Tx Chain Key Impairments – Analog and Digital

- **Non-Linear Distortion (Active and Passive: xFormer, ...)**
- **Quantization and Background Noise**
- **Noise due Tx Clock Jitter**
- **Slew Rate Limitations Related**
- **Imperfect DSP**
- **Spurious – Clock Leakage, Supply, Parasitic Coupling, etc...**
- **Need a Compact and Meaningful Metric to Account for the Net System Impact**

Transmitter Noise-Like Broadband Output: Need Specialized Characterization Methodology



Tx Ideal Output at MDI – Noise-Like Time Domain Waveform

Tx Ideal Output at MDI – Frequency Domain PSD

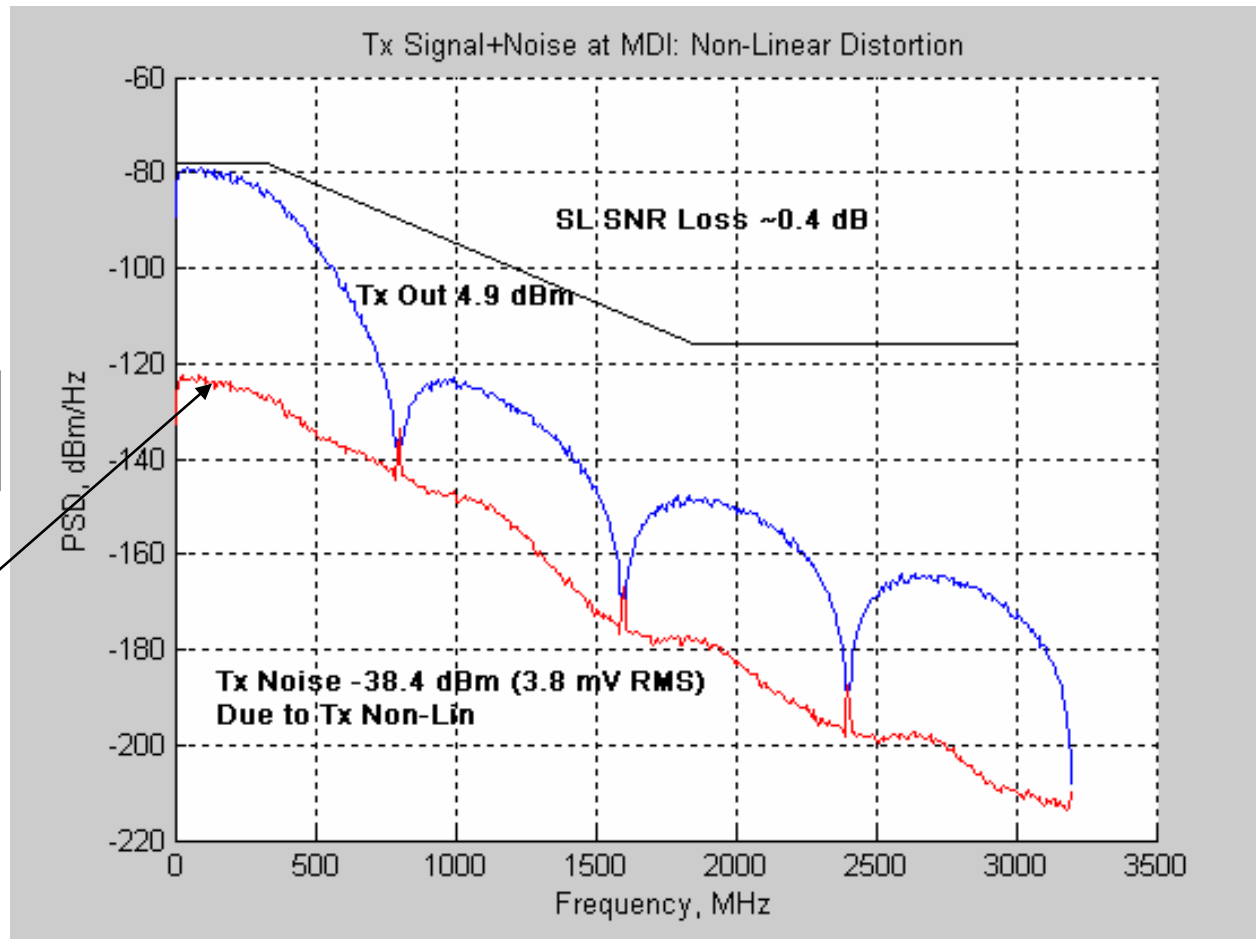
Signal Power →

$$pwr = \int_0^f psd(f)df$$

Note – Signal Power Converges fast with f

Tx Impairments – Non-Linear Distortion

Frequency Domain



Single-Tone
Dist. Yields
49-50 dB

Act. Tx SNR 43.3 dB
SL SNR Loss ~0.4 dB

-122 dBm/Hz max
Low-Pass type

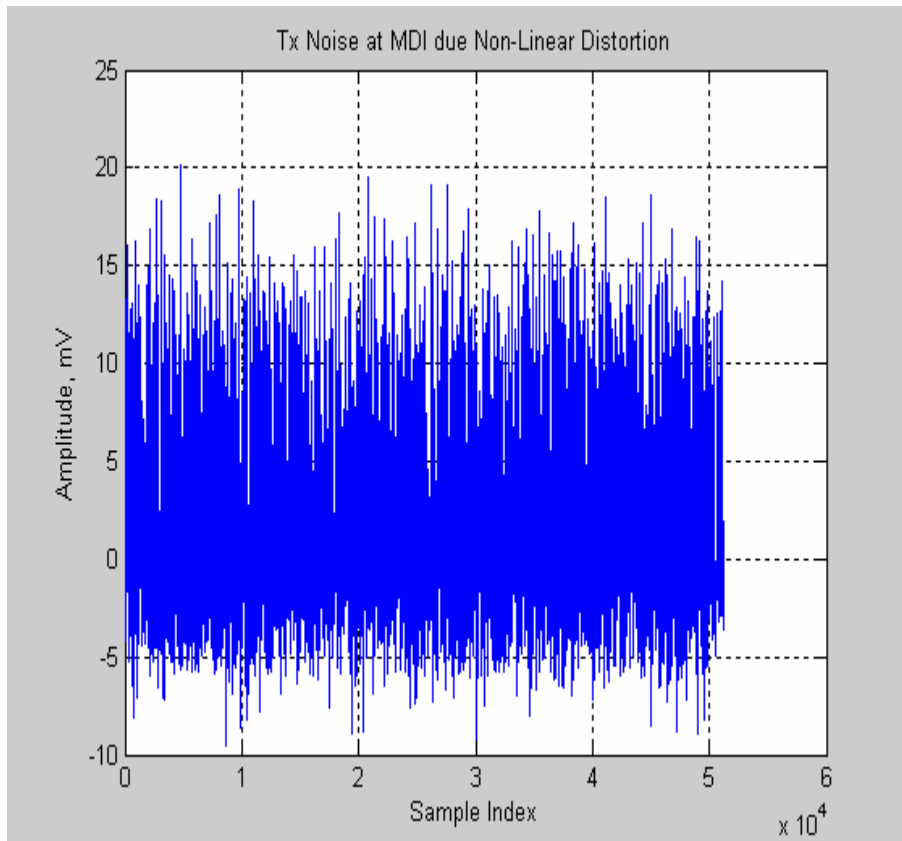
Asymmetrical
Compression

$a_1 = 1.0$
 $a_2 = 0.005$
 $a_3 = -0.007$

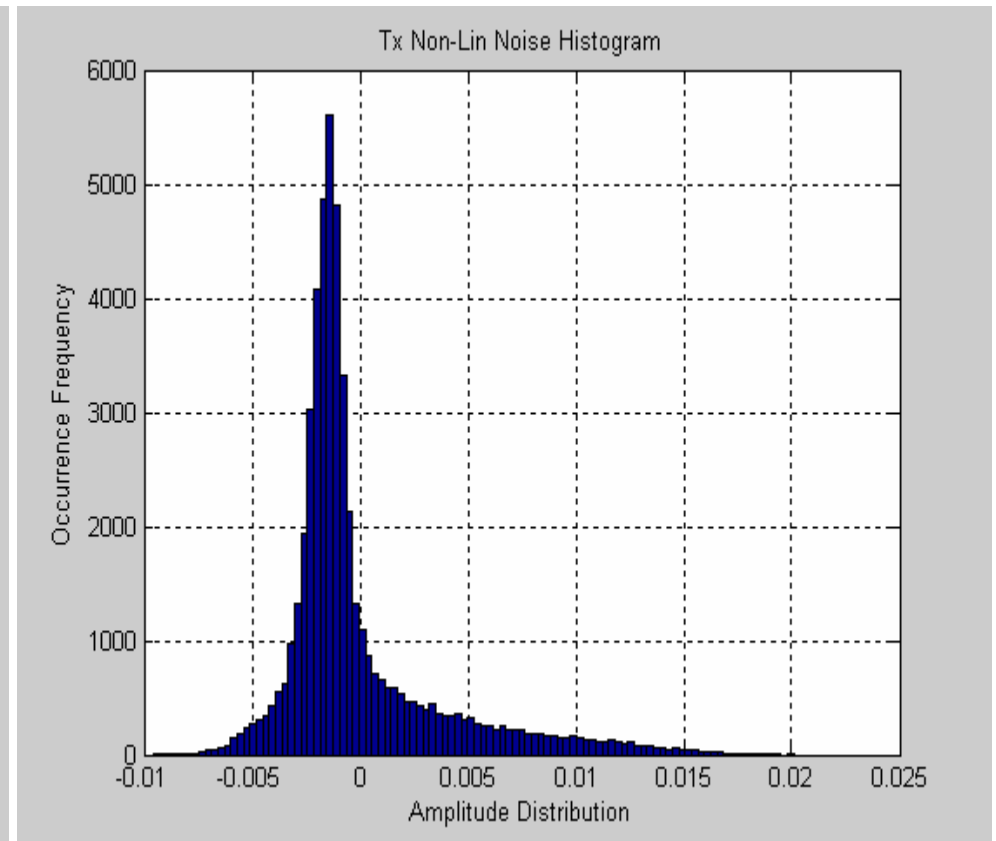
$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) \quad |v_o| < 1.25 \text{ V}$$

Tx Impairments – Non-Linear Distortion

Time Domain



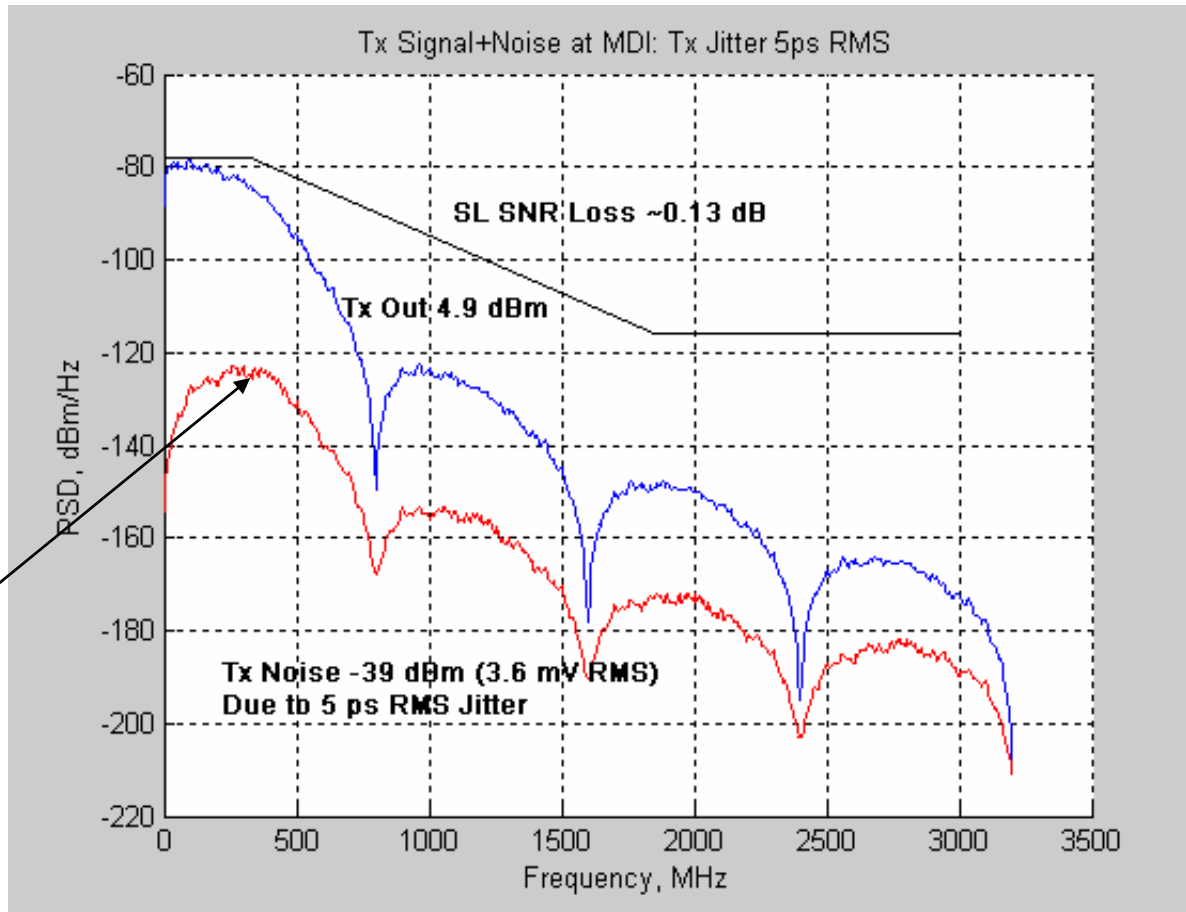
Non-Linear Distortion Noise due to Asymmetrical Compression in Tx Chain



Skewed Non-Gaussian Distribution

Tx Impairments – Fast Tx Clock Jitter

Frequency Domain



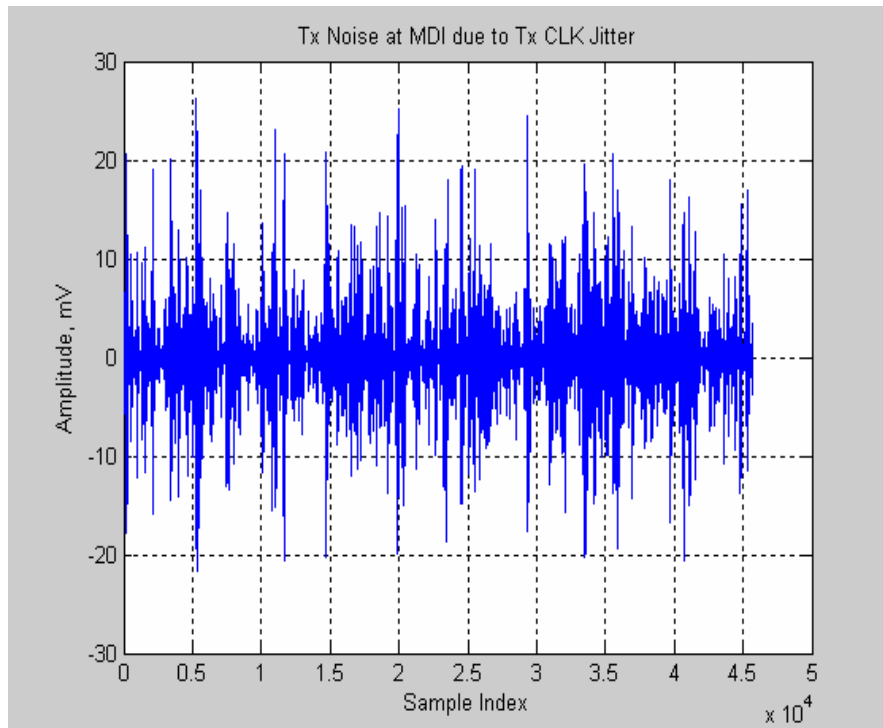
Tx CLK
Jitter ~5 ps rms
BW 1-10 MHz

-121 dBm/Hz max
High-Pass type

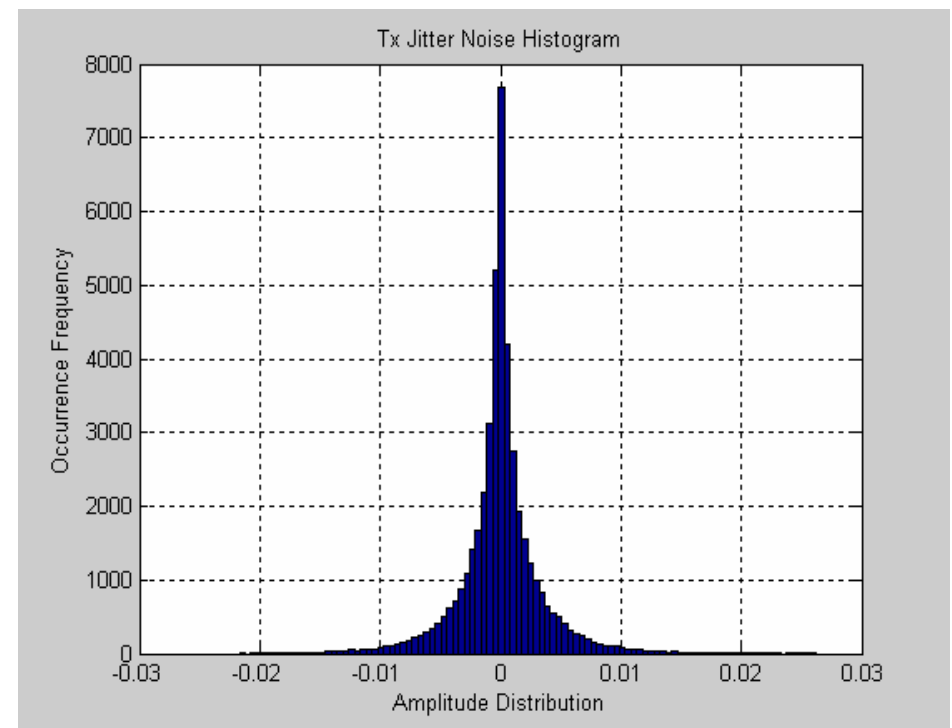
Tx SNR 44 dB
SL SNR Loss 0.13 dB

Tx Impairments – Noise due to Fast Tx Clock Jitter

Time Domain



Noise due to 5 ps rms Tx CLK Jitter, BW 1-10 MHz

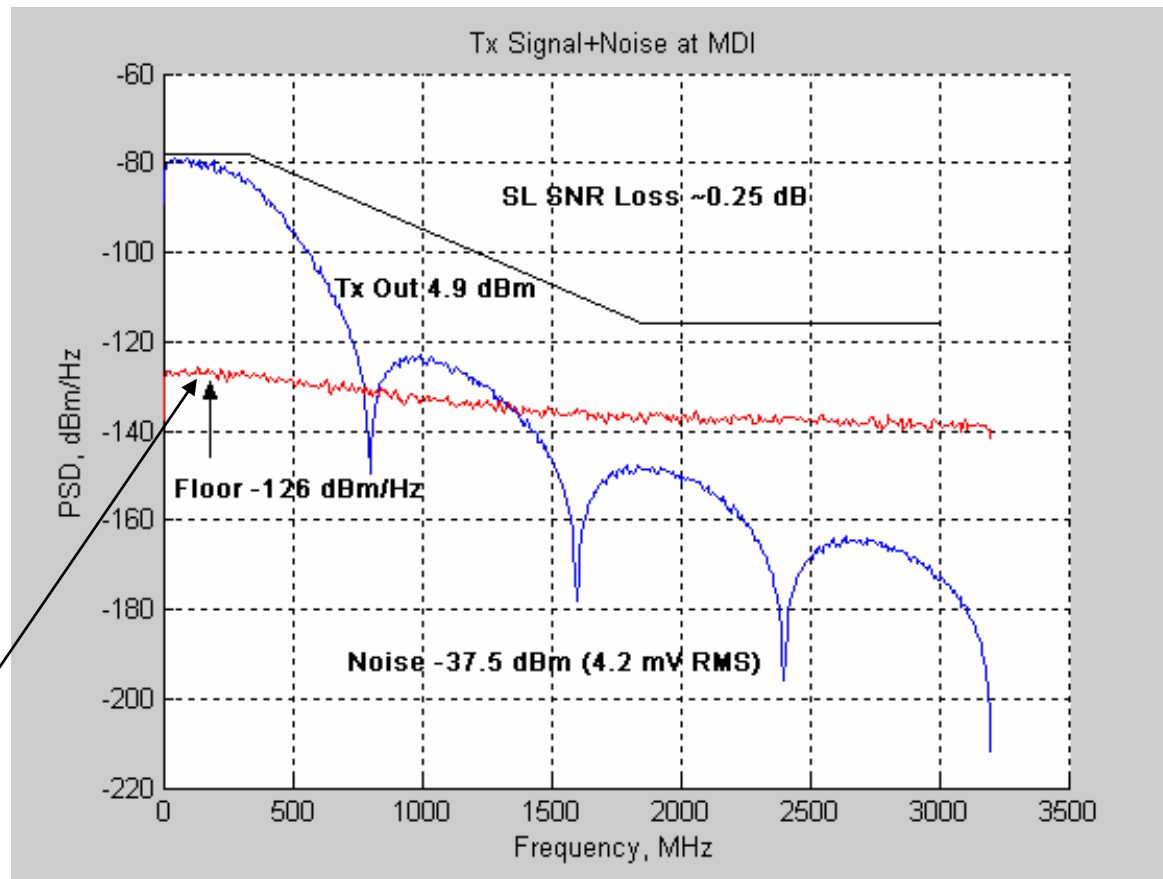


Centered Non-Gaussian Distribution

Will Reduce with Power Back-off → SNDR Maintained

Tx Impairments – Q- and Background Noise

Frequency Domain



Q- and Thermal
Noise -126 dBm/Hz

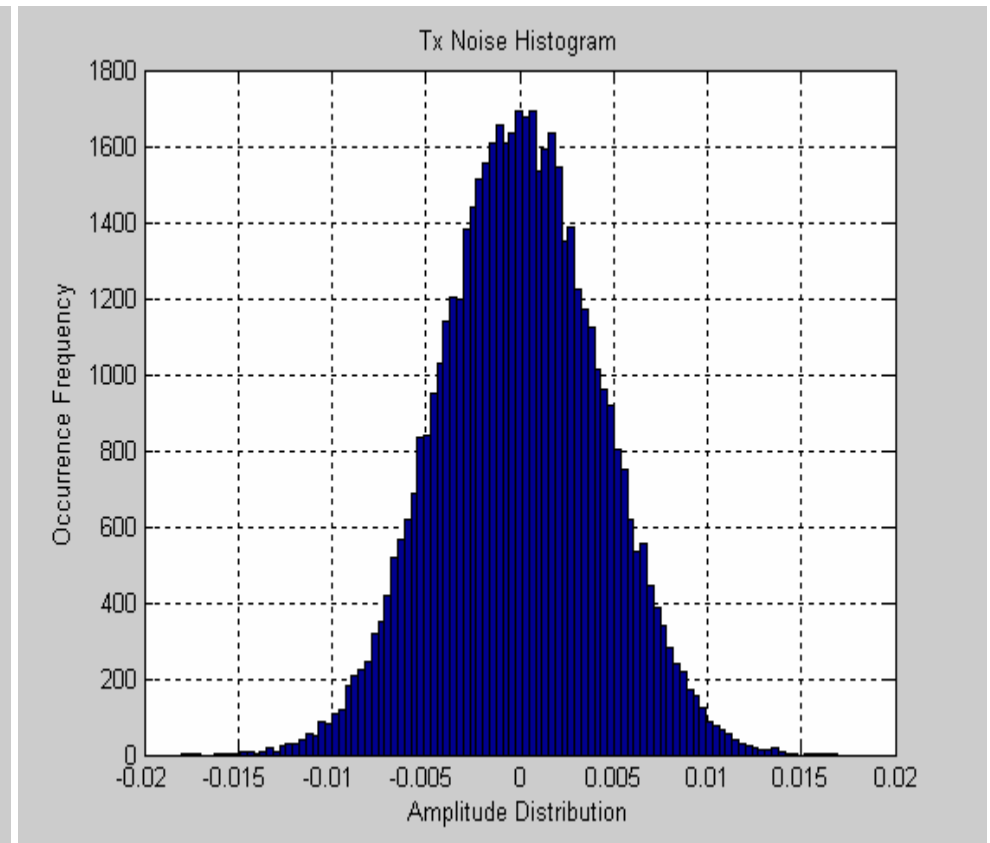
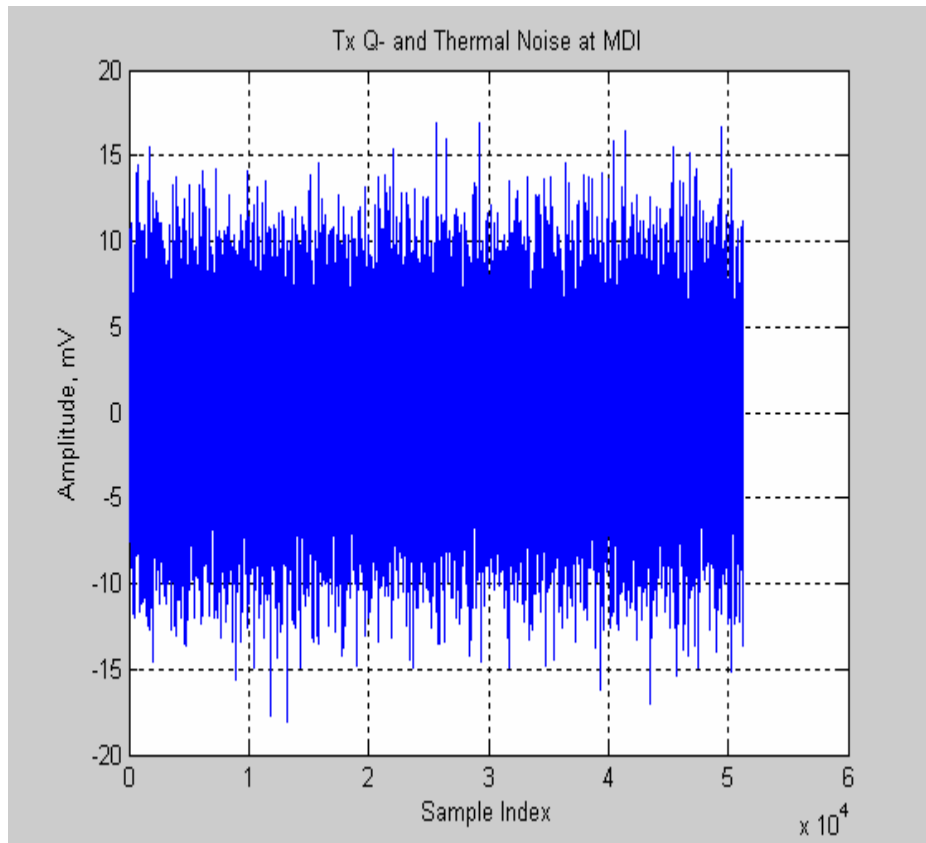
Budget:
9 ENOB DAC
Therm. -129 dBm/Hz
Gain < 2

-126 dBm/Hz max
App. White in-Band

Tx SNR 42.4 dB
SL SNR Loss 0.25 dB

Tx Impairments – Q- and Background Noise

Time Domain



Quantization and Background Noise -126 dBm/Hz

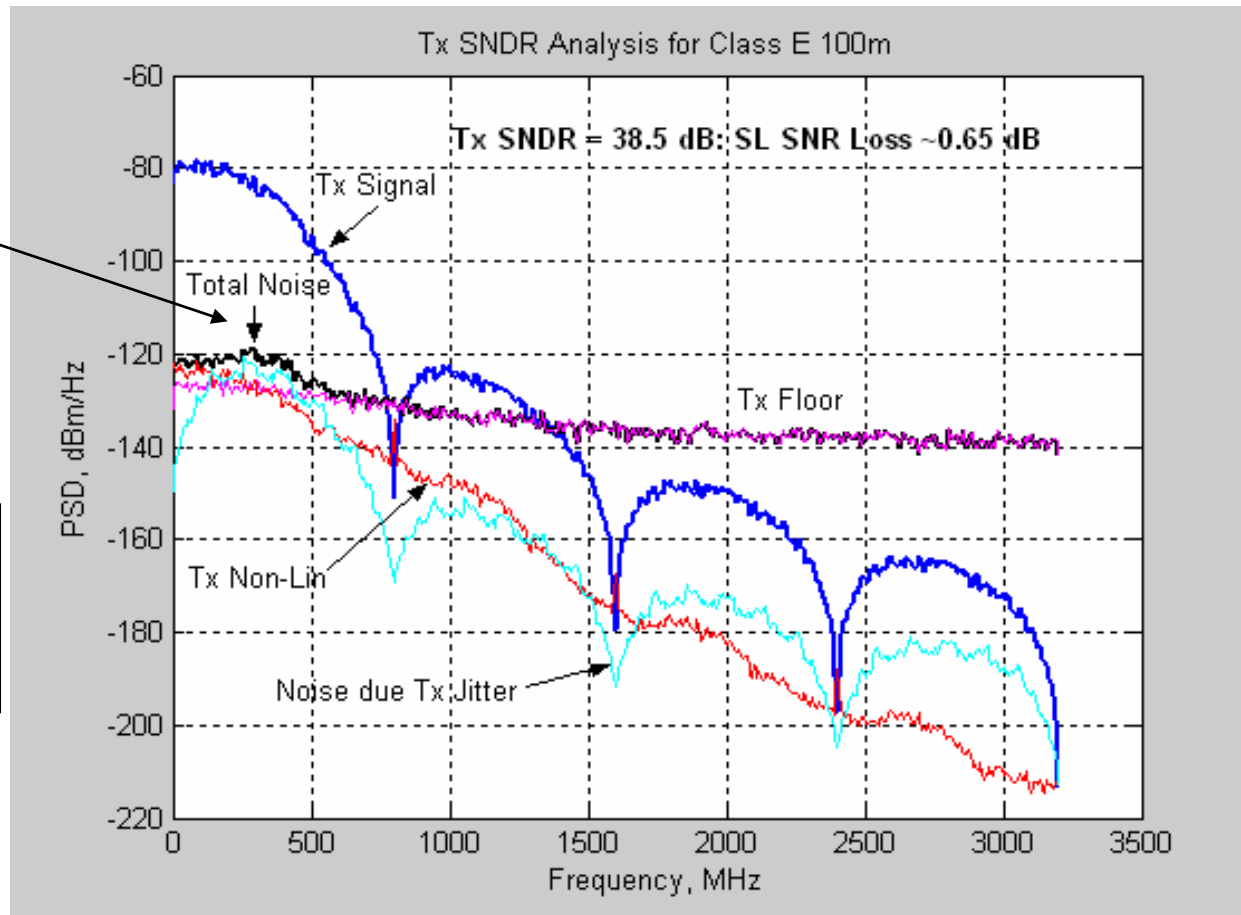
Centered Gaussian-like Distribution



May or May NOT Reduce with Power Back-off → SNDR May Degrade

Tx Impairments – Overall Noise and Distortion

Frequency Domain



TOTAL Noise
-119 dBm/Hz max
Slightly Colored

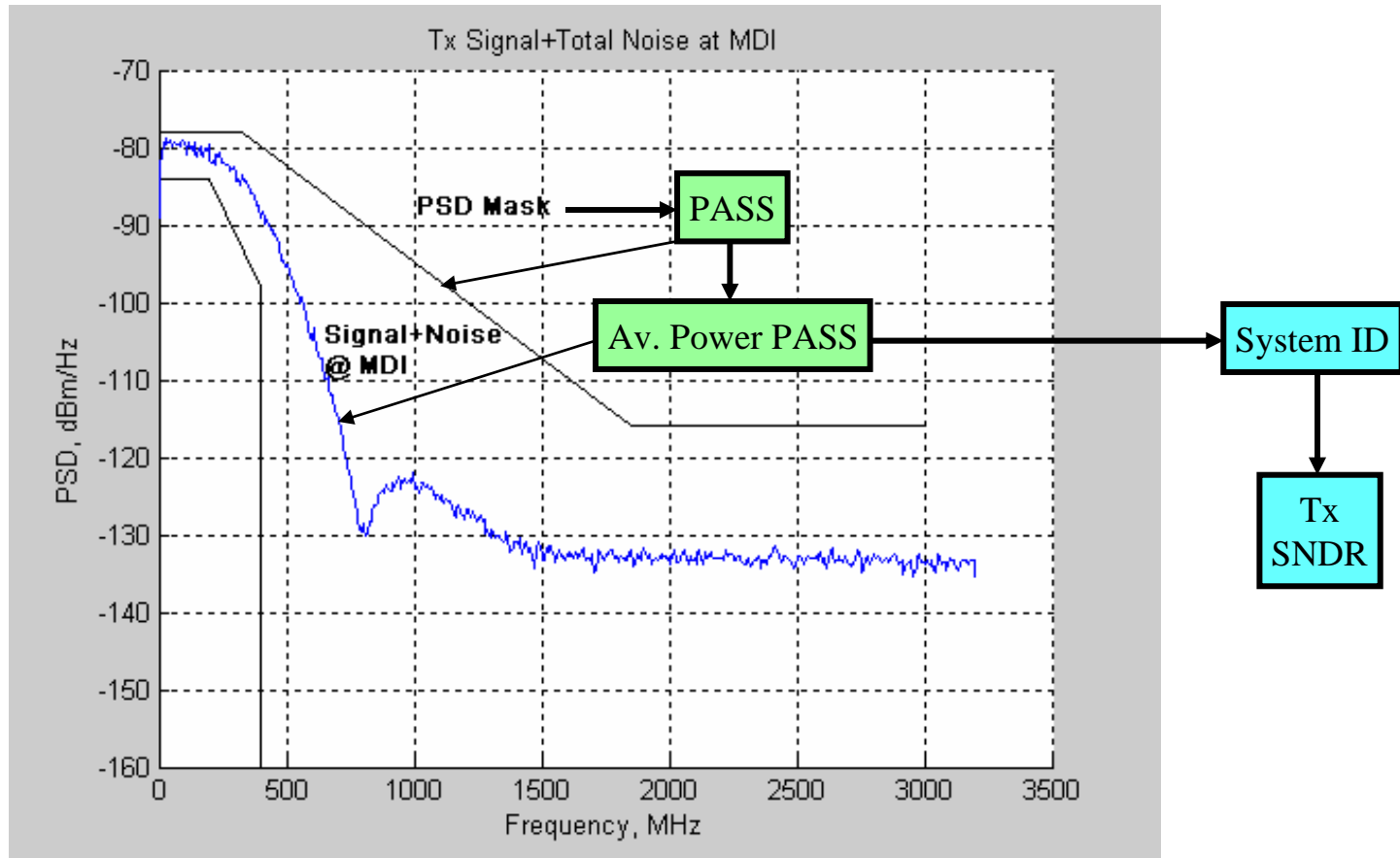
Tx SNDR 38.5 dB
SL SNR
Loss < 0.65 dB

“Normal” Operation Waveform SNDR in BW $\geq F_s$
is a Good Metric for Transmitter Characterization

Tx Impairments – What is Observed at MDI

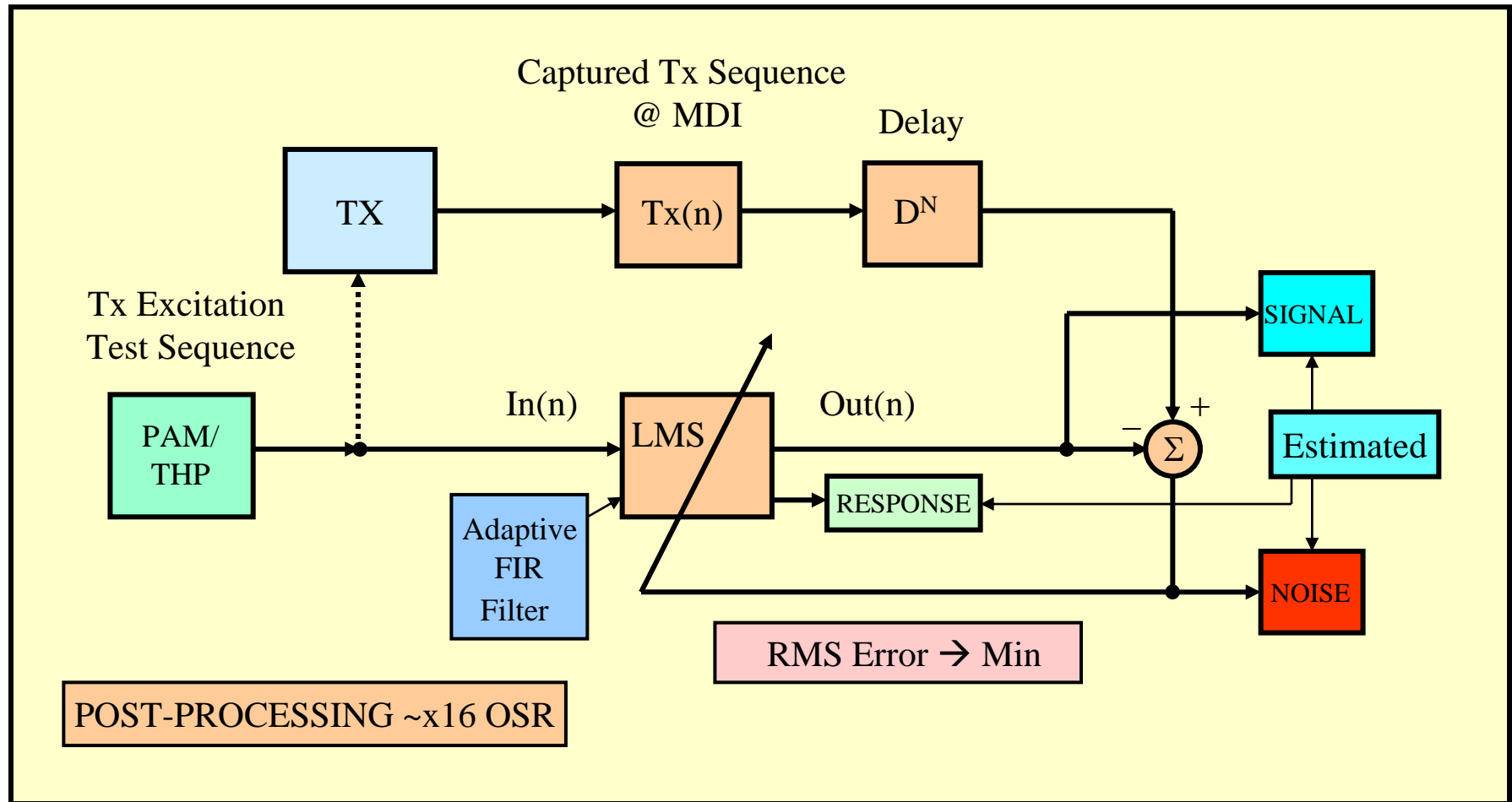
Time-Domain Sequence → Frequency Domain Analysis

How to Separate:
TOTAL NOISE
From
SIGNAL



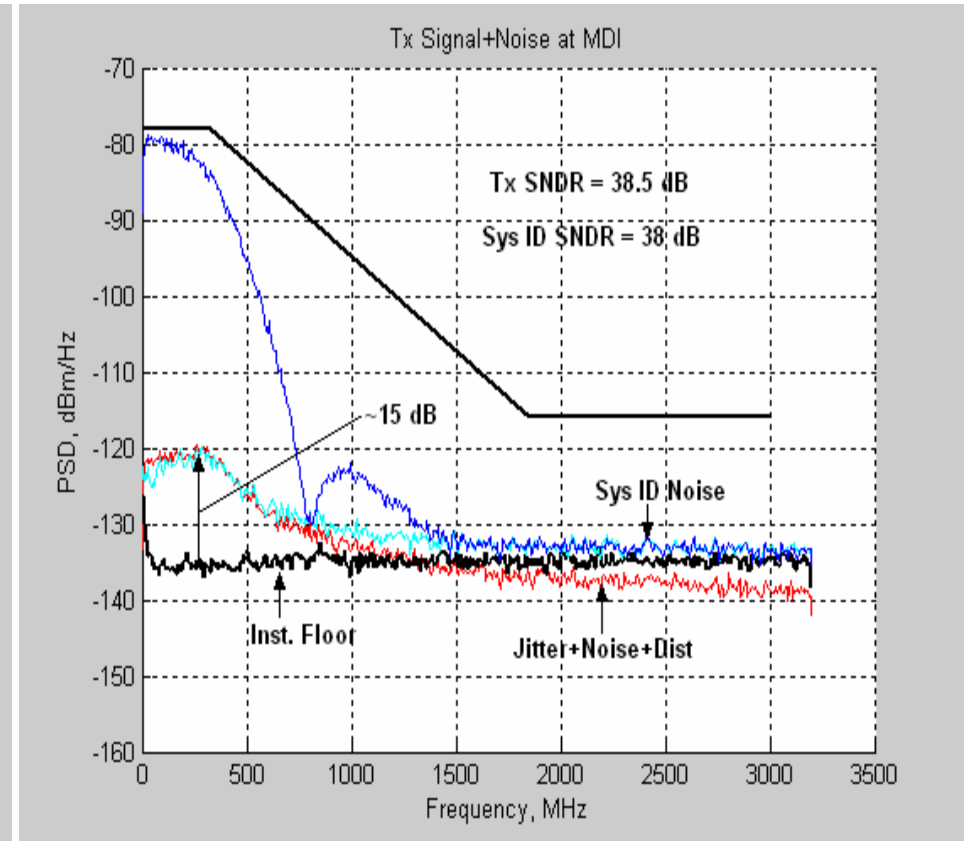
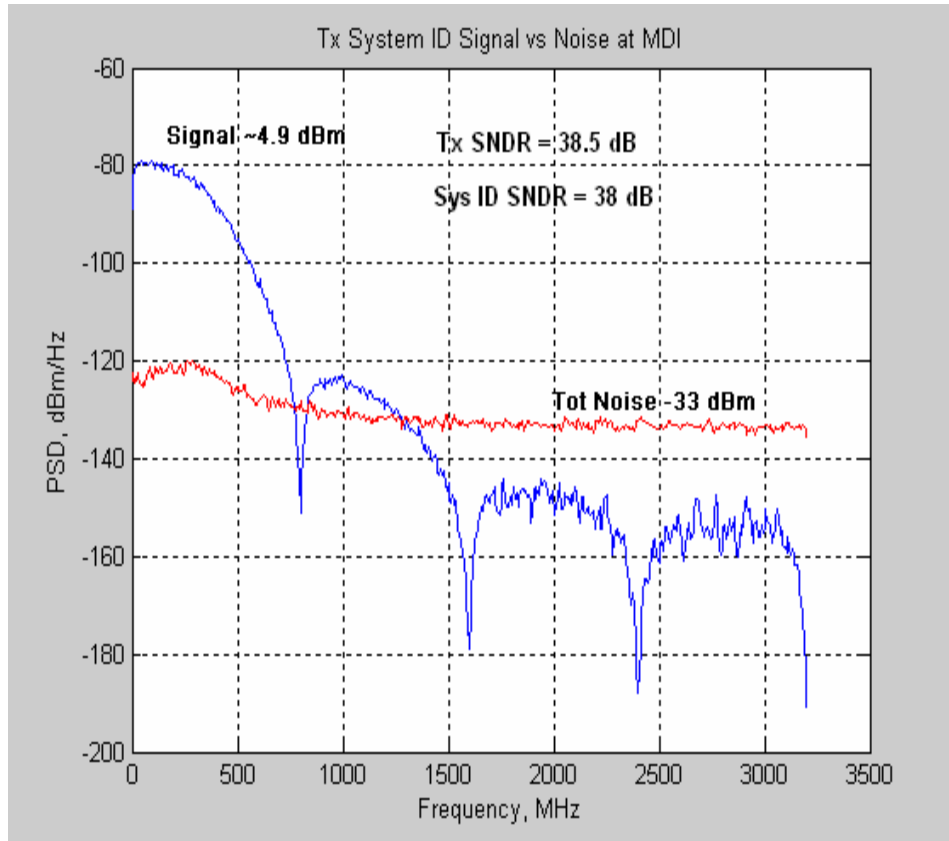
PSD Mask and Average Output Power Compliance Checked Before SNDR

System ID Signal Post-Processing Scheme



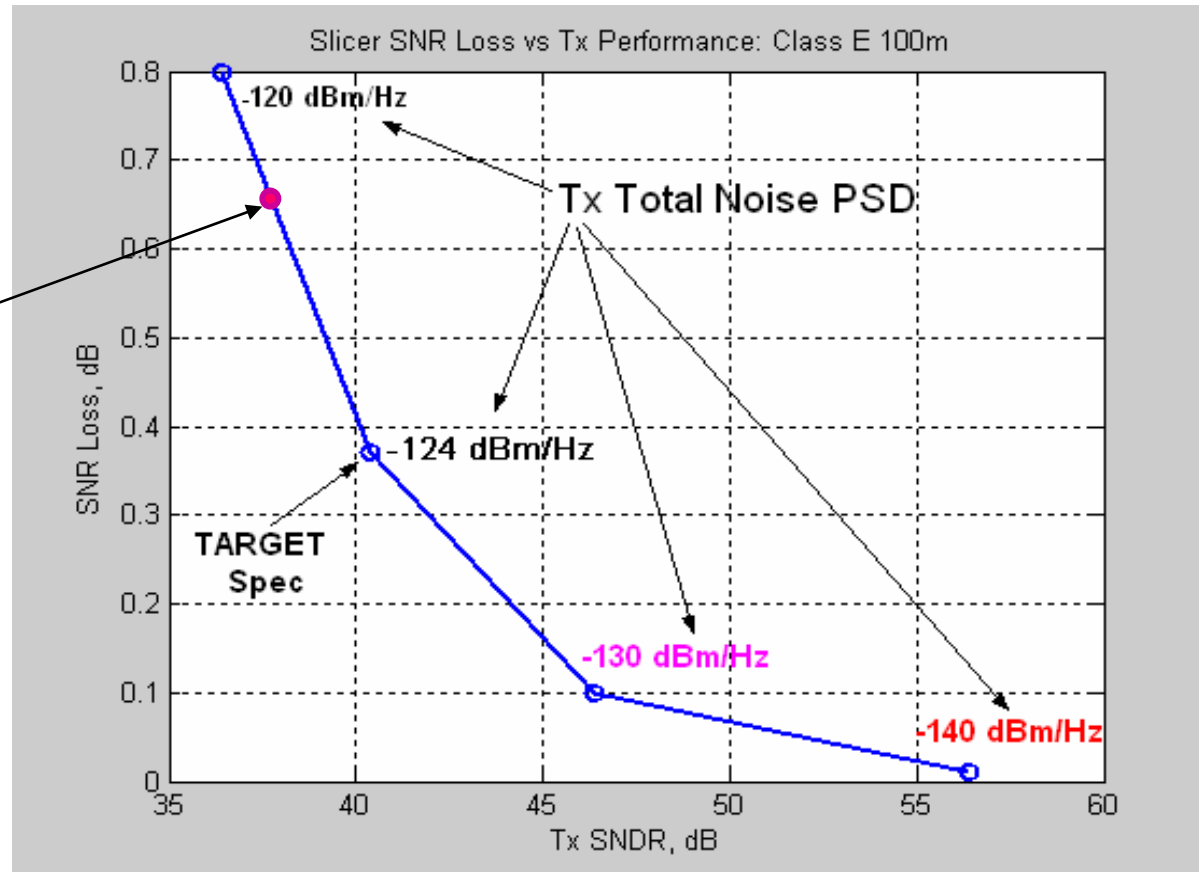
System ID Estimated Signal and Total Noise

Time-Domain Processing → Frequency Domain Analysis



Example Tx Impairment SNDR: Actual 38.5 vs 38 dB System ID Estimated in ~ 3GHz BW

Proposed System ID Tx SNDR Specification



Analyzed
EXAMPLE
SYSTEM:
Reasonably High
Performance/
Difficulty

@ MDI
Into 100 Ohm

$$Tx_SNDR = \frac{\text{Estimated \{Tx Output Signal Power\}}}{\text{Estimated \{Tx Output Total Noise Power\}}} \geq 40 \text{ [dB]}$$

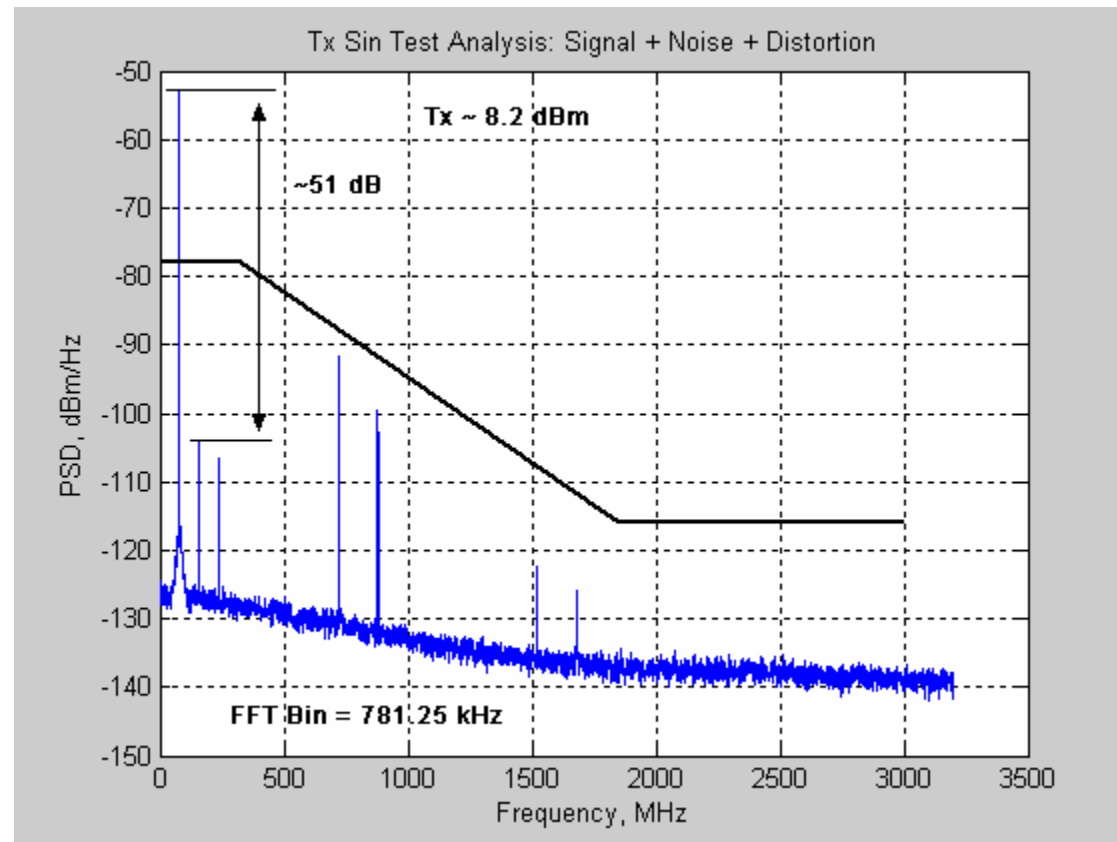


Conclusion

- **Based on Detailed Analysis of Transmitter Major Impairments SNDR ≥ 40 dB Objective Provides a Reasonable Feasibility and Complexity Trade-off between Transmitter and Receiver Sections, and is Proposed for the PHY Interoperability Compliance Testing at MDI**
- **Transmitter Qualification SNDR Metric at MDI and its Derivation Methodology Based on System ID Approach is Introduced**
- **Complimentary THP Processor Interoperability Compliance Method Needs to be Additionally Defined**

Back Up Slides

Non-Linear Distortion Single-Tone Test

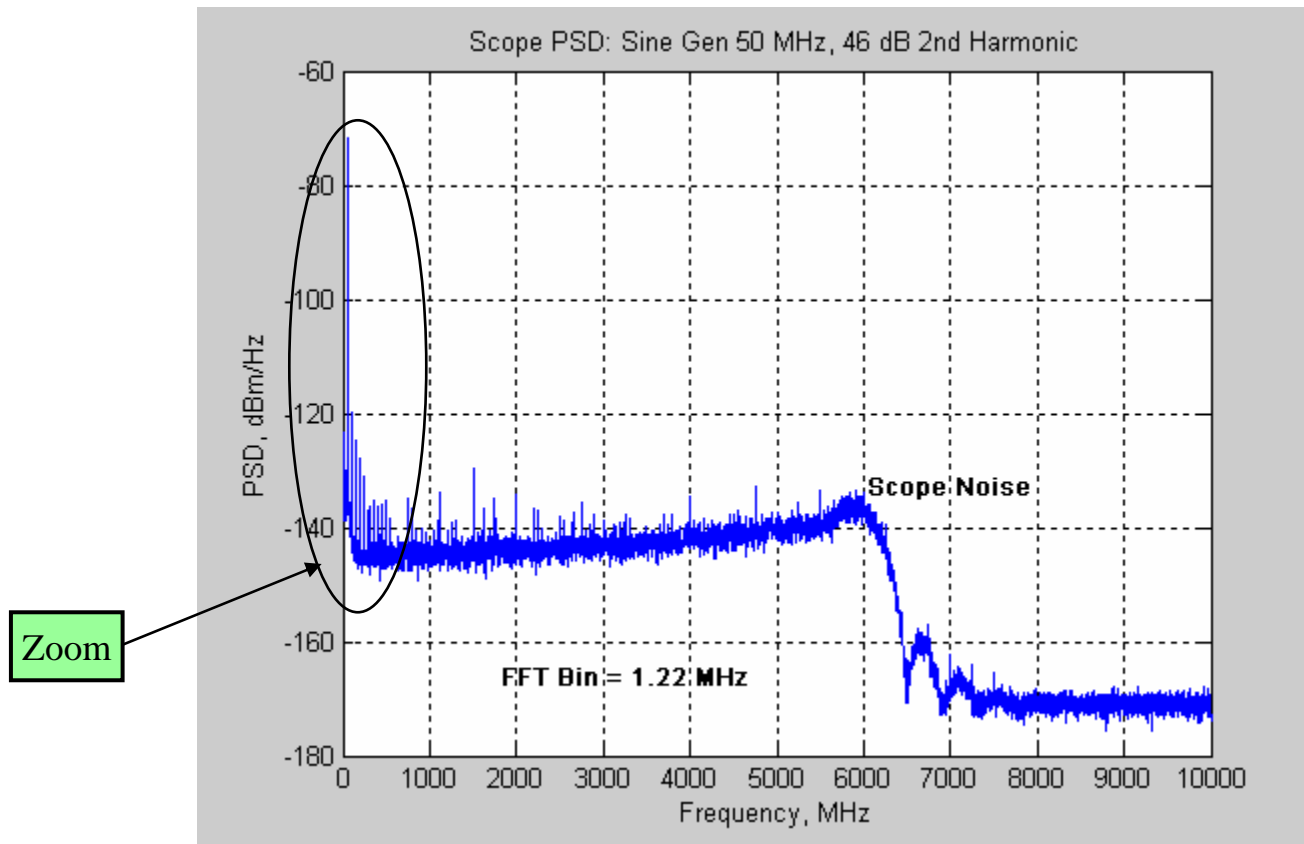


Total Output Power
Tx +16, -16 Sym
> 8 dBm
OVERLOAD

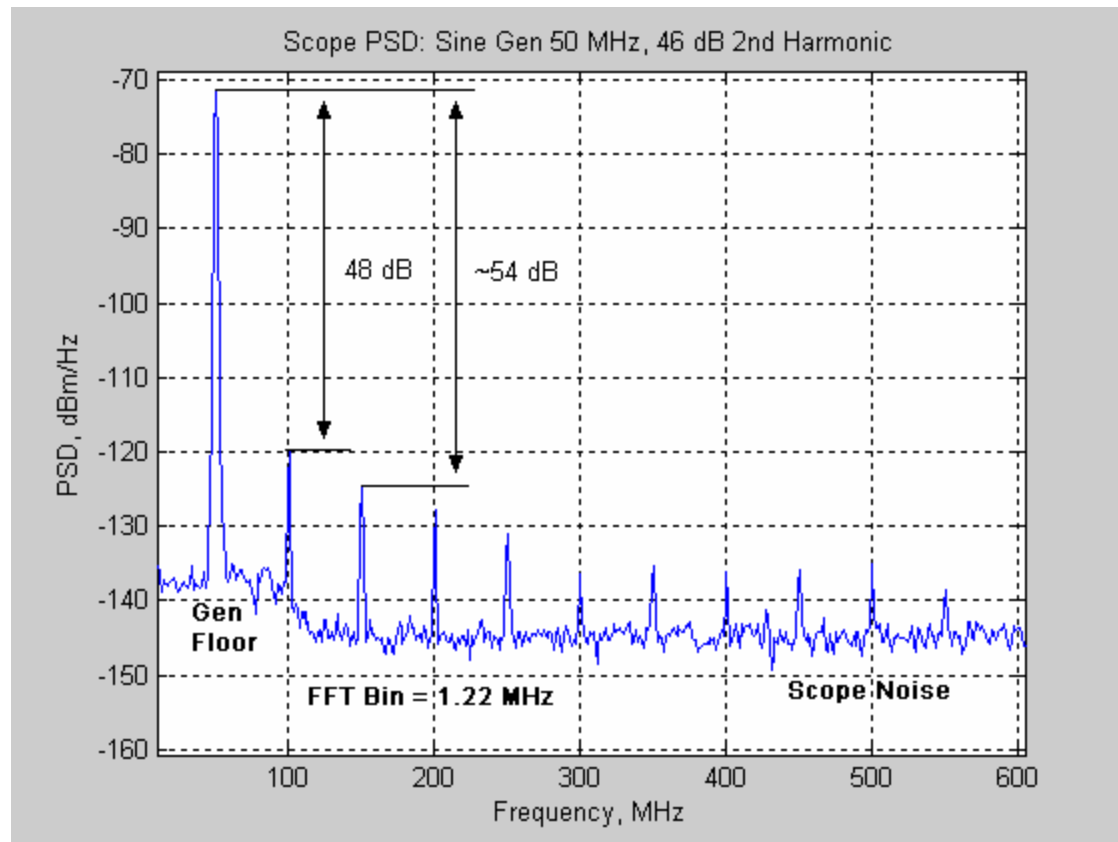
Single Tone SNDR Test: Non-Linear, 5 ps Jitter, Q- and Background → Pass

Actual Normal Operation SNDR = 38.5 dB < 40 dB → Fail

Scope Source 50 MHz, ~46 dB 2nd



Scope Source 50 MHz, ~46 dB 2nd → Zoom



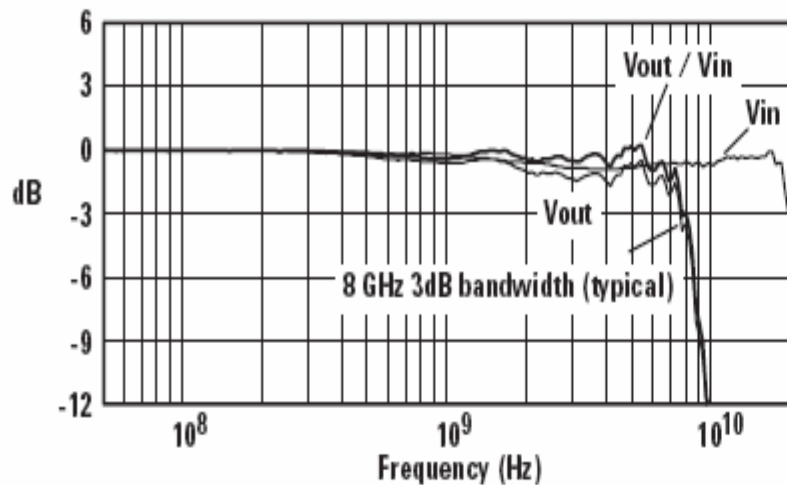
Scope Captured Sine Generator THD – Confirmed by Spectrum Analyzer

Diff Probe Characteristics

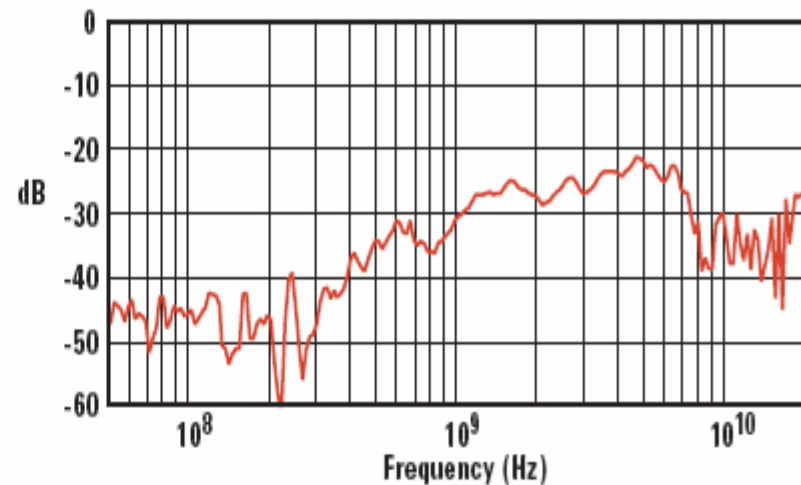
Input Noise = 3 mV in 7 GHz \rightarrow 36 nV/sqrt(Hz)

-139 dBm/Hz

Ref. to 316.2 mV into 100 Ohm (0 dBm)

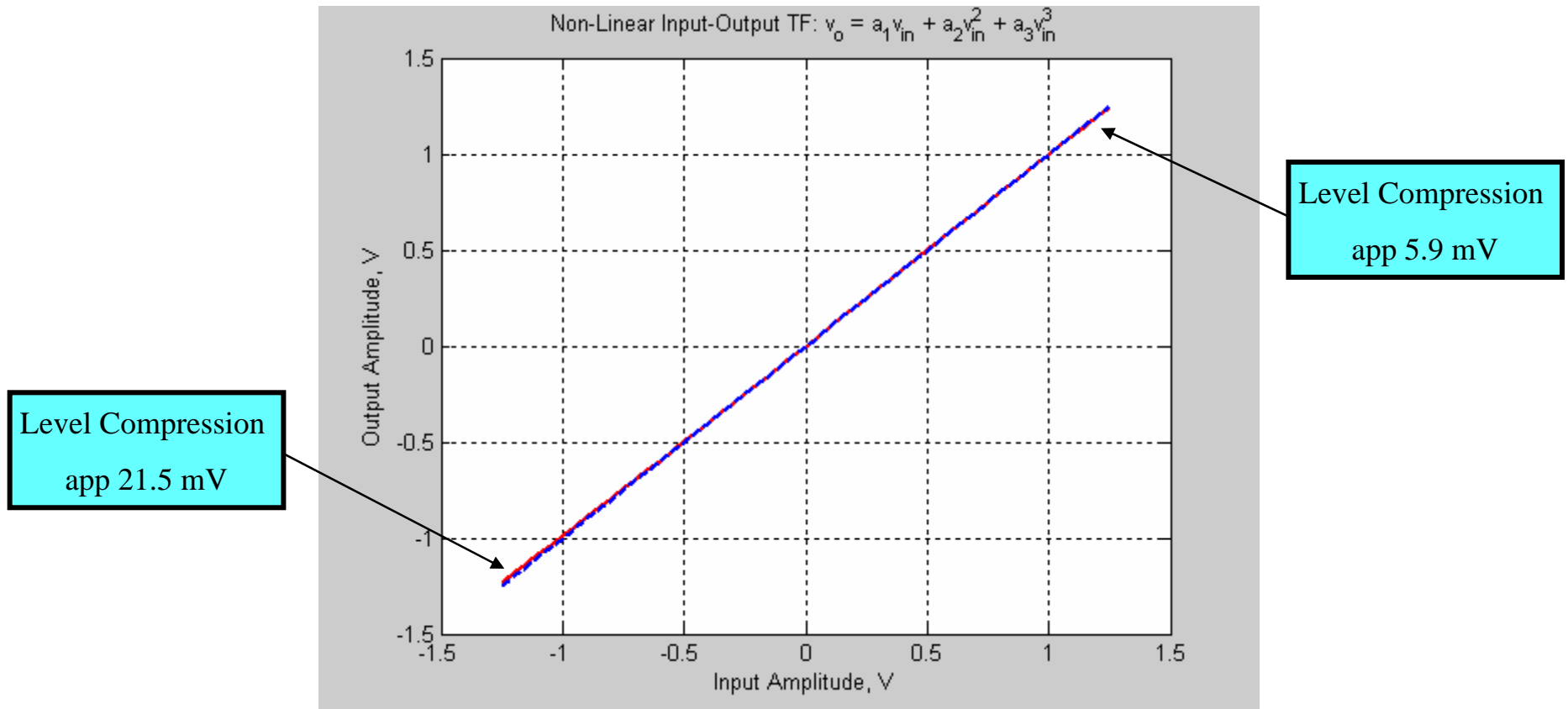


Swept frequency response



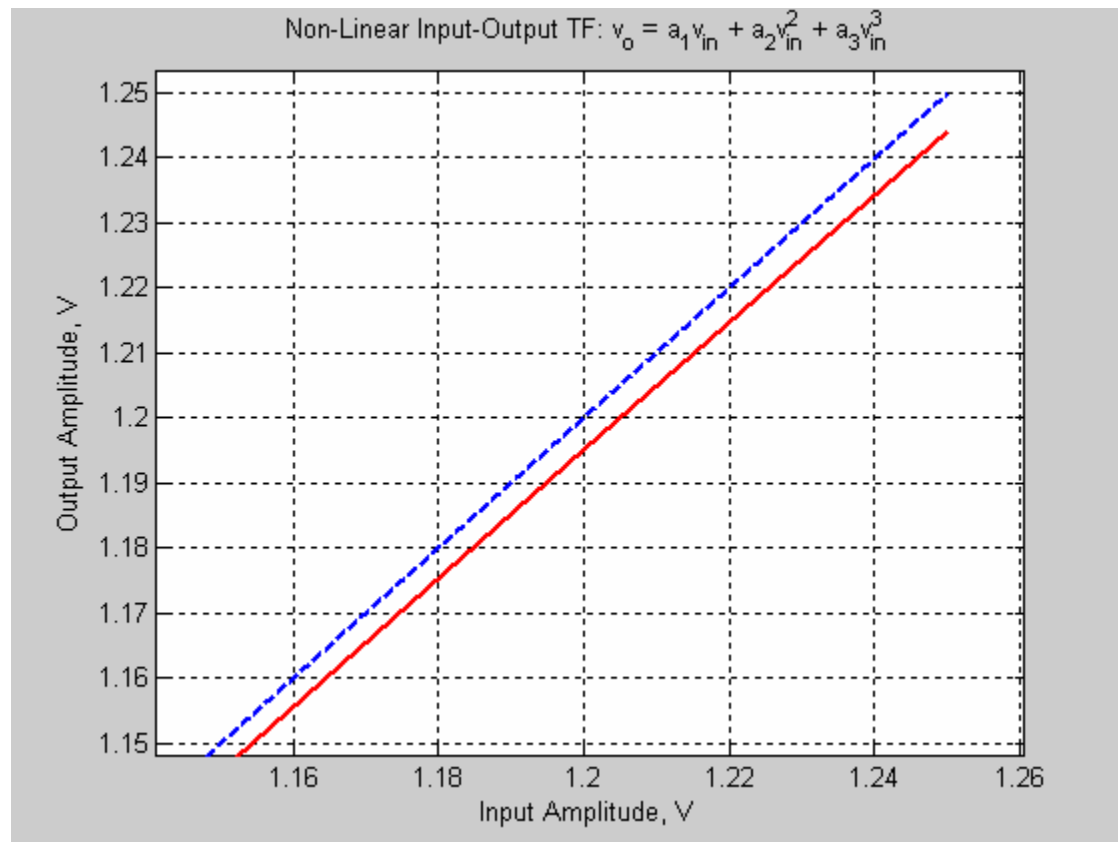
Common mode rejection vs. frequency

Non-Linear Input-Output TF



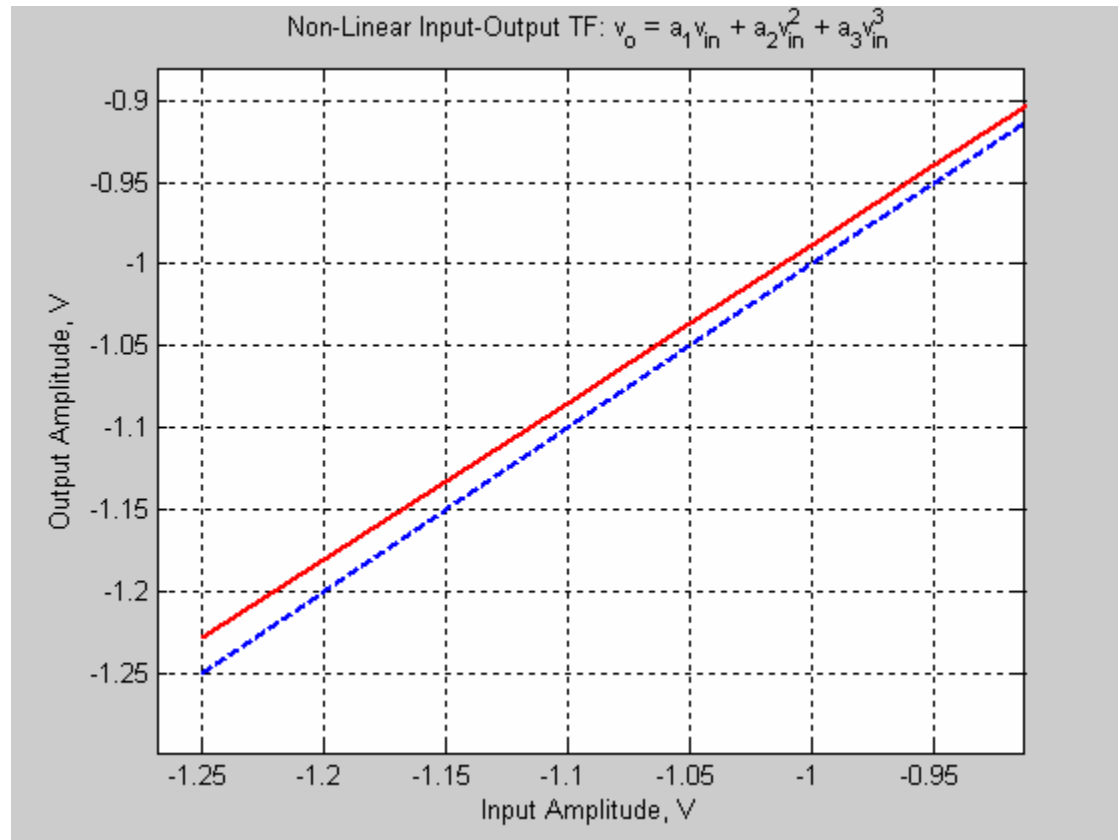
Non-Linear 3rd-Order Asymmetric Input-Output Transfer Function
(Frequency-independent)

Non-Linear Input-Output TF



Non-Linear 3rd-Order Asymmetric Input-Output Transfer Function
Compression “Positive”

Non-Linear Input-Output TF



Non-Linear 3rd-Order Asymmetric Input-Output Transfer Function
Compression “Negative”