# Proposal for Transmitter Electrical Specifications

**IEEE P803.2an Task Force**
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# Objectives

- **Establish Transmitter Electrical Specifications**
  - **Transmitter linearity (paragraph 55.5.4)**
  - **Transmitter PSD and power level (paragraph 55.5.6)**
  - **Transmitter clock frequency (paragraph 55.5.7)**
- **Specifications Based on Interoperability Requirements**
  - **Electrical specifications that affect interoperability are normative**
    - **Primary requirement is transmit SNR > 40 dB (broadband average from 1 to 400 MHz)**
  - **Electrical specifications that go beyond interoperability restrict ability of manufacturers to optimize performance**

# Objectives

- **Specifications Tied to Objective Measurements**
  - **Measurements should be possible with commercial lab equipment**
  - **Errors due to lab equipment accuracy must be negligible**
  - **Measurement procedures must be unambiguous**
  - **Elaborate custom test fixtures should not be required**

# Transmitter Linearity

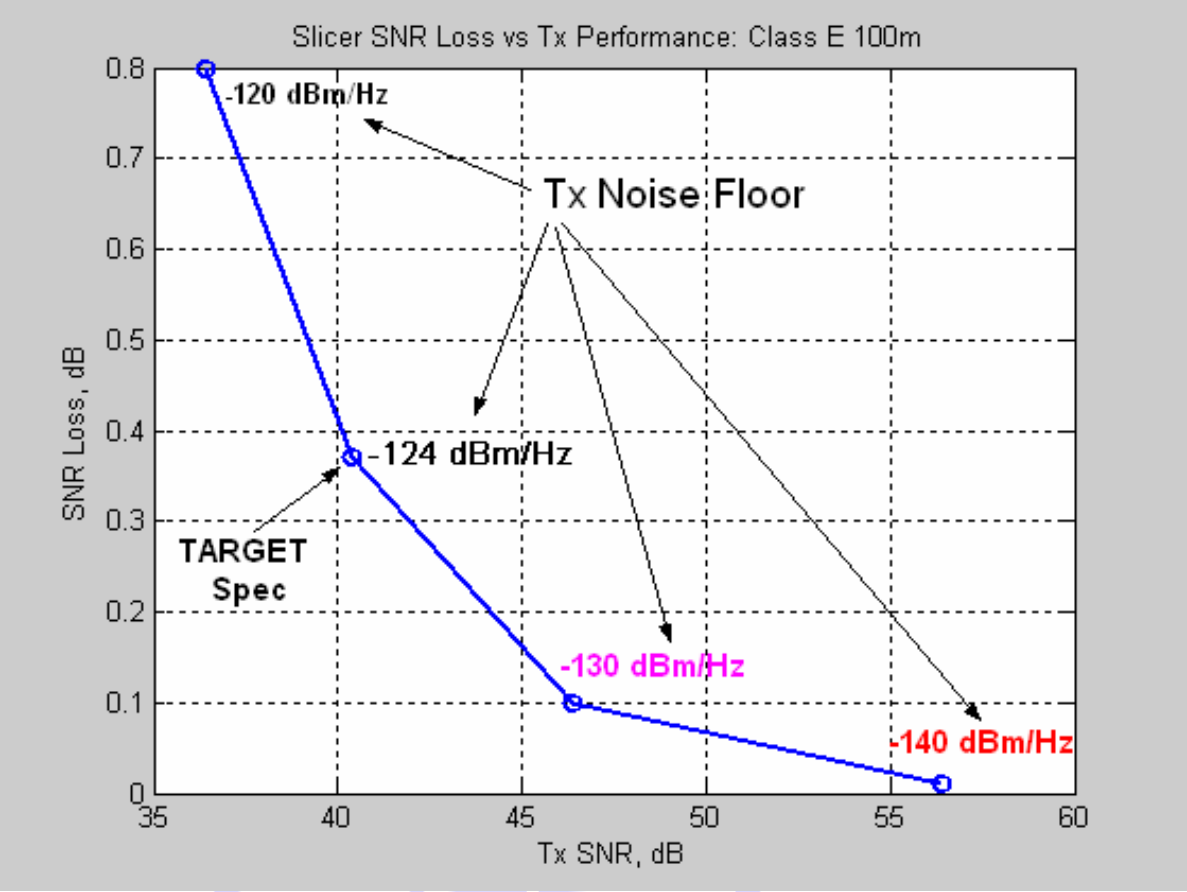
- **Combine Linearity and Timing Jitter Requirements into Specification for Signal to Noise Plus Distortion**
  - **For interoperability, separate specifications for distortion, noise, and jitter are not necessary**
  - **Allows transmitter implementation losses to be optimally allocated by PHY manufacturers**
  - **Test equipment limitations make accurate clock jitter measurements difficult at 10GBASE-T baud rates and jitter levels**
  - **Jitter measured on test clocks can be very different (better or worse) from jitter on MDI output due to buffering and test point accessibility**

# Transmitter Linearity

- **Signal to Noise plus Distortion Ratio Specification is Lower Bound on Transmit SNR Needed for Interoperability**

- **Signal to Noise plus Distortion Specifications Reflect Frequency Dependency of Distortion and Noise Requirements**
  - **Lower distortion and noise required at low frequencies**

# Transmitter Linearity




**Slicer SNR Loss vs Tx SNDR: Time Domain Simulation**

# Transmitter Linearity Specification

**55.5.4 Transmitter linearity**

When in Test mode 4 and transmitting on a single pair into a 100Ω differential resistive load per the test configuration shown in Figure 55-22, the signal to noise plus distortion ratio of the differential signal at the MDI output is required to be greater 40 dB in a broadband sense (1 to 400 MHz band), based on measurements made with either sinusoidal output waveforms, or alternatively, based on measurements made with precoded DSQ output waveforms.

For sinusoidal measurements, the MDI shall be configured to output single-tone and two-tone waveforms at the frequencies specified for the five test cases given in Table 55-x, such that the peak-to-peak output of the sinusoidal signal corresponds to ±16 with respect to a DSQ output signal. The measured signal to noise plus distortion ratio shall be greater than the values specified in Table 55-x. For two-tone waveforms, signal power shall be defined as the total (sum) power of both tones. Signal to noise plus distortion ratio measurements shall be made across a 1 MHz to 400 MHz band, using a resolution bandwidth of less than or equal to 100 kHz.

# Transmitter Linearity Specification

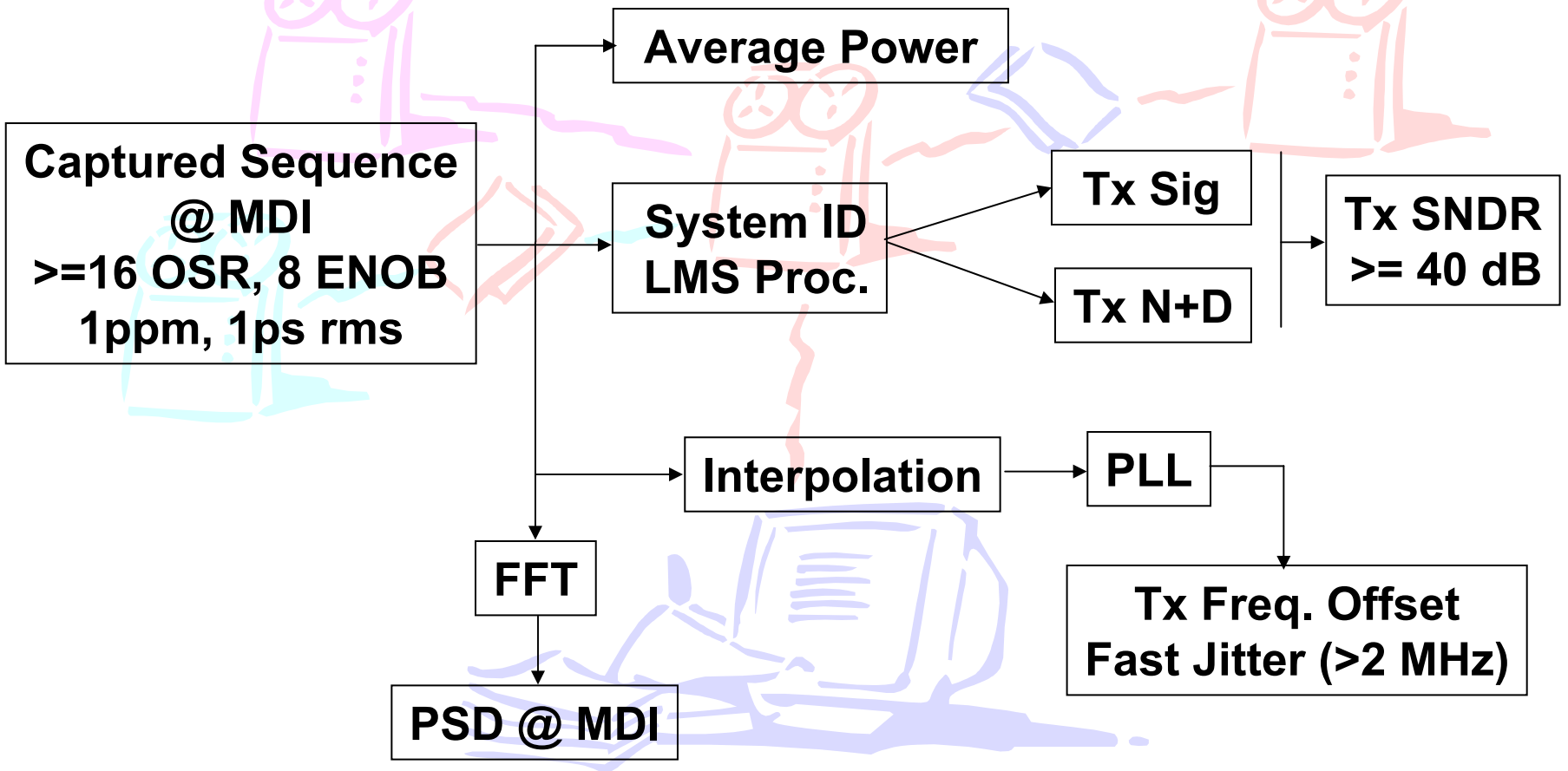
**Table 55-x: Signal to Noise Plus Distortion Requirements**

| Output Waveform Frequencies | SNDR Specification (dB) |
|---|---|
| Single tone: | |
| (101/1024)*800 MHz | 45 |
| (167/1024)*800 MHz | 43 |
| Two tone: | |
| (179/1024)*800 MHz, (181/1024)*800MHz | 43 |
| (277/1024)*800 MHz, (281/1024)*800MHz | 39 |
| (397/1024)*800 MHz, (401/1024)*800MHz | 36 |

# Transmitter Linearity Specification

- **Procedure for Measurement Using Precoded DSQ Waveforms Based on System ID Approach**
  - **Entire Tx Chain is Covered at MDI:**
    - **PCS, THP Bypass, THP Coefficients, Tx DSP (round-off, etc)**
    - **D-A, Analog Processing, Tx DRV, Line Interface, xFormer**
    - **Spurious due to On-Chip/Board Interference**
    - **Average Power at MDI - Normative**
    - **PSD Mask at MDI - Normative**
    - **SNDR at MDI - Normative**
    - **Tx Chain Noise and Distortion Spectral Analysis**
    - **Tx CLK Frequency and Fast Jitter - Normative**
  - **No Balun or Elaborate Custom Test Fixtures Required**
  - **Exact Procedure and processing algorithms (TBD) – will Follow (see Takatori_1_1104)**

# System ID Approach Flow

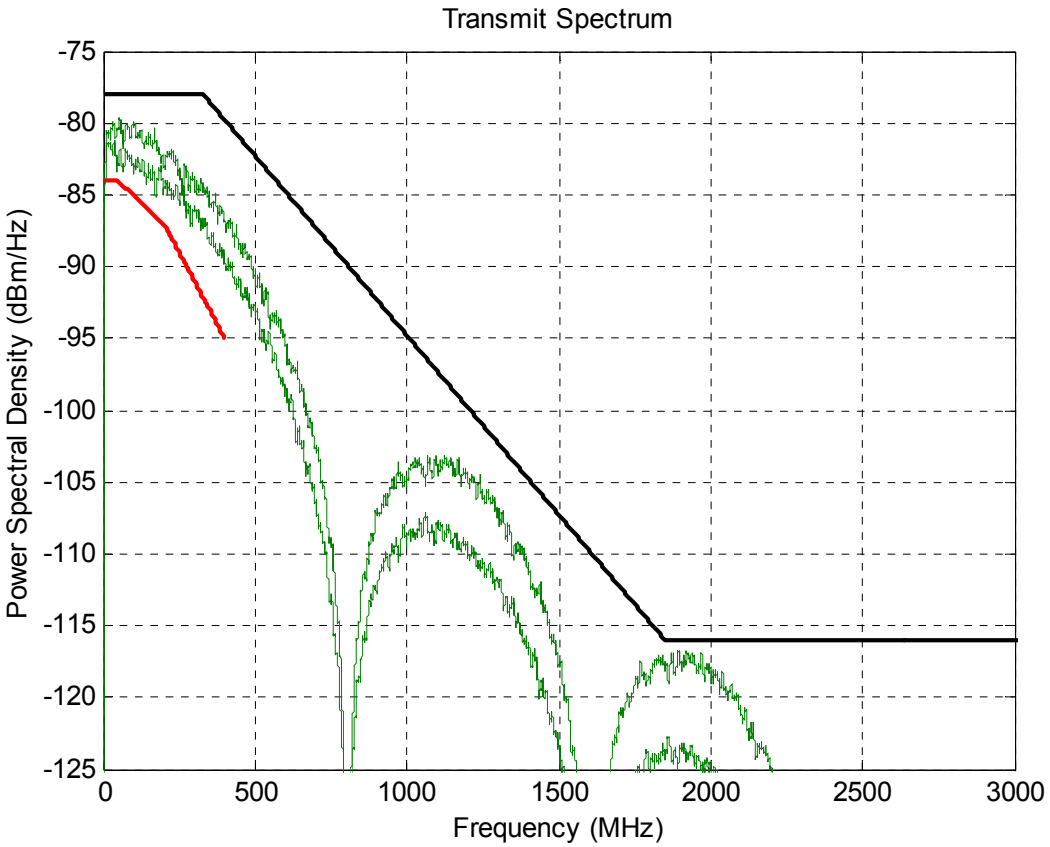


# Transmitter PSD / Output Power

- **Output Power and PSD Specifications Replace for Output Voltage and Output Droop Specifications**
  - **For interoperability, additional specifications for output voltage and output droop are not necessary**
    - **For reference, 3.2 dBm to 5.2 dBm output power corresponds to settled output voltage of 1.85 Vpp to 2.25 Vpp, in 3 dB bandwidth of 450 MHz**
  - **Minimum Output Power Necessary to Ensure Sufficient SNR Margin in the Presence of 1000BASE-T ANEXT and Background Noise**
  - **Maximum Output Power Necessary to Manage Levels of 10GBASE-T ANEXT and 10GBASE AFEXT**
  - **Upper Mask Provides EMI-Based Bound for TH Precoded DSQ Signals (see pagnanelli_2_1104)**
  - **Lower Mask Ensures Output Spectrum is Compatible with Expected Equalizer Capabilities, including Output Droop**

# Transmitter PSD / Output Power

- **Output Power Range Compatible with EMI Compliant PSD Masks**



# PSD and Power Specification

**55.5.6 Transmitter power spectral density (PSD) and power**

In test mode 5 (normal operation with no power back-off), the transmit power shall be in the range 3.2 dBm to 5.2 dBm and the power spectral density of the transmitter, measured into a 100Ω differential resistive load, shall be below the upper mask and above the lower mask specified in Figure 55-26, which corresponds to:

# PSD and Power Specification

$$\text{Upper PSD Mask}\,(f_{\text{MHz}}) = \begin{cases} -78\ \text{dBm/Hz}, & 1 \le f_{\text{MHz}} \le 330 \\ -78 - \left(\dfrac{f_{\text{MHz}} - 330}{40}\right)\ \text{dBm/Hz}, & 330 < f_{\text{MHz}} \le 1850 \\ -116\ \text{dBm/Hz}, & 1850 < f \le 3000 \end{cases}$$

$$\text{Lower PSD Mask}\,(f_{\text{MHz}}) = \begin{cases} -84\ \text{dBm/Hz}, & 1 \le f_{\text{MHz}} \le 50 \\ -84 - \left(\dfrac{f_{\text{MHz}} - 50}{50}\right)\ \text{dBm/Hz}, & 50 < f_{\text{MHz}} \le 200 \\ -87 - \left(\dfrac{f_{\text{MHz}} - 200}{25}\right)\ \text{dBm/Hz}, & 200 < f \le 400 \end{cases}$$

# Transmitter Clock Frequency

- **Required Specification**

  **55.5.7 Transmitter clock frequency**

  The symbol transmission rate on each pair of the Master PHY shall be 800 Mbaud ± 50 ppm.

- **Frequency References with ± 50 ppm Tolerance are Readily Available**

- **Tighter Tolerance Eases Tracking Requirements of Low-Jitter Loop Timing Recovery Circuits**

# Conclusion

- **Specific Transmitter Electrical Specifications have been Established Based on Interoperability Requirements**

- **Specifications are Tied to Objective Measurements that can be Made Accurately with Basic Lab Test Equipment and Simple Procedures**