10GBASE-T PAM Scheme: Proposed Overall Architecture

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Overview of Presentation

1. **Architecture Overview** — **Scott Powell, Broadcom**
2. **Framing and Control** — **Jose Tellado, Teranetics**
3. **Power Backoff** — **Hiroshi Takatori, Keyeye**

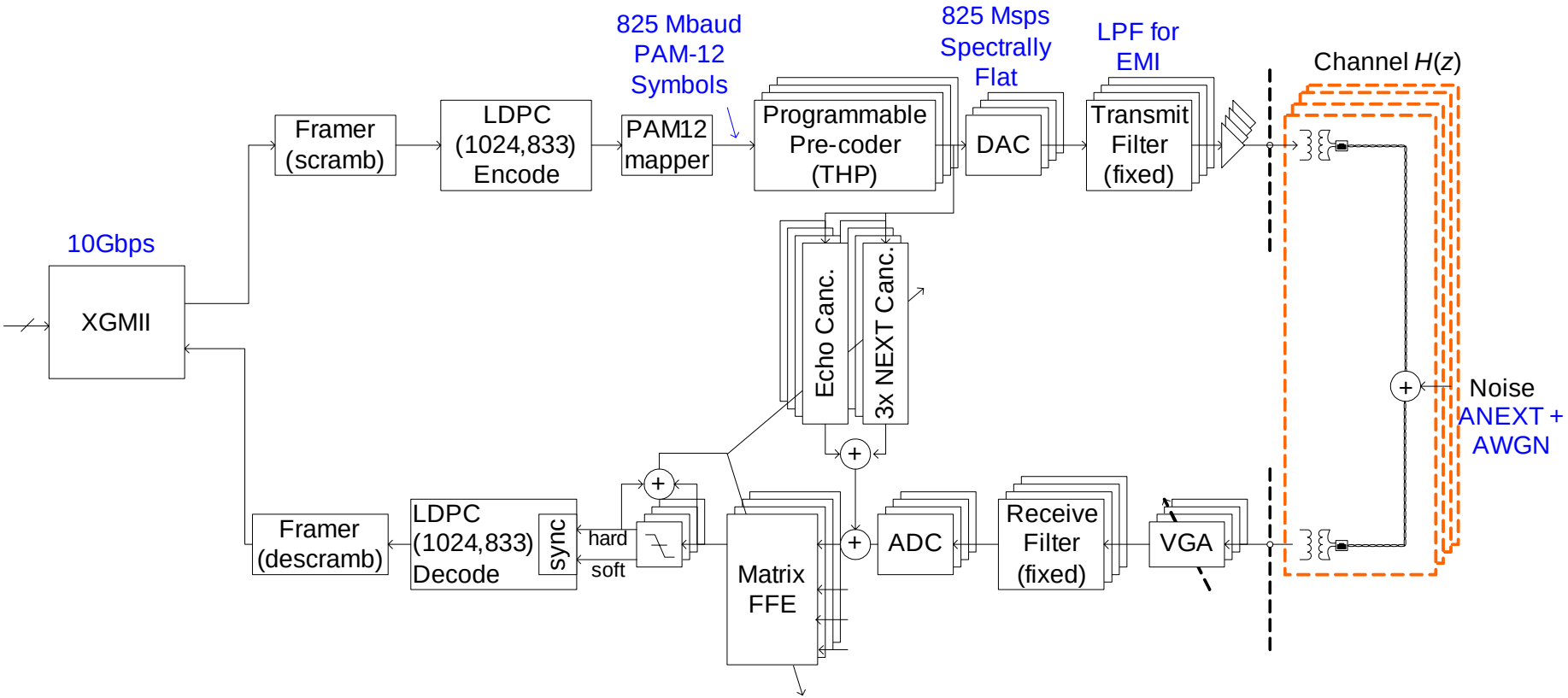
- See also:
  - ungerboeck_1_0704.pdf for precoder analysis
  - seki_1_0704.pdf presentation for channel code details

Overall 10GBASE-T Specification

Modulation Code	**Baseband PAM-12**
Baud Rate	**825 Mbaud**
Channel Code	**LDPC (1024,833)*, systematic**
Framing & Control	**64B/65B + ~10Mbps embedded channel**
Transmitter Equalization	**Tomlinson-Harashima Precoding****
THP Adaptation	**Programmable*****
Transmit Filter	**Spectral mask (tbd***)**
Transmit Power	**5dBm at MDI**
Receive Filter	**Low order CT (tbd***)**
Receiver Equalization	**Adaptive (vendor specific)**
MAC Interface	**XGMII**

*** Baseline code – open to better code, if found**
**** See powell_1_0504.pdf for justification**
***** See ungerboeck_1_0704.pdf for analysis**

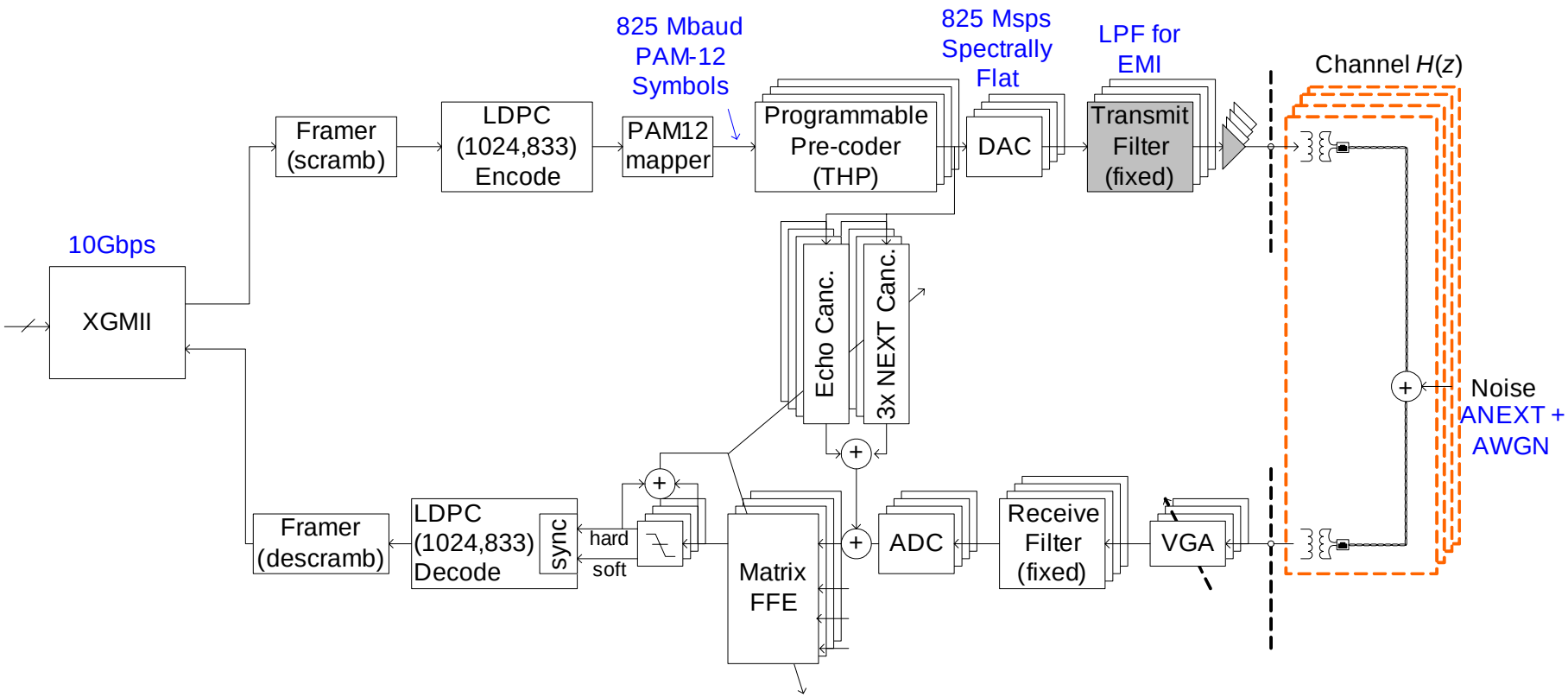
Example System Architecture



- **Implementation used for analysis**

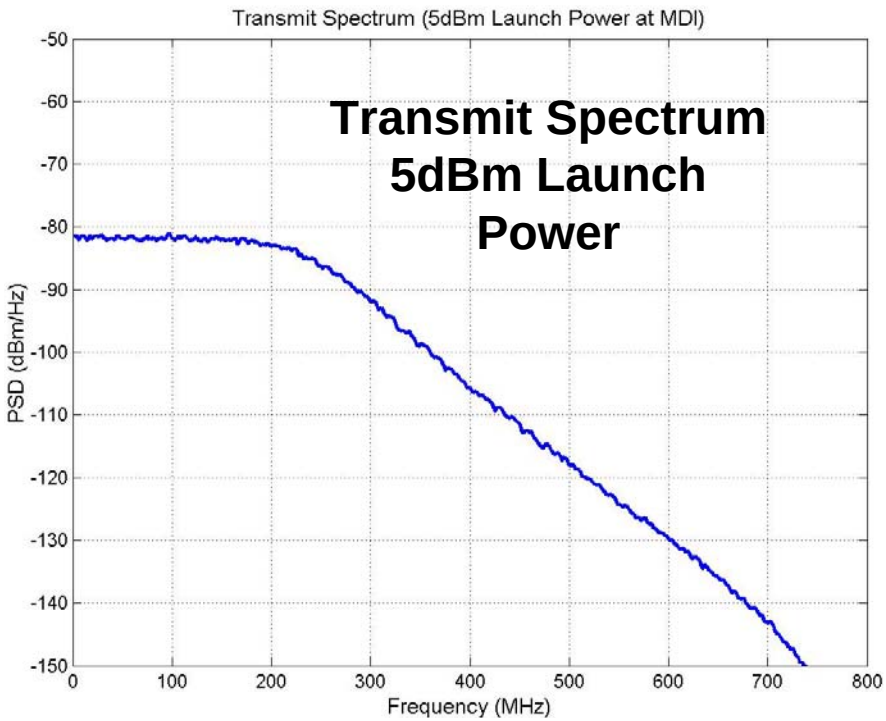
- **Other implementations possible**

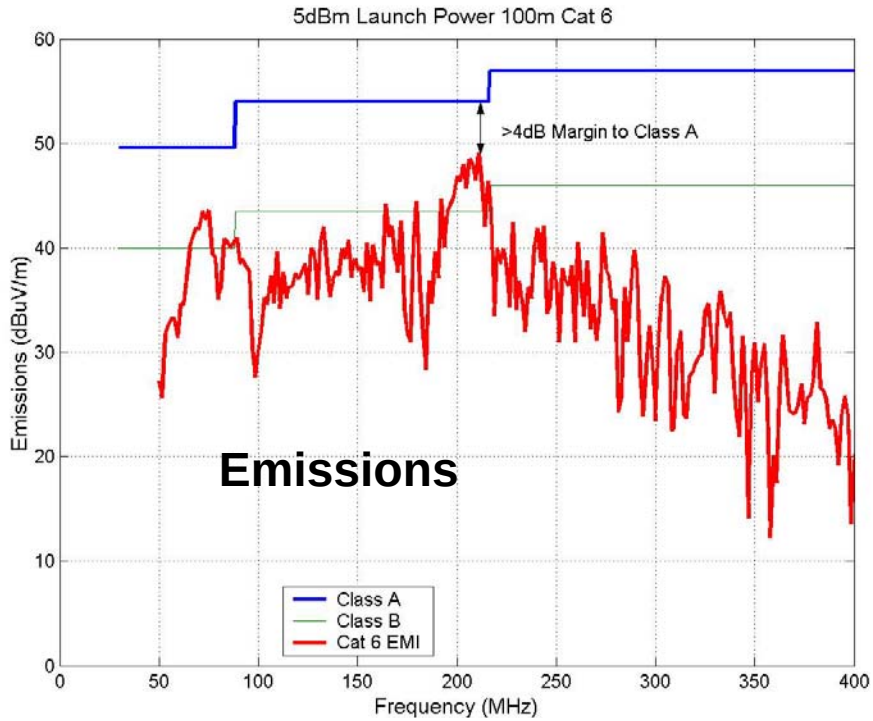
Transmitter



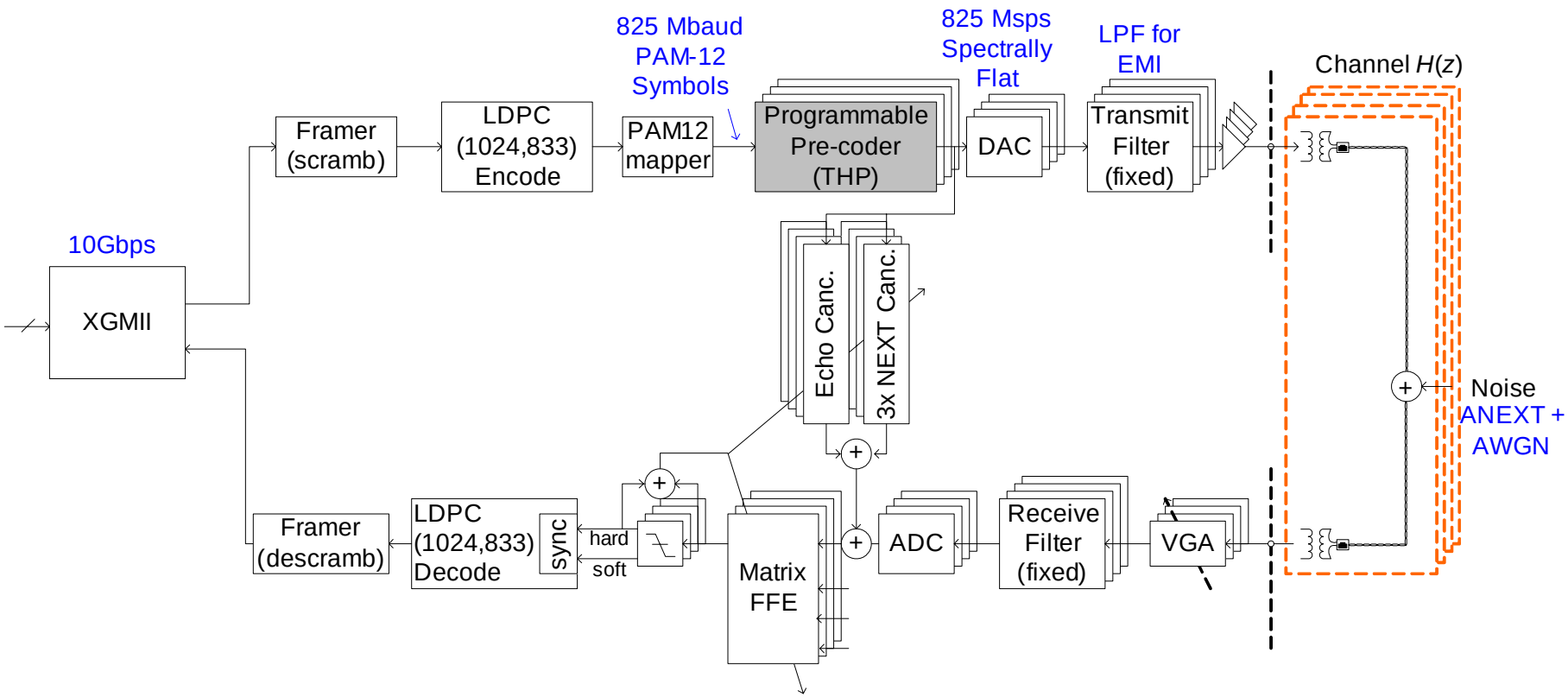
Projected EMI

- **EMI based on channel characterization measurements**
  - Ref: powell_1_0303.pdf Cat 6 + patch panel





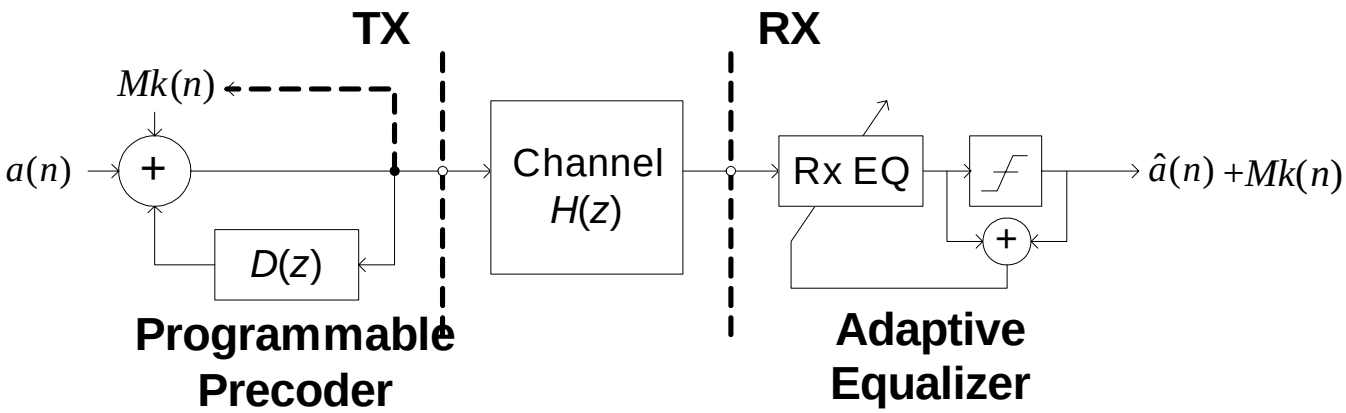
Precoder


825 Mbaud
PAM-12
Symbols
825 Msps
Spectrally
Flat
LPF for
EMI
Channel H(z)
10Gbps
XGMII
Framer
(scramb)
LDPC
(1024,833)
Encode
PAM12
mapper
Programmable
Pre-coder
(THP)
DAC
Transmit
Filter
(fixed)
Echo Canc.
3x NEXT Canc.
Noise
ANEXT +
AWGN
Framer
(descramb)
LDPC
(1024,833)
Decode
sync
hard
soft
Matrix
FFE
ADC
Receive
Filter
(fixed)
VGA

Precoder Details

Ref: powell_1_0304.pdf, ungerboeck_1_0704.pdf

- **Precoder coefficients chosen at start-up to approximately match channel response**
  - Either precomputed/stored or computed at start-up
  - Programmable feedback filter *D*(*z*)



- **Adaptive Rx equalizer removes residual ISI due to channel mismatch**
  - Vendor dependent – precoding does not constrain equalizer type (FFE, DFE, etc)

ARMA Precoder Polynomial

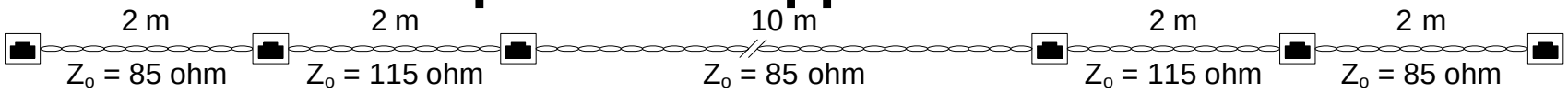
- **Coefficients of precoder (or DFE) feedback filter are given by the channel SNR function**
  - "Channel" includes insertion loss, noise, filters, transformers, etc
  - Twisted pair (TP) channels have very long impulse response tails
- **Pole-zero models approximate TP channels with a much smaller number of parameters**
  - Recursive "Tail cancellers" commonly used to reduce DFE complexity

Al-Dhahir, Sayed, Cioffi, "Stable Pole-Zero Modeling of Long FIR Filters with Application to the MMSE-DFE," IEEE Trans. On Comm., May 1997

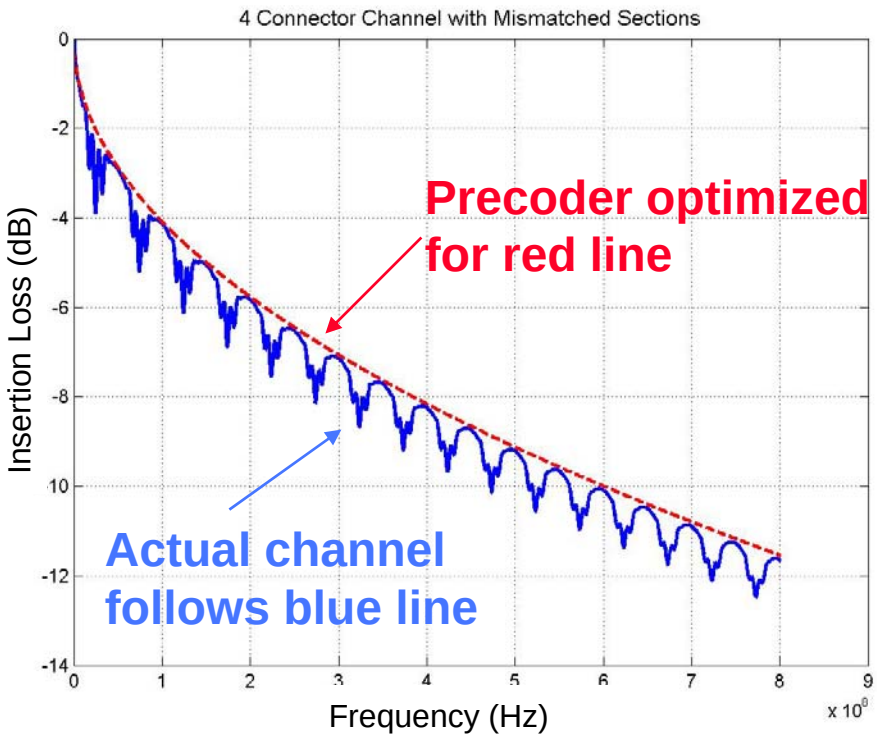
- **A 3-pole, 3-zero channel model accurately describes the worst case 100m cable model** (powell_1_0304.pdf, ungerboeck_1_0704.pdf)
  - Specify precoder as ARMA(3,3) coefficients
  - Precoder can be implemented as either FIR or IIR

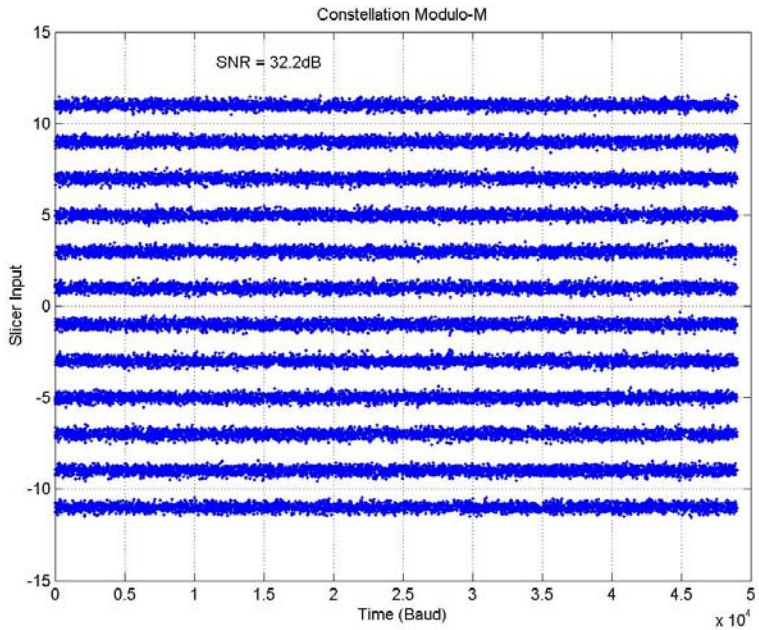
Far End Echo Effects

- **Impedance mismatches can cause insertion loss to deviate from exponential approximation**



Multi-Segment Channel with 15% Mismatch

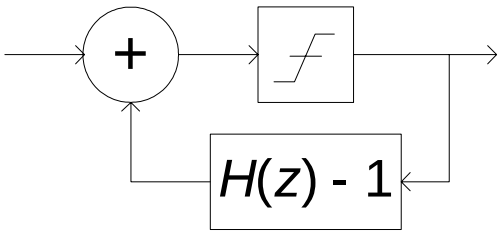




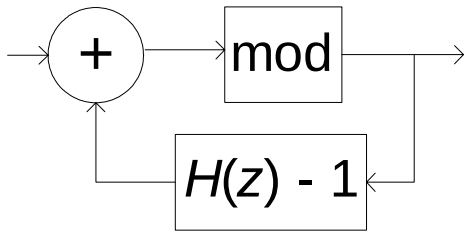
SNR > 32dB (simulated)

Implementing THP at High Speed

- **High speed THP implementation issues similar to high speed DFE implementation issues**
  - Both equalizers have identical feedback filters + a non-linear operator in the loop
  - Precoder has advantage of access to non-causal data



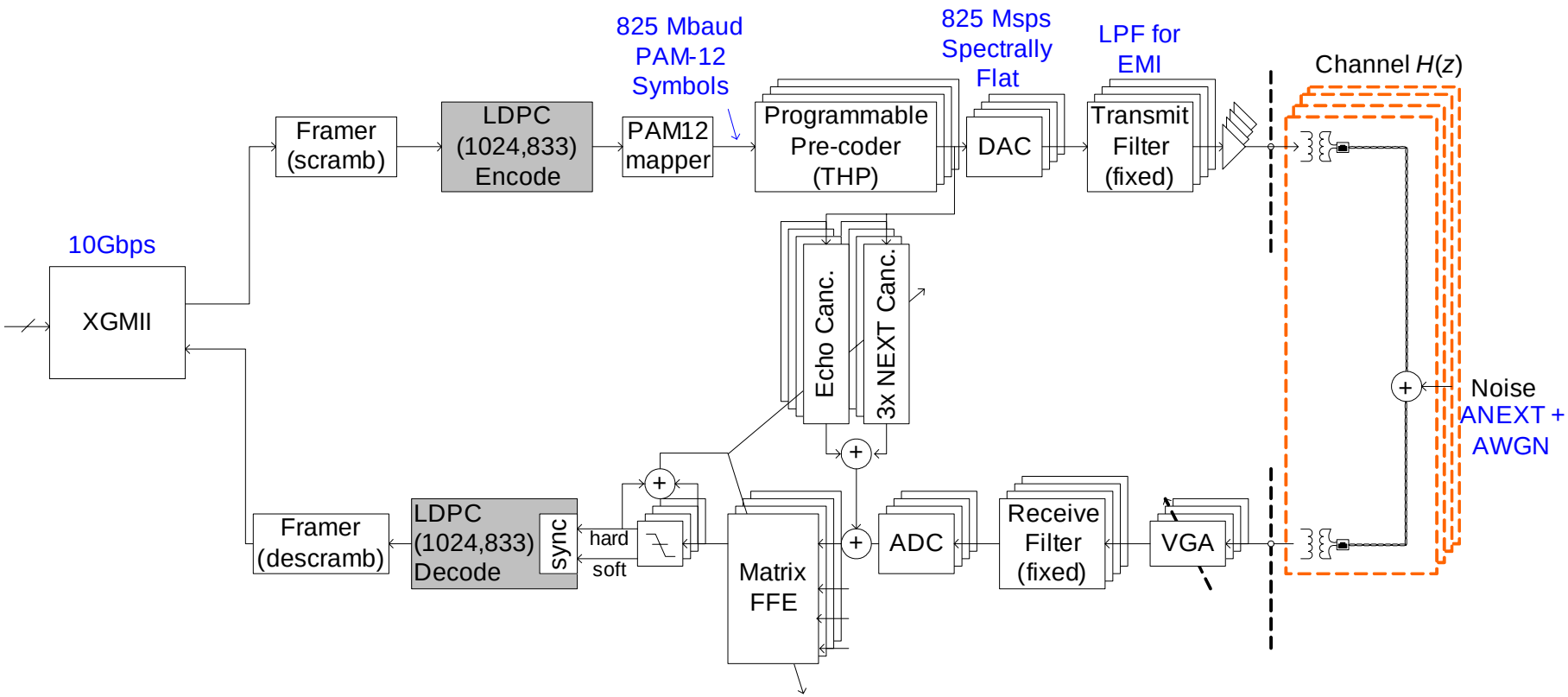
DFE



Precoder

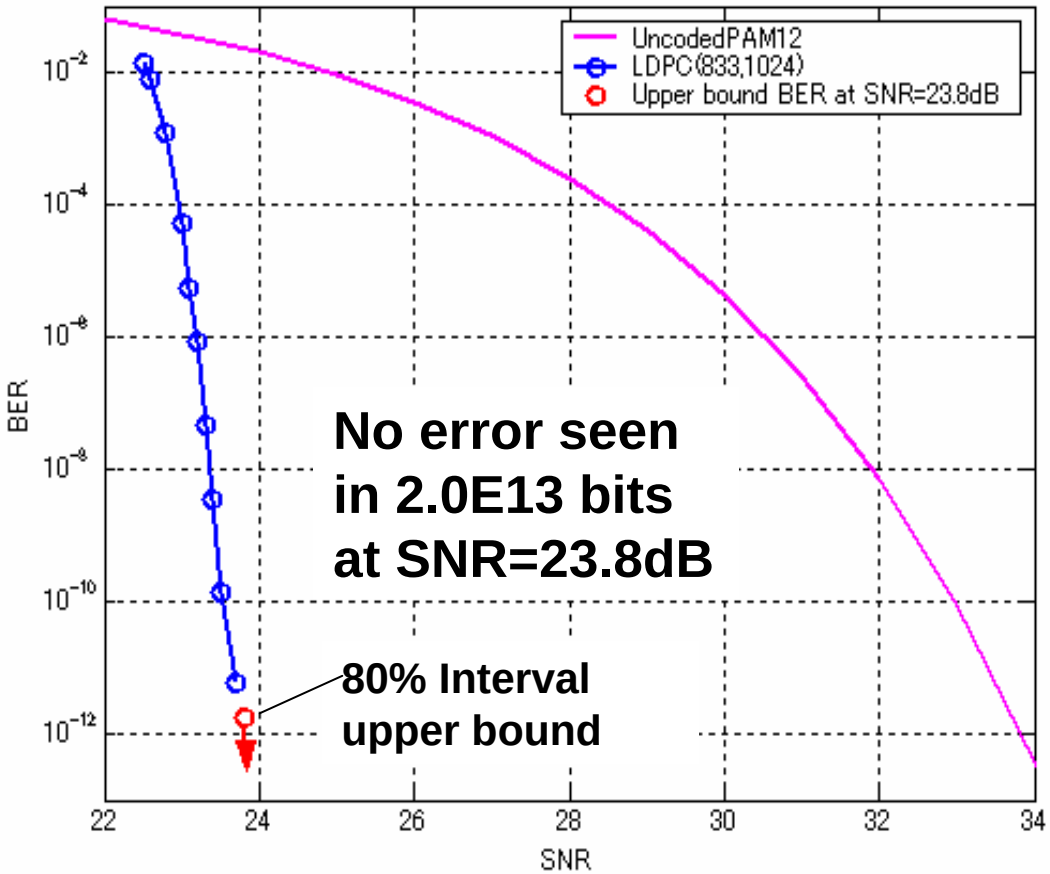
- **Possible approaches:**
  - Simplify coefficient multipliers (see ungerboeck_1_0704.pdf)
  - Prediction techniques
  - Look-ahead techniques
  - Block processing techniques

Channel Code



LDPC(1024,833) Performance*

***Source: AIST/NEC Electronics (see seki_1_0704.pdf for details)**



Average number of error bits per error block =24.0

FER=BER/24.0*1792

UB: upper bound BER with 80% confidence
NF: Number of Frame simulated =2.0E13/1792
f(x) : The probability of error free at x FER

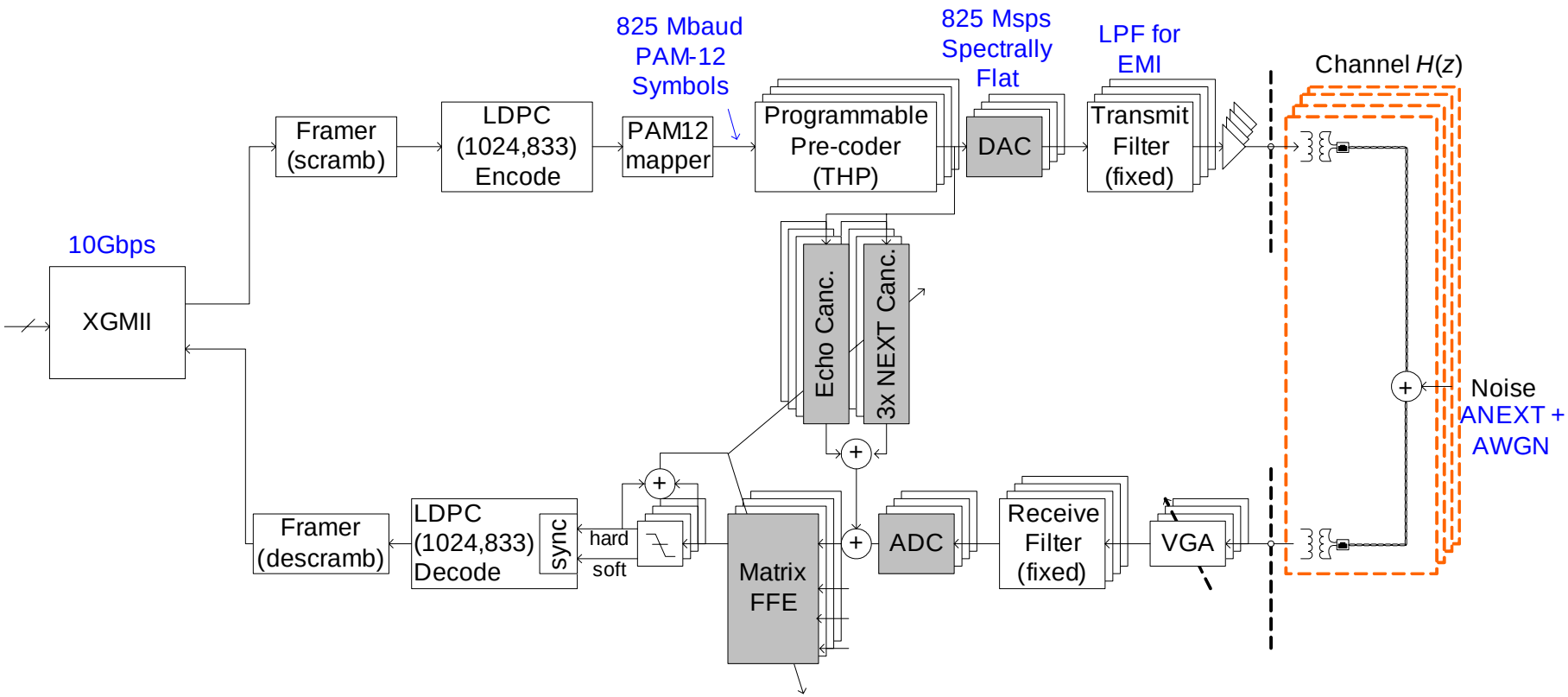
$$\frac{\int_0^{(UB/24*1792)} f(x)dx}{\int_0^1 f(x)dx} = 0.8$$

$$f(x) = \exp(NF*\log(1-x))$$

- **No error floor observed up to 1E-12 BER**
- **Required SNR=23.8dB for 1E-12 BER**

R=3.13 bits/sym
Coding Gain = 7.3 dB

Cancellers, FFE, ADC/DAC

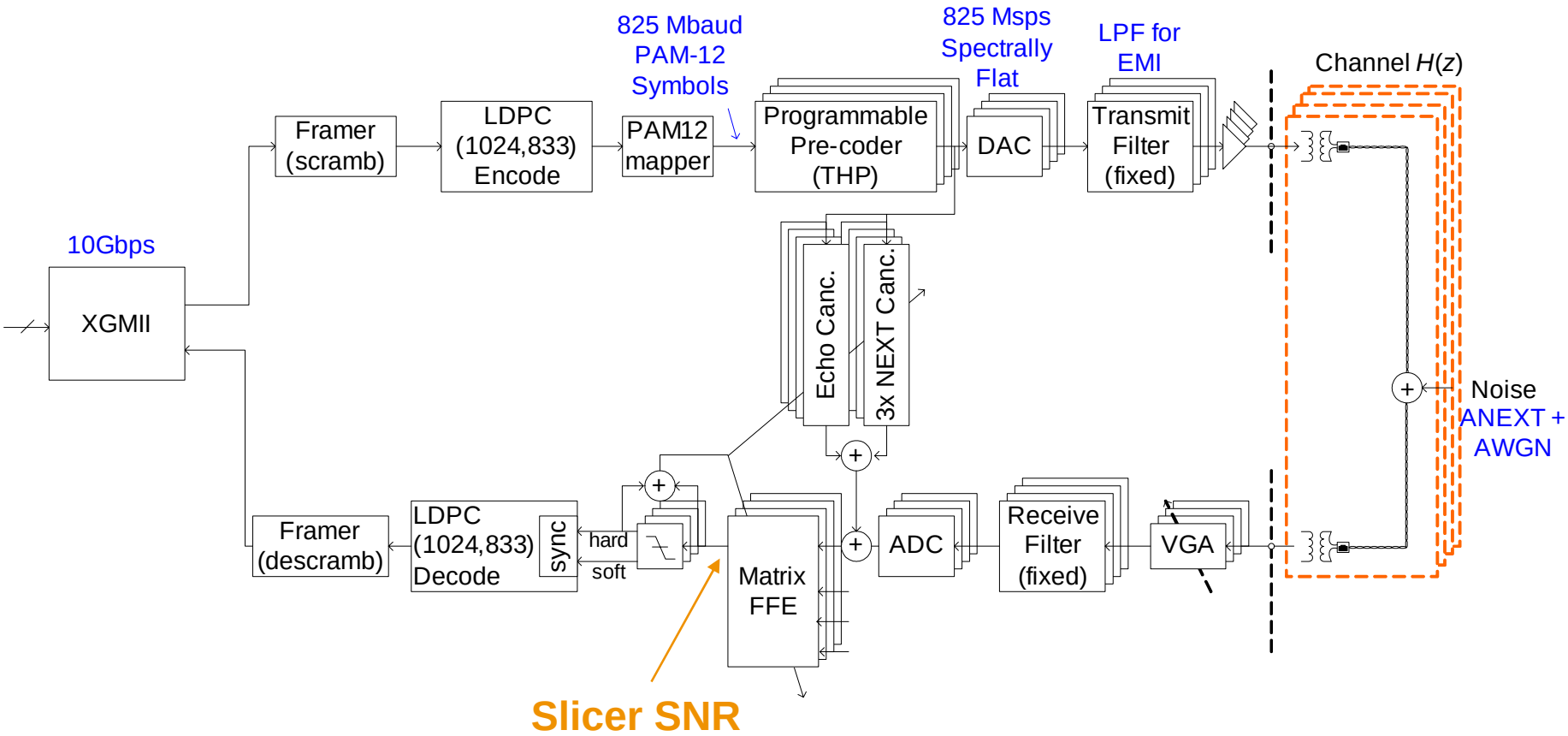


Example System Requirements

Echo Suppression	55 dB
NEXT Suppression	40 dB
FEXT Suppression	25 dB
ADC Resolution*	10 bits
DAC Resolution	10 bits
Timing Jitter	2.5 ps rms
Precoding Function	ARMA (3,3)
FFE span	64 taps

* Assume ideal with 15dB analog echo cancellation
(see takatori_1_0304.pdf for feasibility)

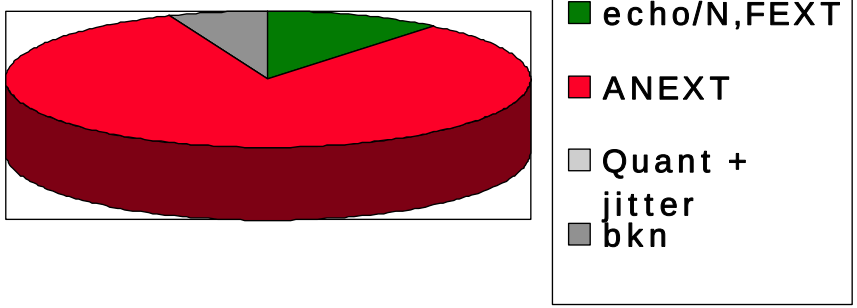
Overall Performance



Cable Model 3 Slicer SNR

100m "Cat 6e" PAM-12 Salz Solution

Optimum slicer SNR assuming ideal analog WMF + ideally sampled baud spaced equalizer



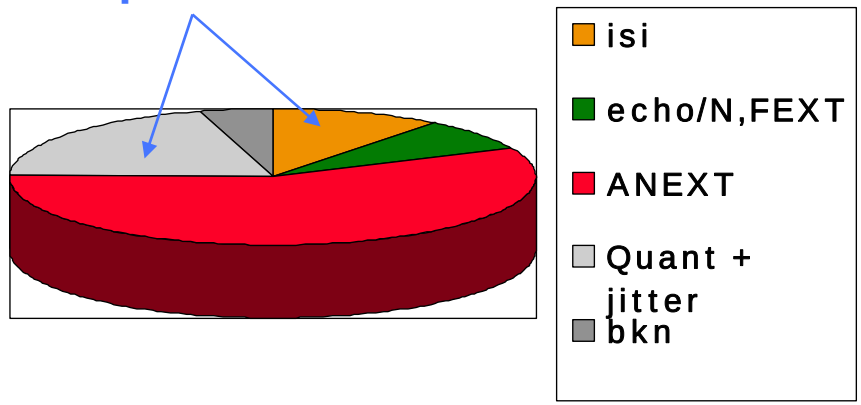
Total Slicer SNR = 28.9dB

- **Required SNR = 23.8dB**

∴ **5.1dB design margin**

100m "Cat 6e" PAM-12 MMSE Solution

"Salz Analysis" ignores these components



Total Slicer SNR = 26.0dB

Note: isi+quant+jitter+bkn ~ -140dBm/Hz

Example System Performance

Salz Link Margin*		5.1 dB
Noise Immunity Target		3 V/m 80MHz-1GHz
Emissions		Class A Demonstratable
Latency		1us
Complexity Metric**		4M-7M gates
Power: (90nm)	analog	4.5W-9W
	digital	3.5W-7W
	total	8W-16W

Represents range for all contributing PHY vendors

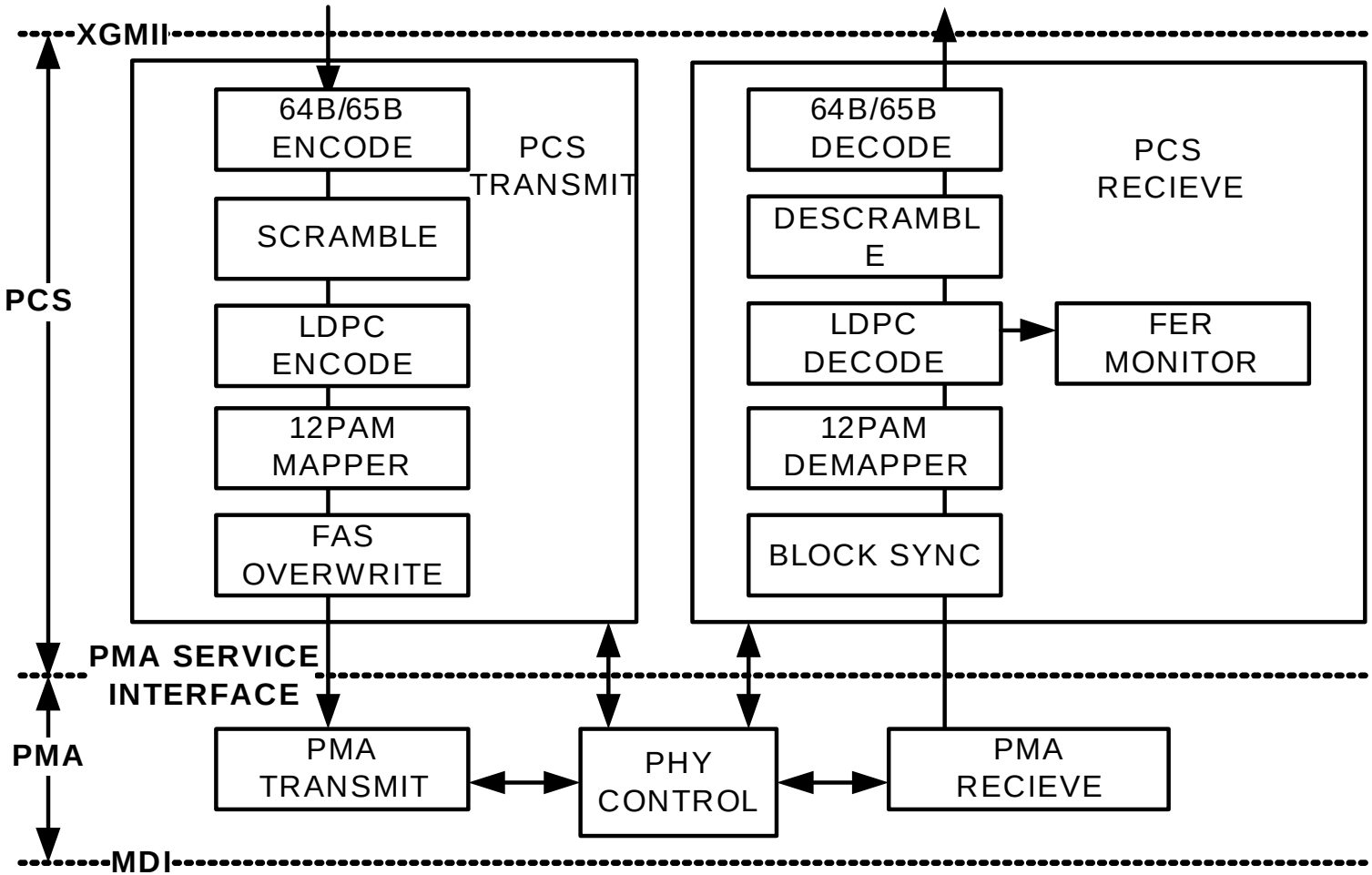
* Cable model 3 Salz equations

** Gate count assuming all processing at F_{baud}

Framing Details

Jose Tellado, Teranetics

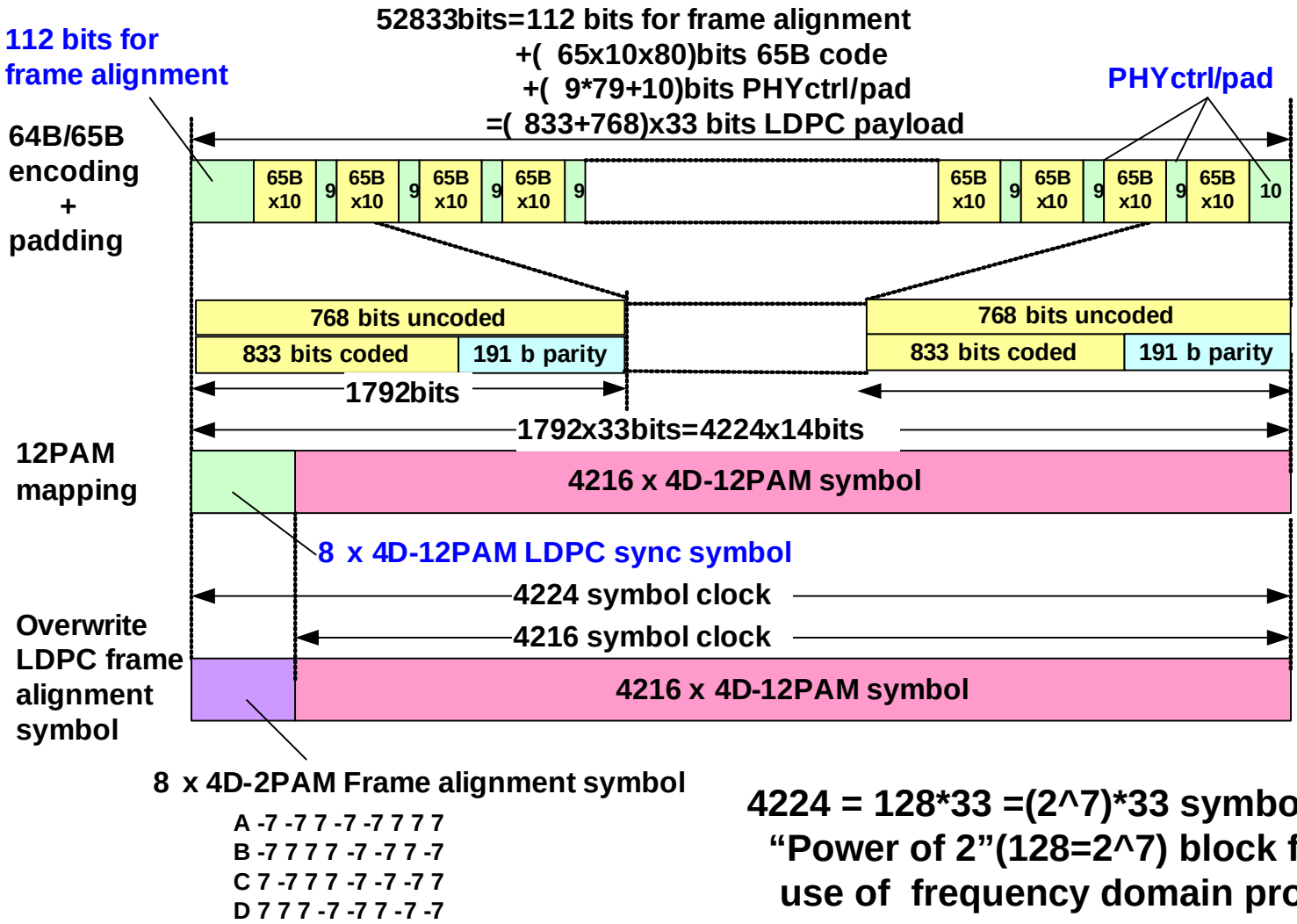
PCS Functional Block



Framing and Control

- **64B/65B Code (based on 64B/66B Clause 49)**
  - Aligned with LDPC Frame
    - Automatic 64B/65B code sync after required LDPC frame sync
  - Eliminates one sync bit (unnecessary with LDPC frame sync)
    - data code “01” -> “0”
    - control code “10” -> “1”
- **LDPC frame payload : 800 65B blocks + 721 PHYcontrol/padbits +112 pad bits for LDPC frame alignment**
- **PHY control/padbits open for PHY status, THP updates, CRC,…**
- **LDPC subunit : 1792bits =128 4D PAM12 symbol**
- **LDPC symbol frame : 33 LDPC subunits**
- **Symbol rate: 10Gx(1792x33)/(64x800)/14 = 825MHz**
  - Symbol rate of 825MHz is easy to generate from standard oscillators in the range 25-170MHz (e.g. 25, 100, 125, 150MHz) with a N/M PLL multiplication

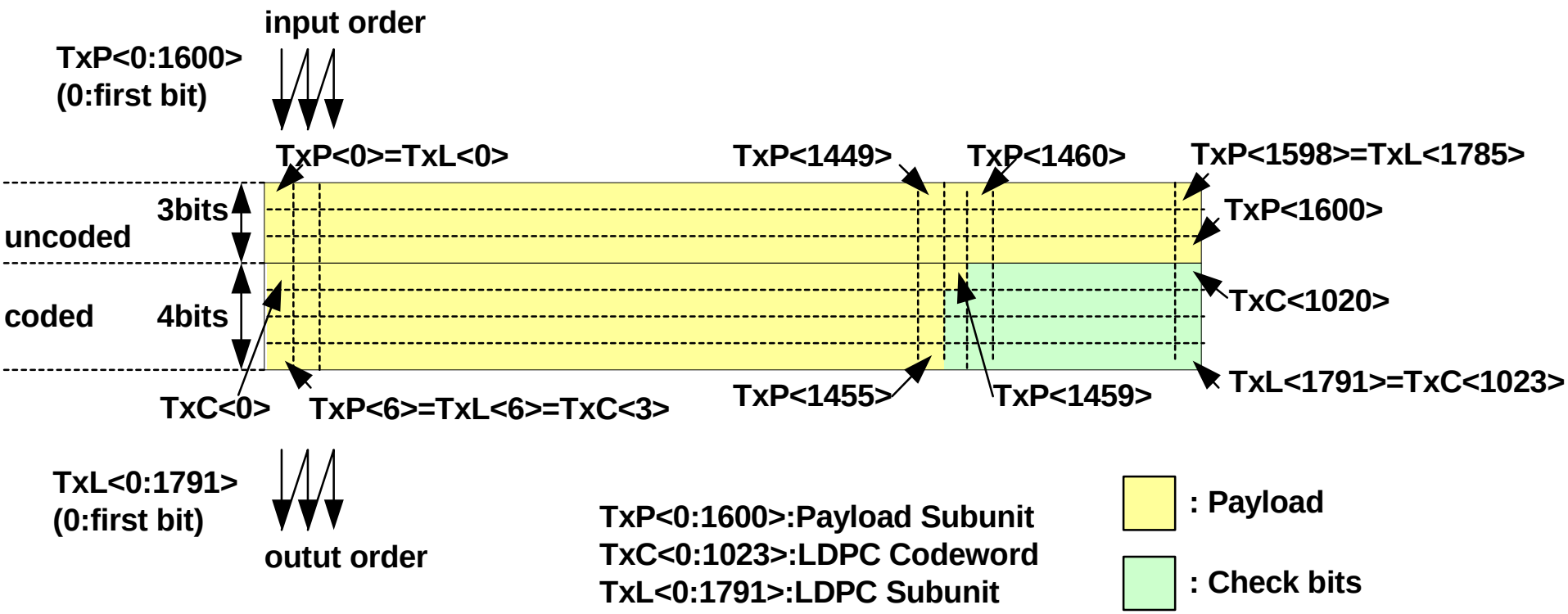
Framing and Control (cont')



4224 = 128*33 =(2^7)*33 symbol clock
"Power of 2"(128=2^7) block facilitates use of frequency domain processing.

LDPC Subunit Systematic Encoding

LDPC Encoding (systematic)



LDPC to PAM12 mapping

- **Based on www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf**
  - PAM12 mapping achieved with simple tables below
    - TA=X1*8+X2 (12PAM mapping on wire A)
    - TB=Y1*8+Y2 (mapping wire B)
    - TC,TD shall use tx_data_ group<7:13> in the same way as TA,TB

Tx_data_group <0:2>	X1	Y1
000	-1	-1
001	-1	0
011	-1	1
010	0	1
110	1	1
111	1	0
101	1	-1
100	0	-1

Tx_data_group <3:4>	X2
00	-3
01	-1
11	1
10	3

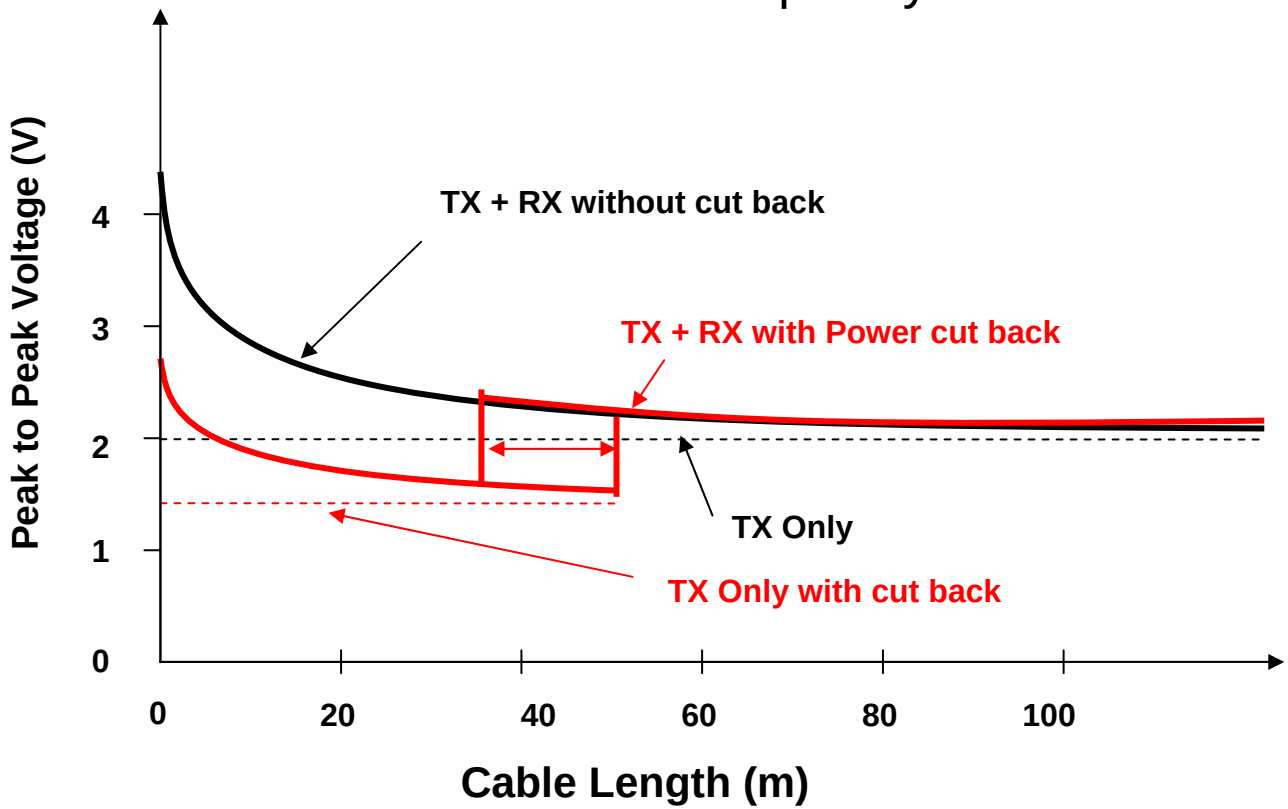
Tx_data_group <5:6>	Y2
00	-3
01	-1
11	1
10	3

Power Backoff

Hiroshi Takatori, Keyeye

Power Cut Back

Benefit: Reduction of A-NEXT
Power and Complexity Reduction



3dB cut back at about 35~55m as an example

Noise Margin
Cat 6e (7dB Coding Gain)