Performance evaluation of low latency LDPC code

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Outline

- Recap of LDPC codes
- Low latency LDPC code parameters
- Performance simulation conditions
- Performance simulation results
- Summary

Recap

- 4D-PAM8 LDPC proposal by Rao *1
  - 1GHz 8PAM
  - Tomlinson-Harashima Pre-coding
  - 12dB coset partitioning
  - LDPC(1723,2048)

- System vendors pointed out that low latency increases the market potential. *2

- Low latency and low symbol rate LDPC proposal by Dariush *3
  - 800MHz 12PAM
  - 160nsec intrinsic latency
  - LDPC(781,1024)

*1 www.ieee802.org/3/an/public/nov03/rao_1_1103.pdf
*2 www.ieee802.org/3/an/public/mar04/muller_1_0304.pdf
*3 www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf

Recap (cont')

- **Modification to low latency LDPC code *1**
  LDPC(845,1024) has comparable performance to LDPC(781,1024) with lower complexity

- **Low latency code has a doubt of BER slope change *2**
  Longer simulation must be necessary to estimate the performance at 1E-12 BER

***1 www.ieee802.org/3/an/public/may/seki_1_0304.pdf**
***2 www.ieee802.org/3/an/public/nov03/rao_1_0504.pdf**

Purpose :
Down to 1E-12 BER simulation to confirm error floor free

Low latency LDPC codes

	New candidate code	Proposed code In May meeting
Code	LDPC(833,1024)	LDPC(845,1024)
Mapping	PAM12	PAM12
Information bits/Symbol	3.13bits	3.15bits
Shannon bound	18.8dB	18.9dB
Intrinsic Latency	160nsec	160nsec
Hamming Distance	>=12	>=10
Symbol rate (w/o packet overhead)	799MHz	793MHz

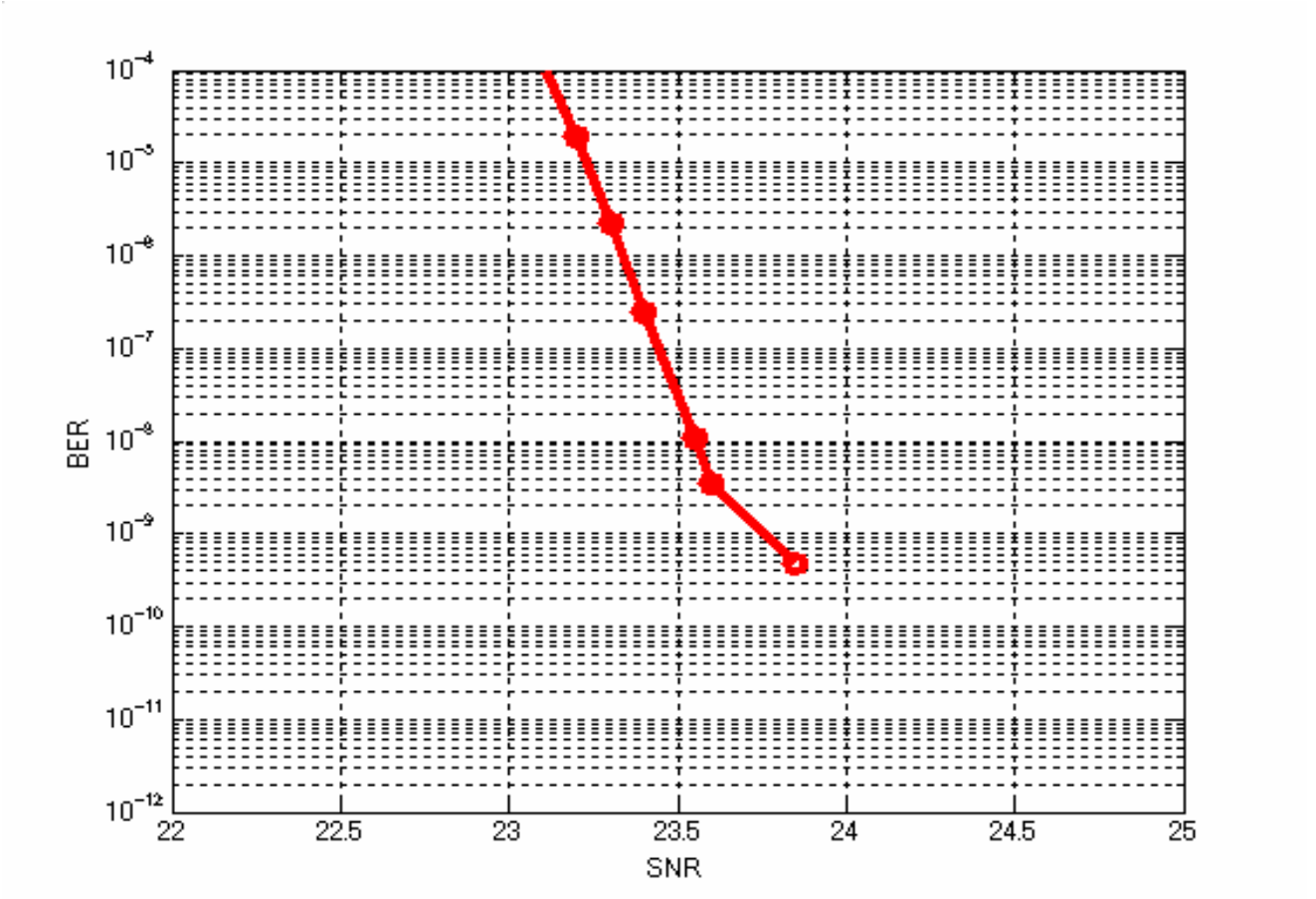
Simulation conditions

- Floating points design
- 10 times Iteration
- Standard SPA
- Concurrent decoding schedule

Configuration of the computer cluster

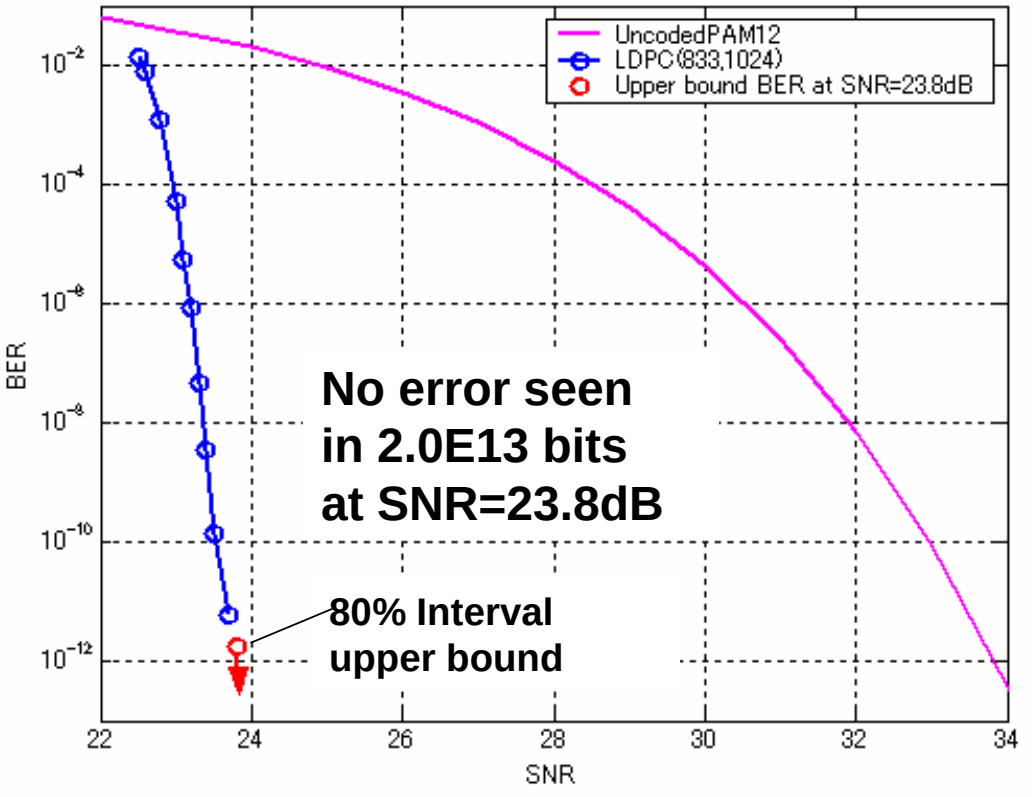
- AIST Super Cluster (ASC)
- 256 CPUs
- Intel Xeon 3.06GHz
- 2 weeks calculation for 2.0E13 simulating bits

LDPC(845,1024) Performance



Has a BER slope change at unacceptable BER

LDPC(833,1024) Performance



Average number of error bits per error blocks =24.0

FER=BER/24.0*1792

UB: UB: upper bound BER with 80% confidence
NF: The number of Frame =2.0E13/1792
f(x) : The probability of error free at x FER

$$\frac{\int_0^{(UB/24*1792)} f(x)dx}{\int_0^1 f(x)dx} = 0.8$$

$$f(x) = \exp(NF * \log(1-x))$$

- **No error floor observed up to 1E-12 BER**
- **Required SNR=23.8dB for 1E-12 BER**

Summary

LDPC(845,1024)

- **Has a BER slope change at unacceptable BER**

LDPC(833,1024)

- **Comparable performance to LDPC(1723,2048)**
  - **Required SNR=23.8dB for 1E-12 BER**
  - **Gap to Shannon capacity = 5dB**
  - **No error floor**
- **Low intrinsic latency of 160nsec**