LDPC-PAM12 PHY proposal for 10GBase-T

P802.3an July '04
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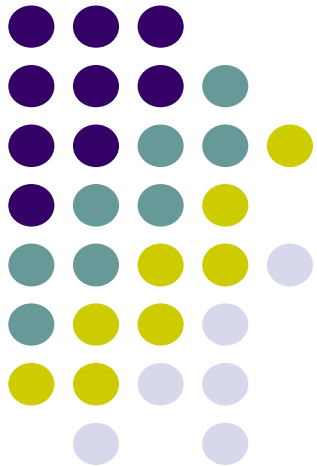

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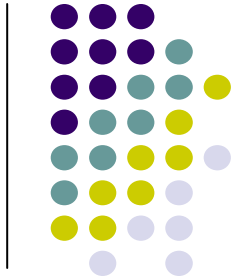

Supporters

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Overview

- Main parameters of PHY proposal
  - PAM
  - LDPC
  - THP
  - Start-up and Framing
- Performance
  - Margin or Noise Immunity
  - Transmitter and Receiver assumptions
- Implementation

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Main parameters of PHY proposal

- FEC code: LDPC(833,1024)
- Modulation: 12PAM.
- Symbol rate: 825MHz
- Equalization: Tomlinson-Harashima precoding (THP)
- LDPC Framing
- MAC I/F, MAC/PHY Control

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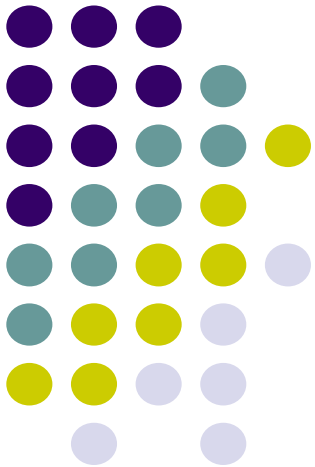
LDPC



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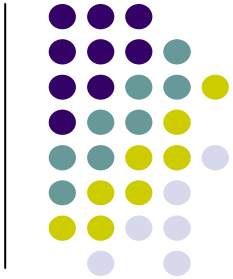

LDPC Parameters

Code	LDPC(833,1024) PAM12 mapping	LDPC(1723,2048) PAM12 mapping
Information bits/Symbol	3.13bits	3.18bits
Required SNR for BER=1E-12	23.8dB (*1)	~24dB (*2)
Shannon bound	18.8dB	19.1dB
Gap to capacity @ BER =1E-12	5dB	~5dB
Intrinsic Latency	160nsec	320nsec
Symbol rate (w/o packet overhead)	799MHz	786MHz
Hamming Distance	12	8

*1 : Ref. http://www.ieee802.org/3/an/public/jul04/seki_1_0704.pdf

*2 : Estimated based on Rao's proposal and re-mapping the code from PAM8 to PAM12

LDPC(833,1024) has comparable performance to LDPC(1723,2048) with lower latency.

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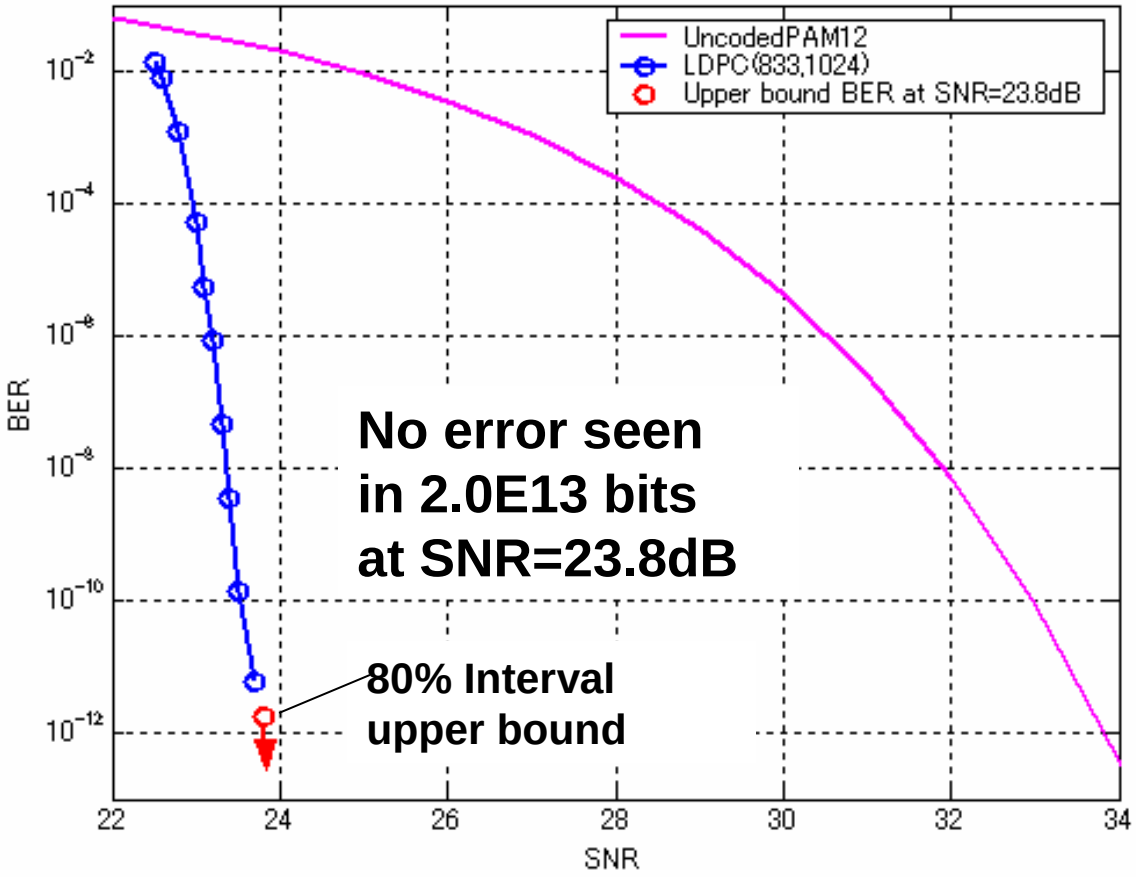
LDPC(833,1024) Performance



- No error floor observed up to 1E-12 BER
- Required SNR=23.8dB for 1E-12 BER

No error seen in 2.0E13 bits at SNR=23.8dB

Average number of error bits per error blocks =24.0

FER=BER/24.0*1792

UB: Upper Bound BER with 80% confidence
NF: Number of Frames =2.0E13/1792
f(x) : The probability of error free at x FER

$$\frac{\int_0^{(UB/24*1792)} f(x)dx}{\int_0^1 f(x)dx} = 0.8$$

$$f(x) = \exp(NF * \log(1-x))$$

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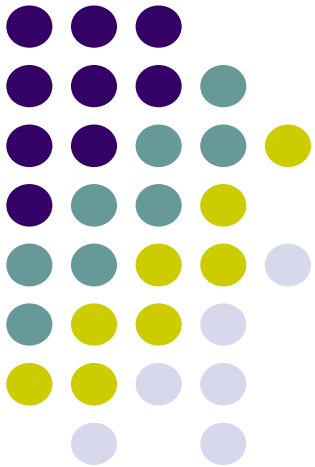
THP



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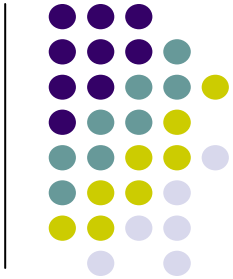

Benefits of THP

1. Permits strong block code such as LDPC by decoupling channel equalization from channel coding

   Strong block code is necessary to get sufficient margin for implementation losses and reliable performance

2. Error propagation free

   Avoids sub-optimal performance of DFE equalizer

3. Removes DFSE timing loop

   Simplifies timing closure

Ref. http://www.ieee802.org/3/an/public/mar04/powell_1_0504.pdf
Scott Powell et al, “Multi-Vendor Agreement on Precoder Proposal”

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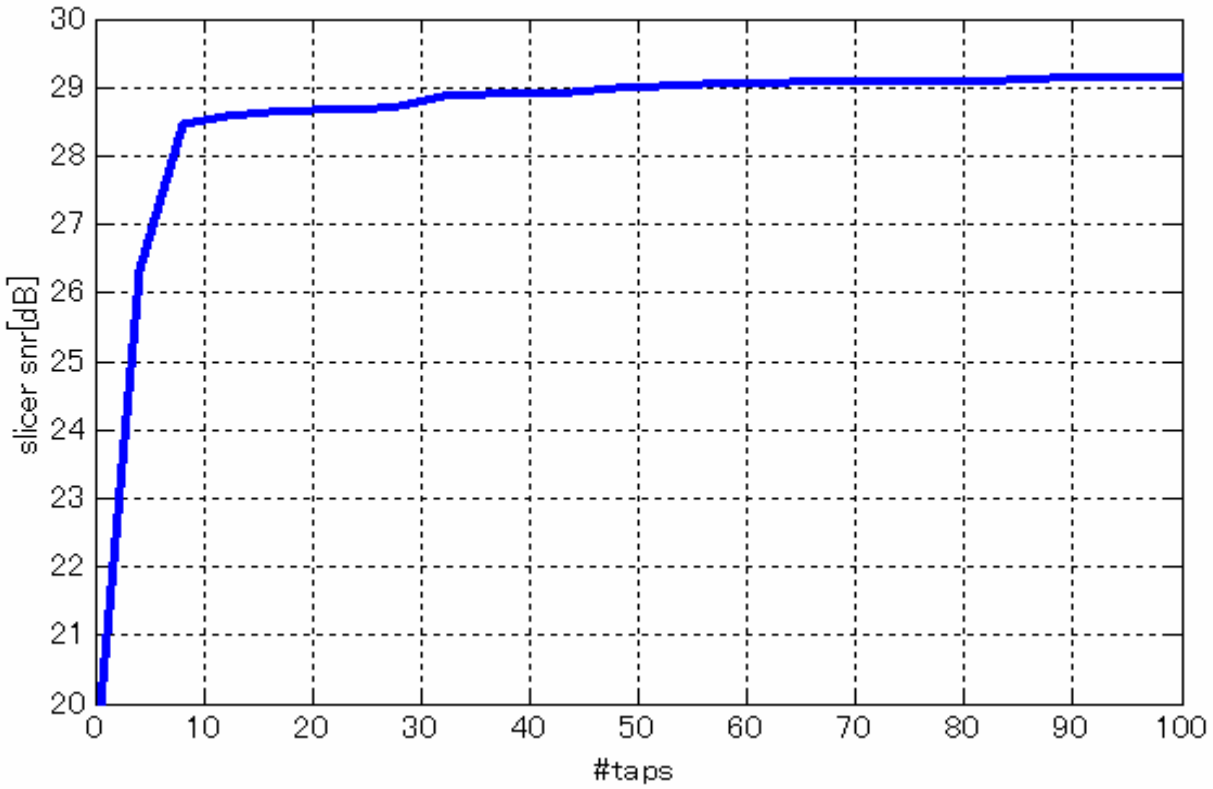
Performance relative to num. of coef.



IL Model :
P802.3 Task Force Material
Measured Class E model
ANEXT :
64.5 - 10.0*log10(F/100)
(F < 100MHz)
64.5 - 15.0*log10(F/100)
(F >= 100MHz)
BGN : -150dBm/HZ
Without other impairments
FFE : 64 taps

20 coefs. are necessary to achieve enough performance over different channels

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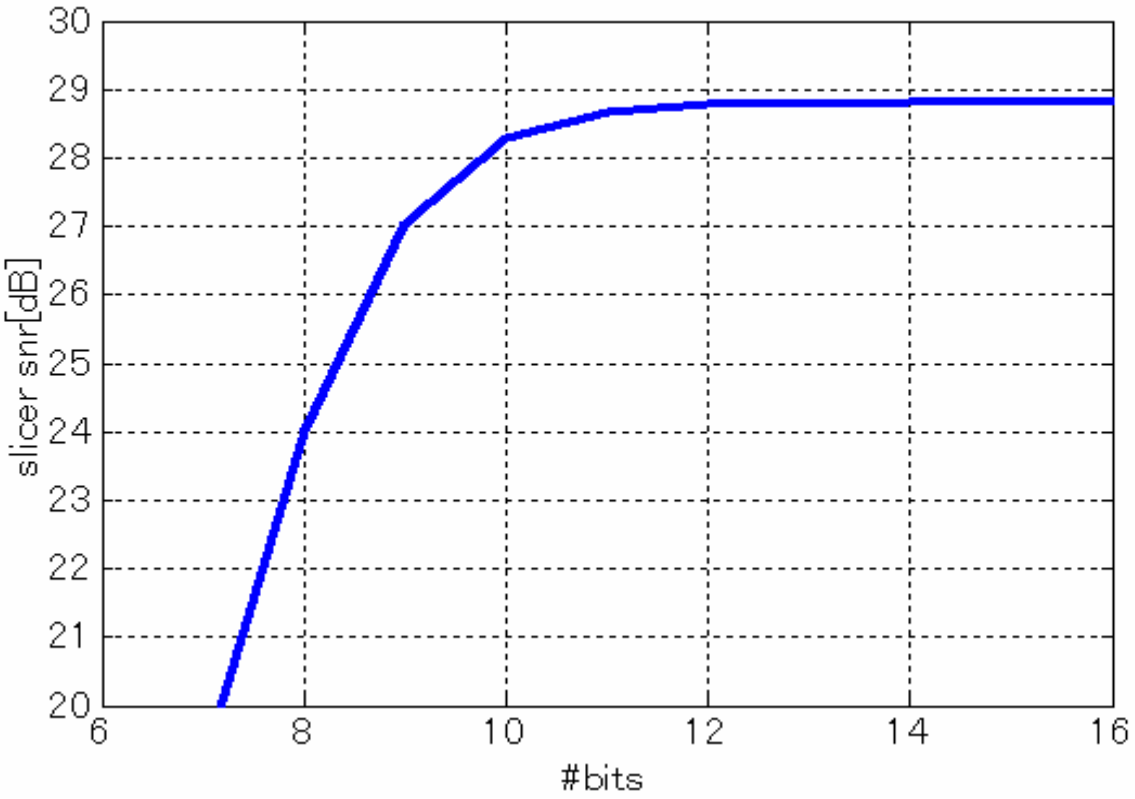
Performance relative to accuracy of coef.



IL Model :
P802.3 Task Force Material
Measured Class E model
ANEXT :
64.5 - 10.0*log10(F/100)
(F < 100MHz)
64.5 - 15.0*log10(F/100)
(F >= 100MHz)
BGN : -150dBm/HZ
Tx Power : 10dBm(Flat PSD)
FFE : 64taps
DFE : 32taps

Bit lengths after the decimal point
= #bits – 3bit

THP coefficients requires 12 bits accuracy for negligible loss

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THP proposal summary

- **Number of coef. : 20 taps**
- **Bit accuracy of coef. : 12 bits**
- **Interoperability : HDSL2 approach**
  - **Coefficients determined at start up then fixed**

- **We have provided a mechanism for coefficient update which may be eliminated if we have sufficient data to prove that the update is not required**

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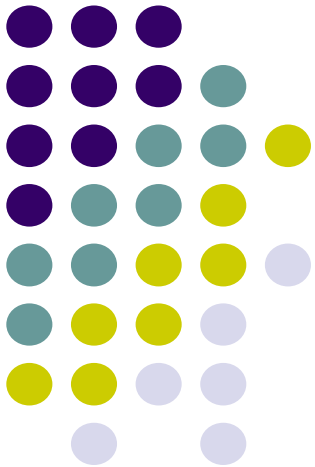
Startup protocol



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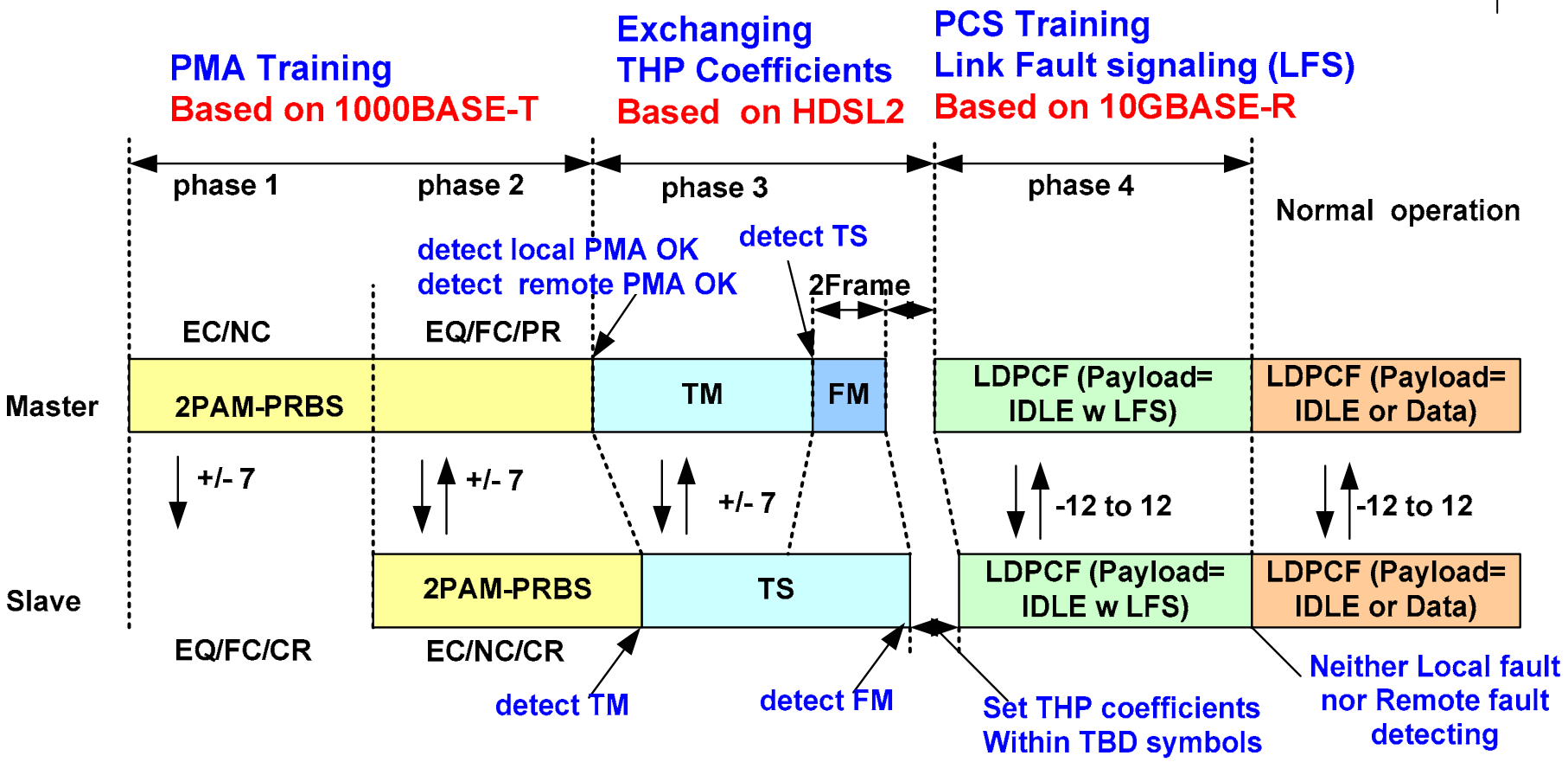
Startup sequence

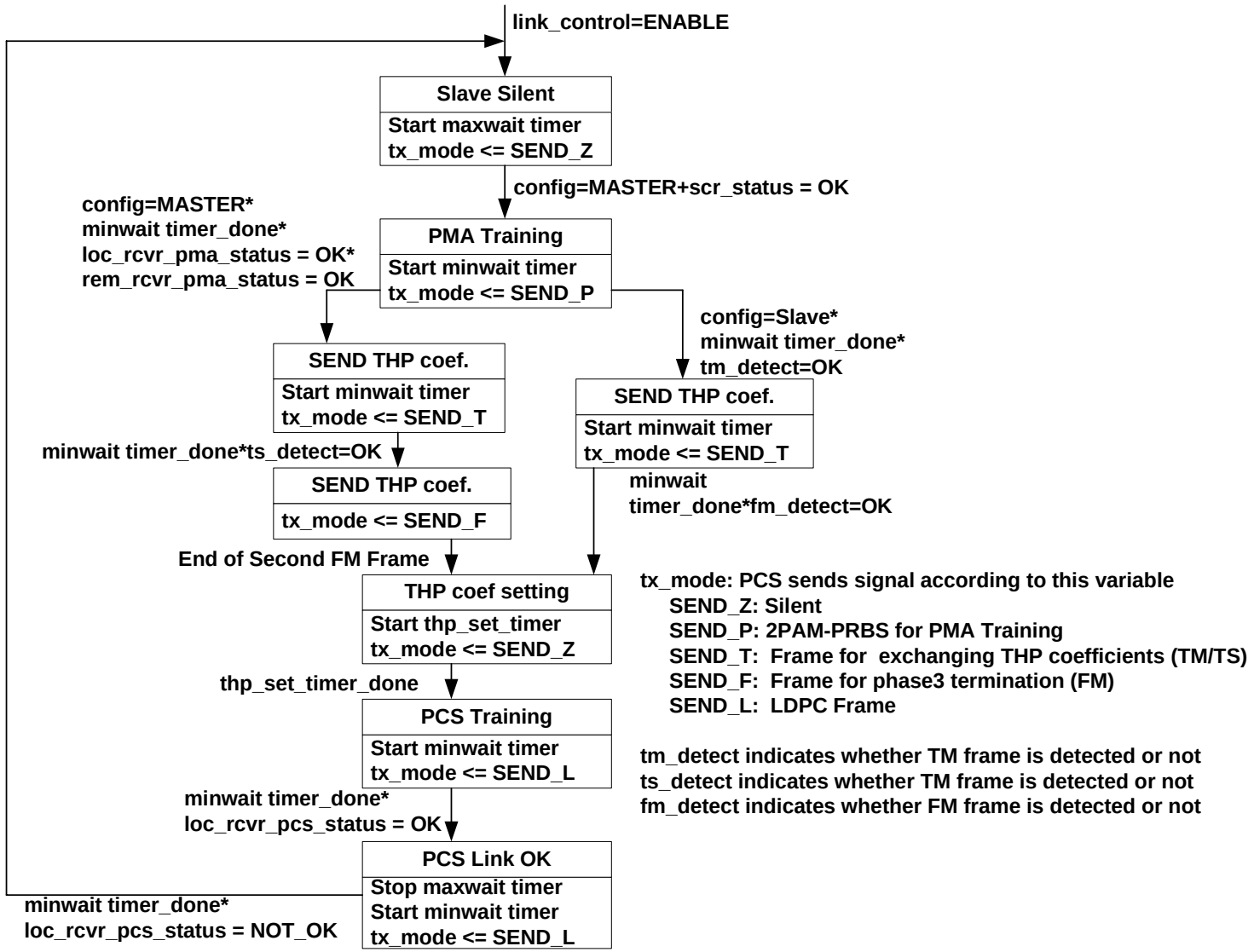


EC: Echo Cancellation
NC: NEXT Cancellation
EQ: Equalization
FC: FEXT Cancellation
CR: Clock recovery
PR: Phase recovery

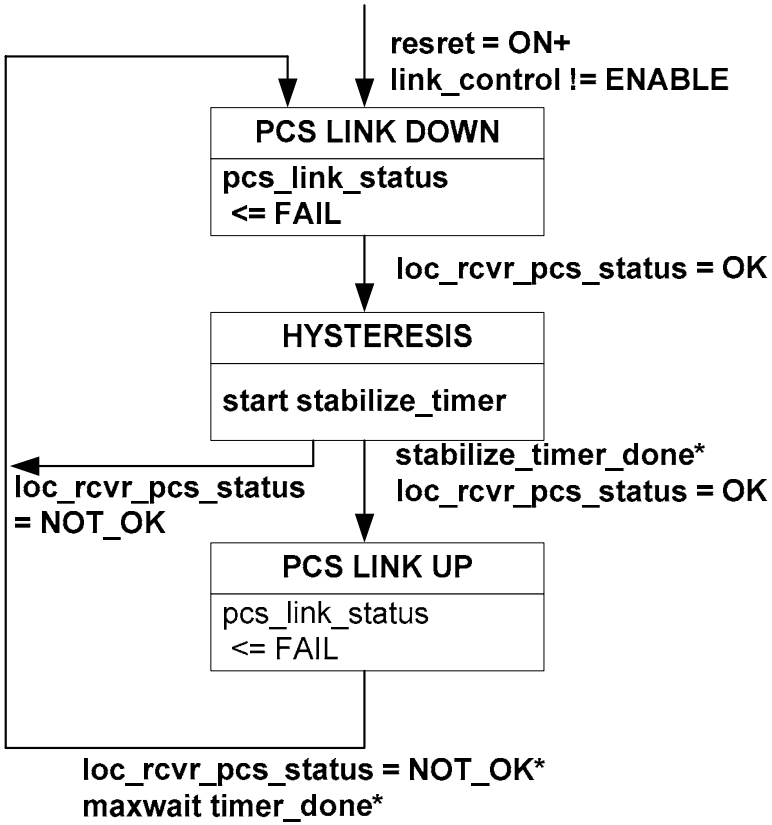
TM/TS : Frame for exchanging THP coefficients
FM : Frame for phase 3 termination
LDPCF : LDPC Frame

PCS Training includes LDPC sync and XAUI Lane alignments

PHY Control State Diagram



PCS Link Monitor State Diagram



The variable pcs_link_status and link_control are designated as link_control_(10GigT) and link_status_(10GigT), respectively, by Auto-negotiation Arbitration state diagram (Fig 28-16)

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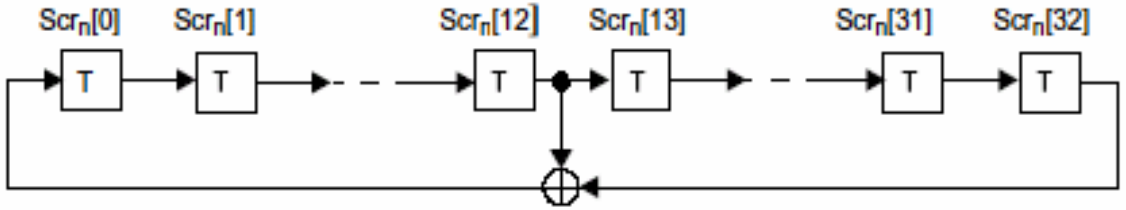
PMA Training signal

Objective:

- **Recover timing and adaptive filter coefficients**
- **Establish polarity correction, pair swap, pair deskew**

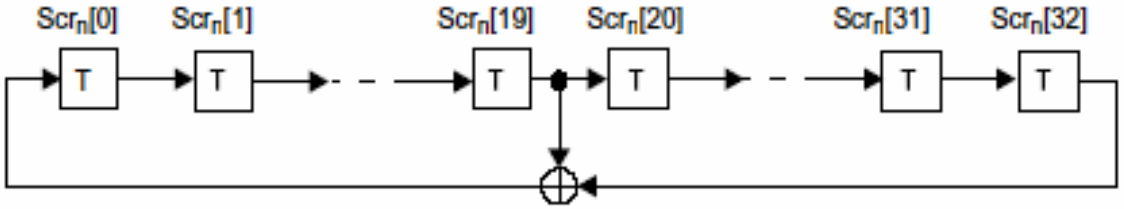
Side stream scrambler: (ref IEEE802.3 40.3.1.3.1)

Side-stream scrambler employed by the MASTER PHY



$$g_m(x)=1+x^{13}+x^{33}$$

Side-stream scrambler employed by the SLAVE PHY



$$g_s(x)=1+x^{20}+x^{33}$$

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PMA Training signal (cont')

Generation of bits Syn[3:0]

$$Sy_n[0] = Scr_n[0]$$

$$Sy_n[1] = g(Sy_n[0]) = Scr_n[3] \wedge Scr_n[8]$$

$$Sy_n[2] = g(Sy_n[1]) = Scr_n[6] \wedge Scr_n[16]$$

$$Sy_n[3] = \begin{cases} g(Sy_n[2]) = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24] & if\ (loc\_rcvr\_pma\_status = NG) \\ g(Sy_n[2]) \wedge Sy_n[0] = Scr_n[9] \wedge Scr_n[14] \wedge Scr_n[19] \wedge Scr_n[24] \wedge Scr_n[0] & else \end{cases}$$

$$g(x) = x^3 + x^8$$

Generation of Transmit symbol vector

$$A = \begin{cases} 7 & if\ (Sy_n[0] = 0) \\ -7 & else \end{cases} \qquad B = \begin{cases} 7 & if\ (Sy_n[1] = 0) \\ -7 & else \end{cases}$$

$$C = \begin{cases} 7 & if\ (Sy_n[2] = 0) \\ -7 & else \end{cases} \qquad D = \begin{cases} 7 & if\ (Sy_n[3] = 0) \\ -7 & else \end{cases}$$

This PMA training signal can meet objectives of polarity correction, pair swap and pair deskew.

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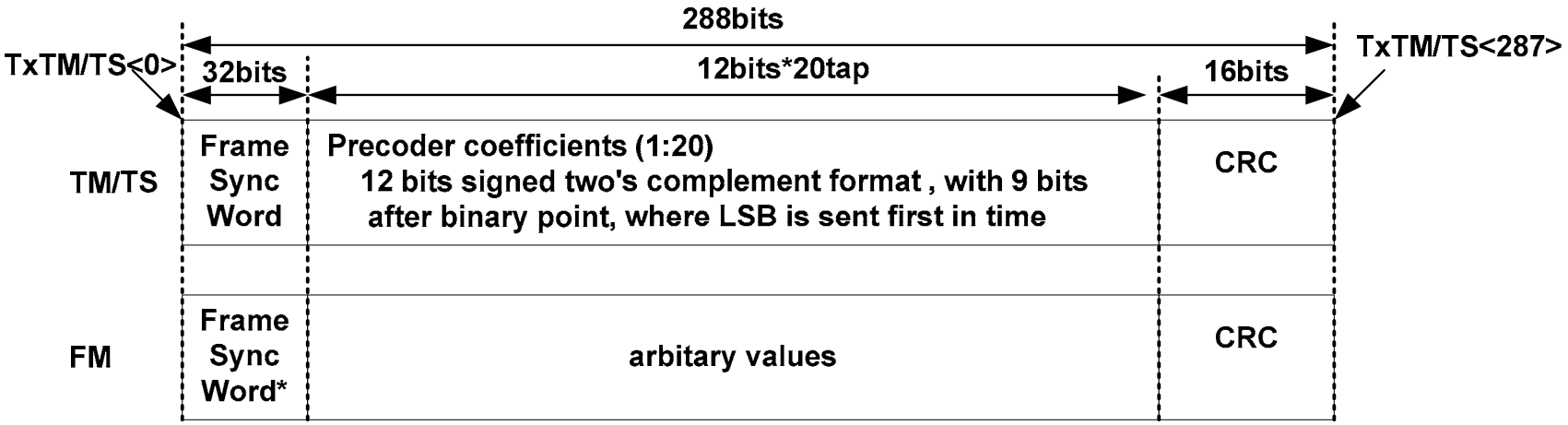
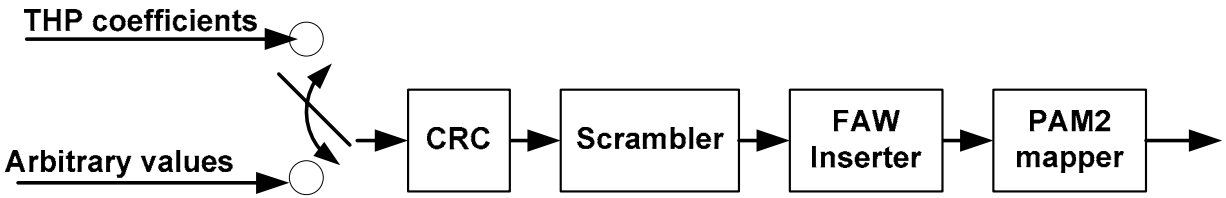
THP coefficient exchange frame



*The frame sync word of TM/TS Frame is "CA09F635"
The frame sync word of FM Frame shall be reversed in time



CRC generator polynomial : $g(x)=x^{16}+x^{12}+x^5+1$

Scrambler Polynomial : $g(x)=x^{23}+x^5+1$ **(Master)**

$g(x)=x^{23}+x^{18}+1$ **(Slave)**

Ref. ITU-T G.991.2 "Single-pair high-speed digital subscriber line (SHDSL)" Sec .7.2

PAM2 mapping

$$A=\begin{cases}7 \; if \; (TxTM < 4n >= 0)\\ -7 \; else\end{cases}$$

$$B=\begin{cases}7 \; if \; (TxTM < 4n+1 >= 0)\\ -7 \; else\end{cases}$$

$$C=\begin{cases}7 \; if \; (TxTM < 4n+2 >= 0)\\ -7 \; else\end{cases}$$

$$D=\begin{cases}7 \; if \; (TxTM < 4n+3 >= 0)\\ -7 \; else\end{cases}$$

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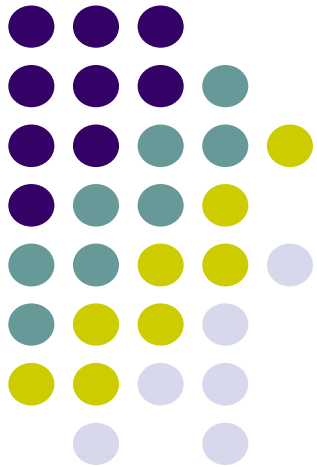
Framing



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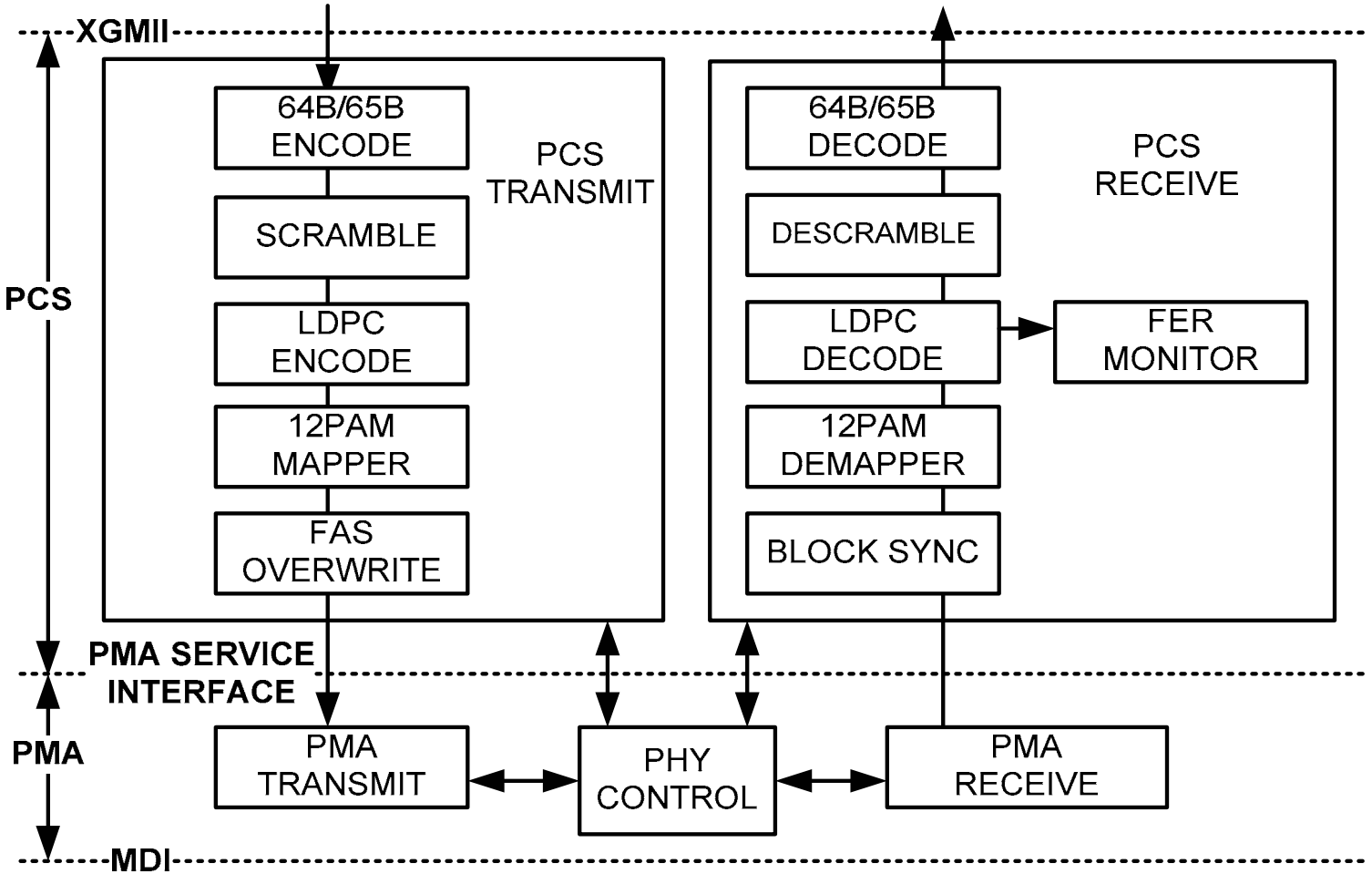
PCS Functional block



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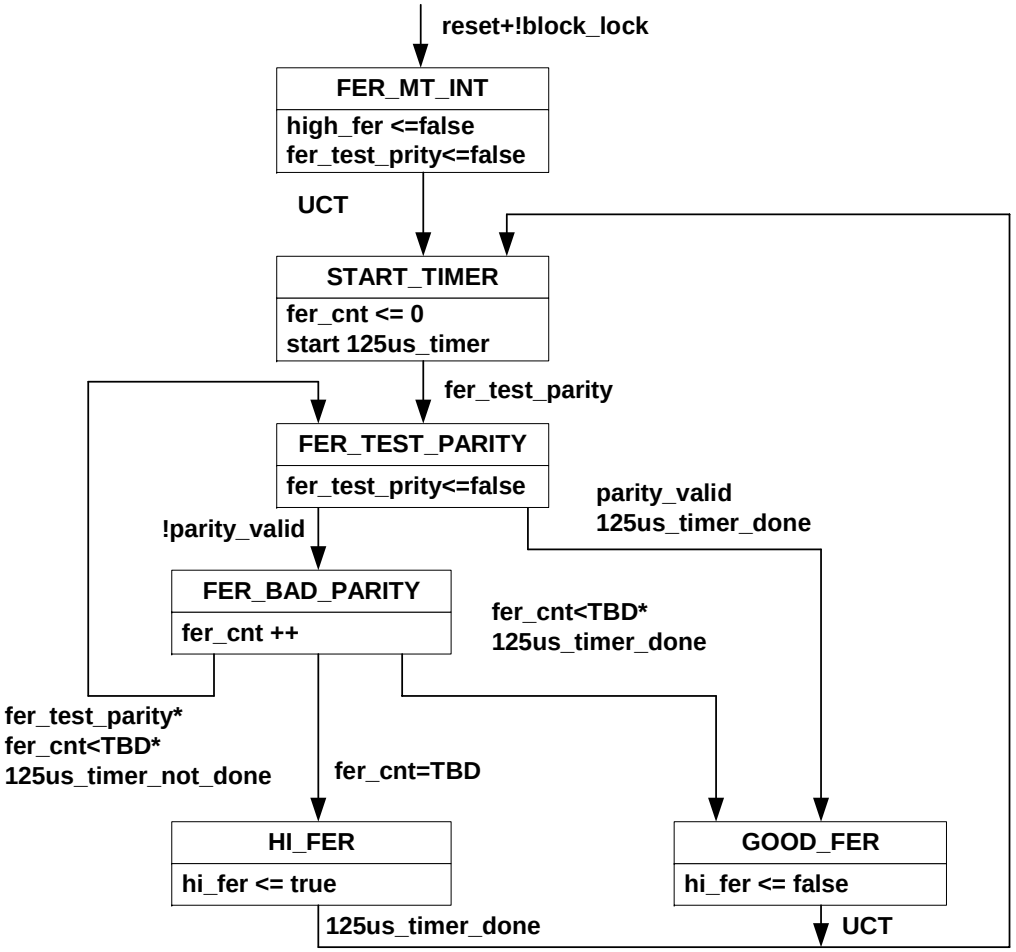
FER Monitor



Proposal:
FER monitor instead of BER monitor using 66B 2bits sync header

block_lock: Boollean variable that is set true when receiver aquires LDPC frame synchronization. The method used to detect frame synchronization is vendor dependent.
parity_valid:Boollean variable that is set true if recieved LDPC subunit has no parity check error.

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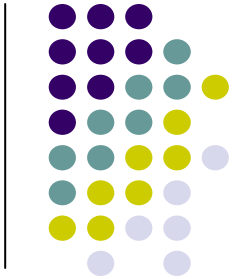

Framing and Control

- 64B/65B Code (based on 64B/66B Clause 49)
  - Aligned with LDPC Frame
    - Automatic 64B/65B code sync after required LDPC frame sync
  - Eliminates one sync bit (unnecessary with LDPC frame sync)
    - data code “01” -> “0”
    - control code “10” -> “1”
- LDPC frame payload : 800 65B blocks + 721 PHYcontrol/padbits +112 pad bits for LDPC frame alignment
- PHY control/padbits open for PHY status, THP updates, CRC,…
- LDPC subunit : 1792bits =128 4D PAM12 symbol
- LDPC symbol frame : 33 LDPC subunits
- Symbol rate: 10Gx(1792x33)/(64x800)/14 = 825MHz
  - Symbol rate of 825MHz is easy to generate from standard oscillators in the range 25-170MHz (e.g. 25, 100, 125, 150MHz) with a N/M PLL multiplication

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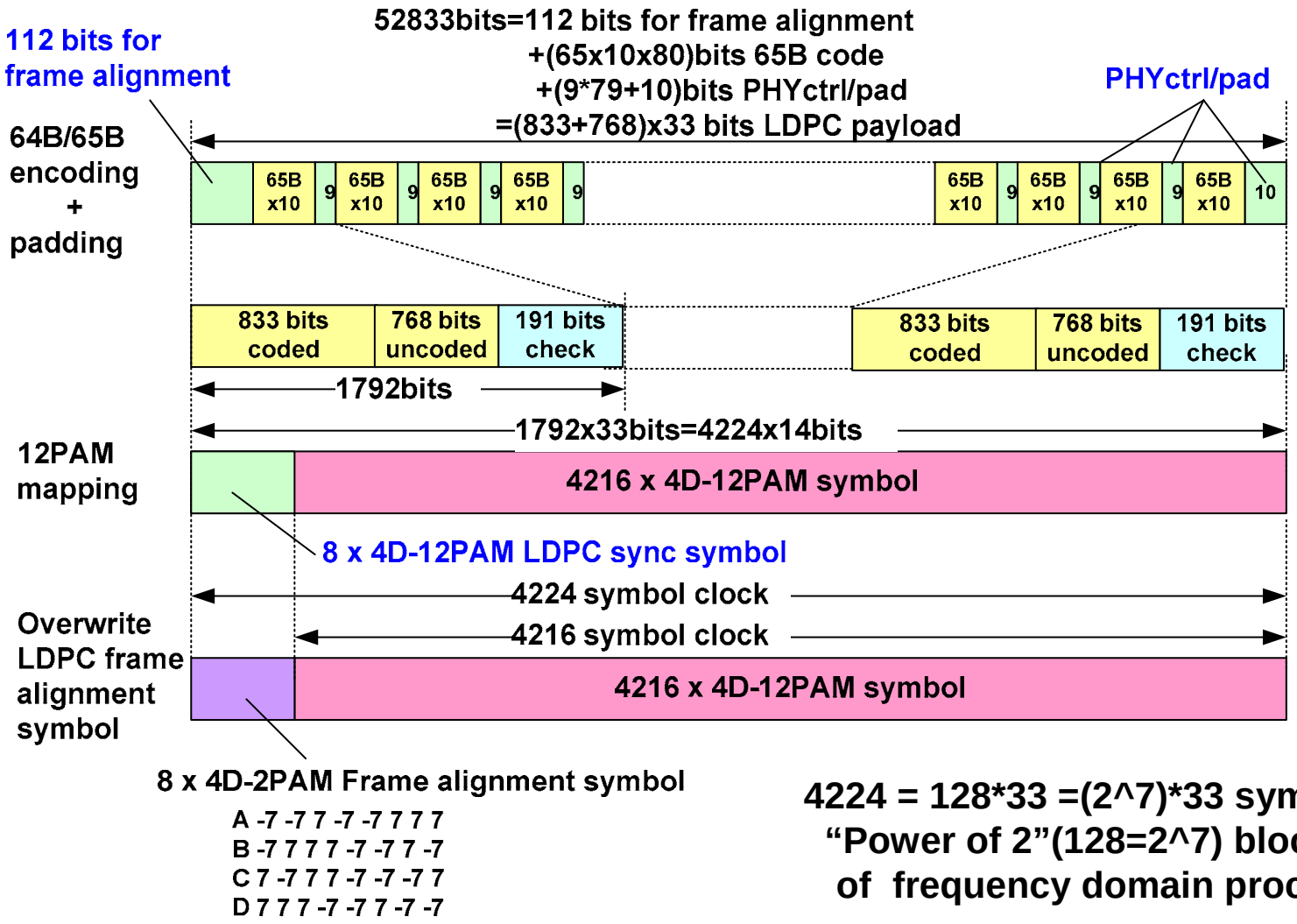
Framing and Control (cont')



4224 = 128*33 =(2^7)*33 symbol clock
"Power of 2"(128=2^7) block facilitates use of frequency domain processing.

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Frame alignment parameters

Frame alignment parameters	
Num. of Frame alignment symbol (FAS) bits	32 bits
Num. of candidate positions	4224
Assumed BER before decoding	<1E-12
Average reframe time (Trf)	2.00 frames
Variation reframe time (Vrf)	0 frames
False In-frame time (Tff)	4.367E15 frames = 709 years
Out-of-frame detection time (Tof)	4.00 frames
Misframe time (Tmf)	9.537E41 frames =1.55E29 years

Note 1 : Two successive good FAS confirmation for frame alignment
Note 2 : Four successive bad FAS confirmation for frame misalignment
Ref. : D. Choi, “Frame alignment in digital carrier system – A tutorial”, IEEE Communications magazine, Feb. 1990, p47-54

PAM2 Frame alignment can achieve fast reframe and negligible misframe

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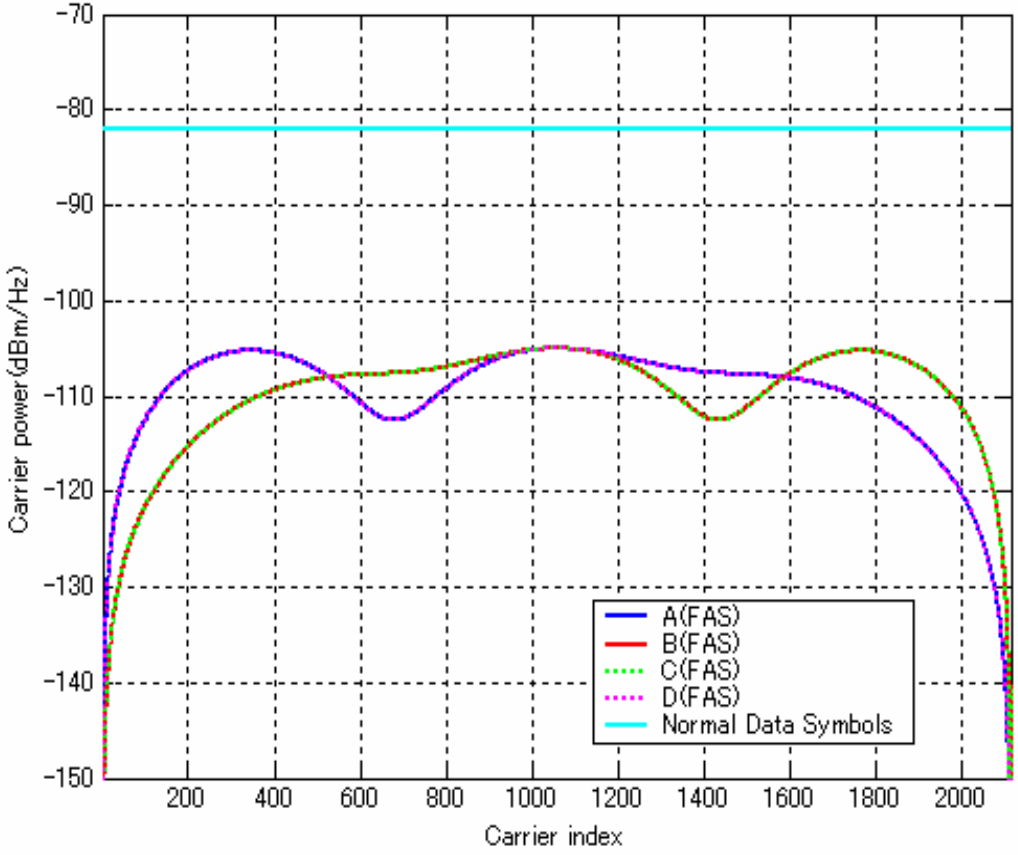
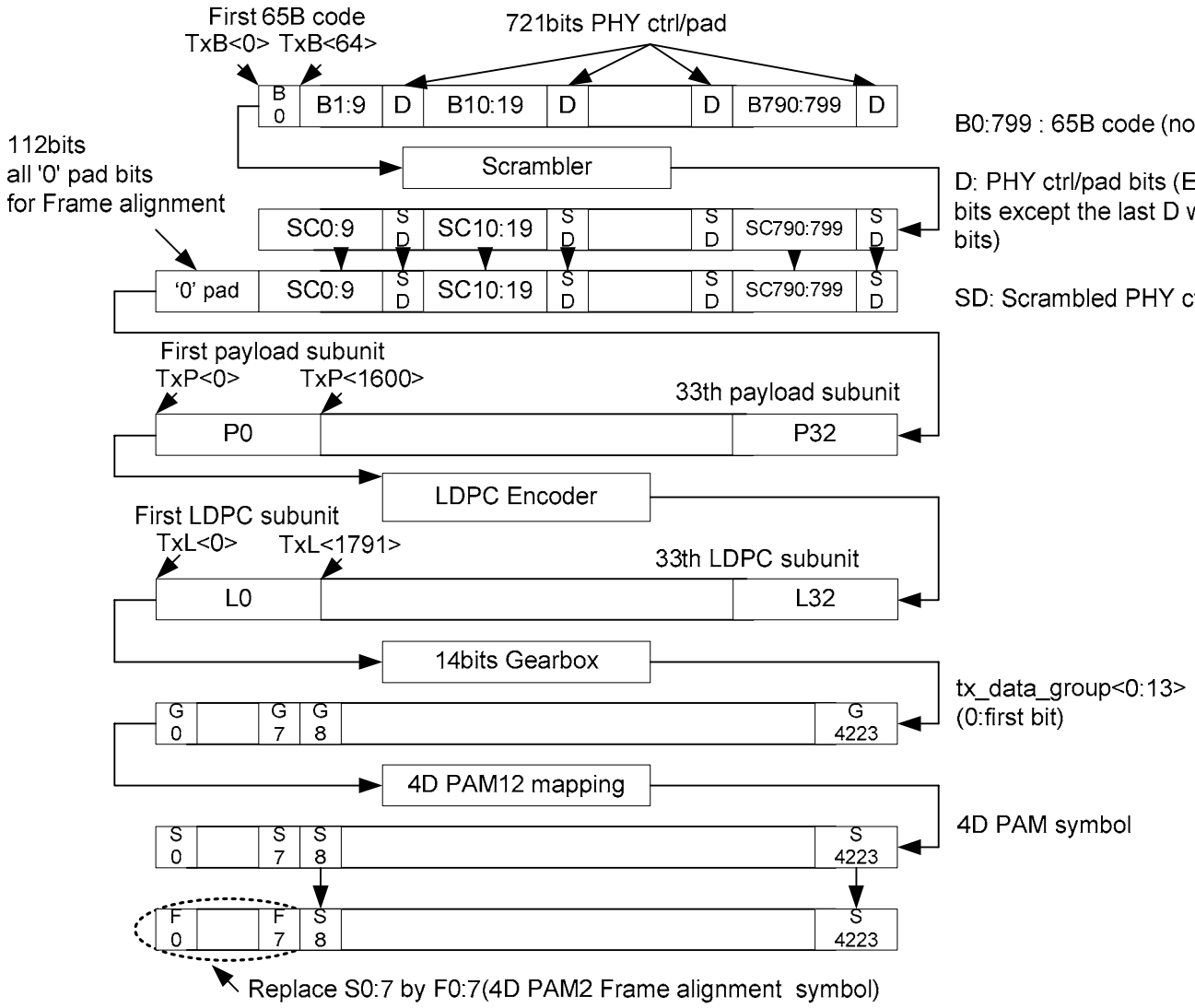
Frame alignment symbol spectrum

- All four Frame alignment symbols (FAS) have good Spectral behavior
  - Spectral Null at DC and Nyquist frequency
  - Low peak to average level
  - No spectral lines
- FAS spectrum has 2112 (=4224/2) carriers in 412.5MHz (=825MHz/2)
- Assumptions
  - Max. transmit voltage: 2.0Vp-p
  - No digital filter



Transmit bit ordering



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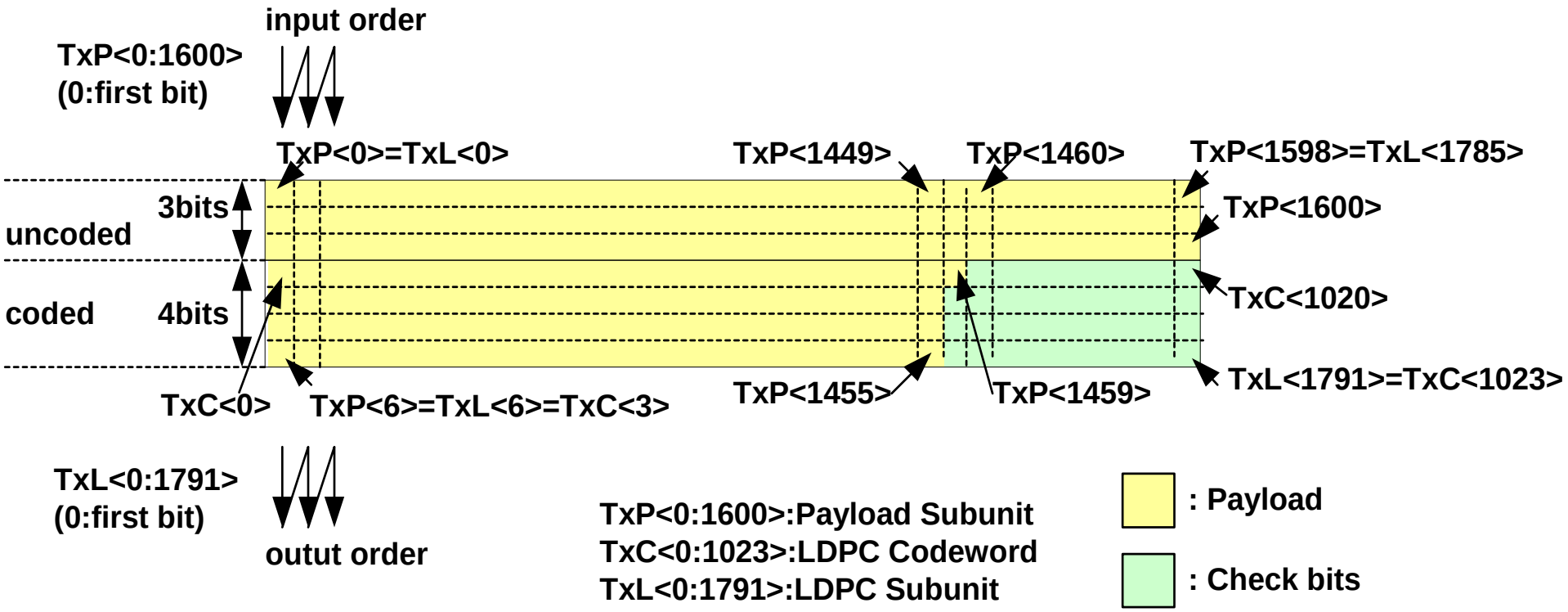
LDPC Subunit Systematic Encoding

LDPC Encoding (systematic)



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LDPC to PAM12 mapping

- Based on www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf
  - PAM12 mapping achieved with simple tables below
    - TA=X1*8+X2 (12PAM mapping on wire A)
    - TB=Y1*8+Y2 (mapping wire B)
    - TC,TD shall use tx_data_ group<7:13> in the same way as TA,TB

Tx_data_group<0:2> (uncoded bits A&B)	X1	Y1
000	-1	-1
001	-1	0
011	-1	1
010	0	1
110	1	1
111	1	0
101	1	-1
100	0	-1

Tx_data_group <3:4> (coded bits wire A)	X2
00	-3
01	-1
11	1
10	3

Tx_data_group <5:6> (coded bits wire B)	Y2
00	-3
01	-1
11	1
10	3

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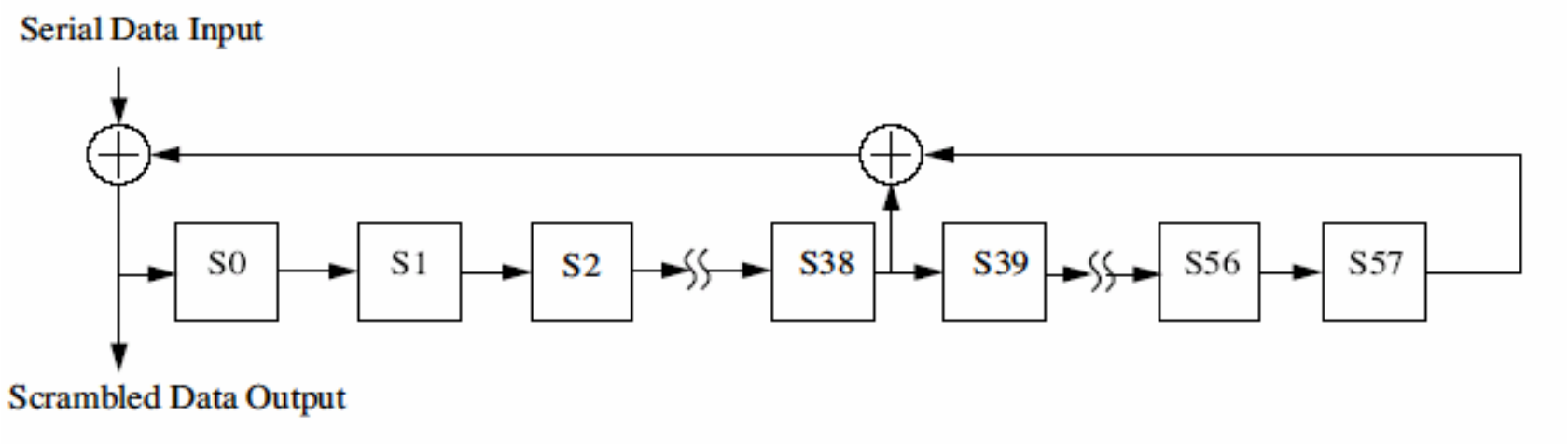
Scrambler

Objective : Maintain DC balance
Scrambler polynomial: $x^{58}+x^{39}+1$



The PAM2 frame alignment symbols and LDPC check bits shall not be scrambled.

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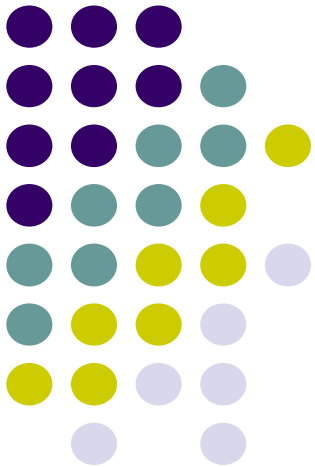
Performance



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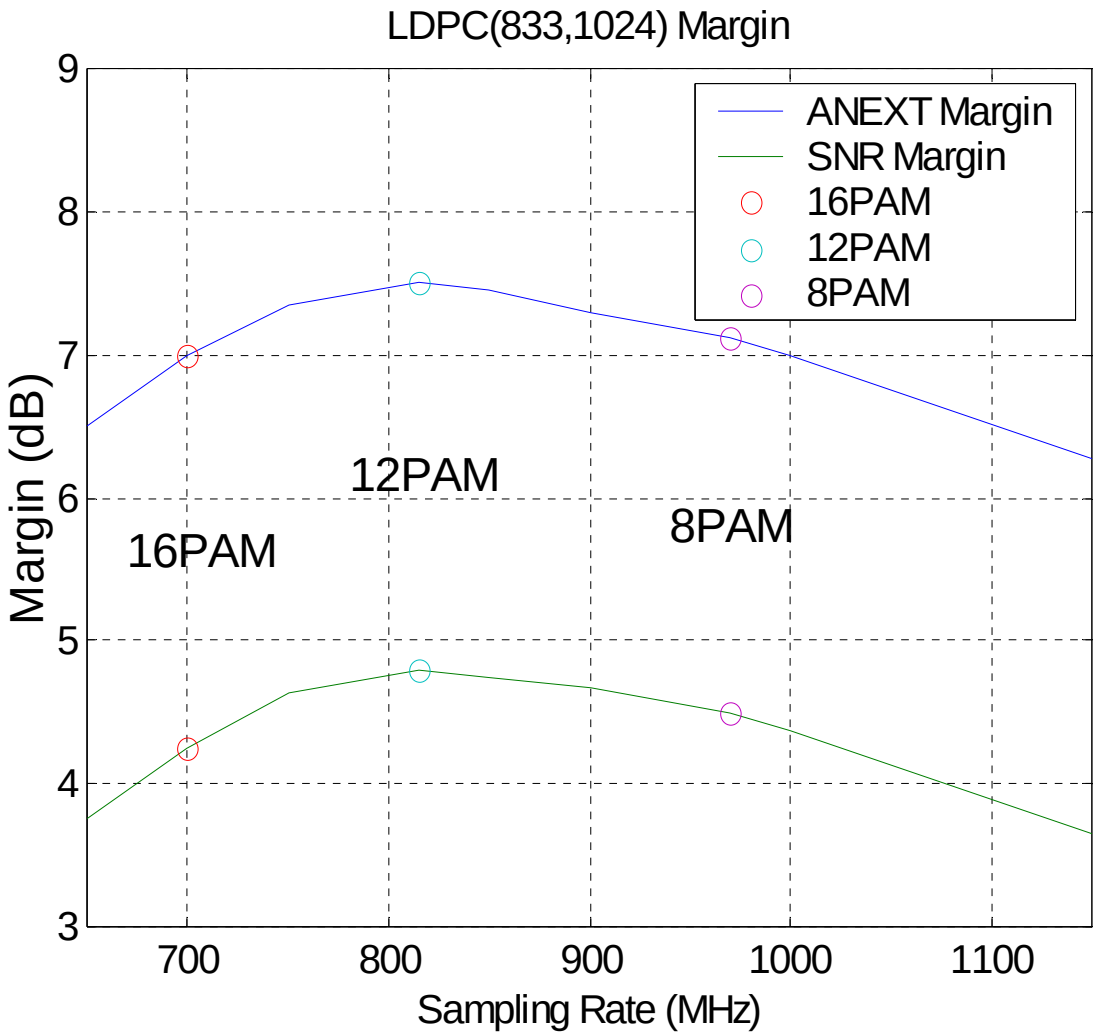
LDPC(833,1024) Margin

- Largest Margin or Noise Immunity close to 800MHz
- Assumptions:
  - Model 3 with AWGN=-150dBm/Hz
  - 4dBm Tx Power (2V pk-pk at MDI)
  - LDPC 8dB gain
  - EcCanc(60dB), NXCanc(40dB), FXCanc(20dB), ADC(9b), DAC(10b)



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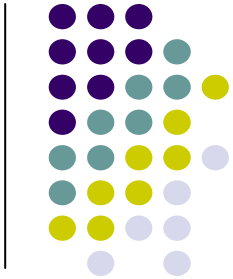

12PAM at 825MHz (cont)

- 12PAM at 825MHz has largest margin
  - Multiple presentations confirm largest margin close to 800MHz
  - Broadcom~800MHz, NEC Electronics ~820MHz, Solarflare~833MHz, KeyEye~833 (uncoded 8PAM)
- 12PAM has lower symbol rate
  - ~20% reduction in digital power consumption relative to 8PAM
  - ~20% reduction in bandwidth of analog and mixed signal circuits relative to 8PAM
- 12PAM can be combined efficiently with THP
- Allows for Framing and MAC/PHY Control overhead

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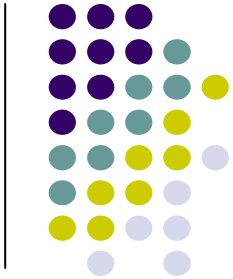

Performance Margin

- 12PAM LDPC(833,1024) requires receiver SNR=23.8dB for BER<1E-12
- ANEXT Link Margin (Salz).
  - Model 1&3: ~7.5dB
  - Model 2: ~6.6dB
- SNR Link Margin (Salz)
  - Model 1&3: ~4.8dB
  - Model 2: ~5.6dB

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Transmitter assumptions

- Modulation: 12PAM
- FEC code: LDPC(833,1024)
- Symbol rate: 825MHz
- DAC resolution: 10bits
- DAC speed: 825MHz
- Max transmit launch voltage: 2volt pk-pk at MDI port

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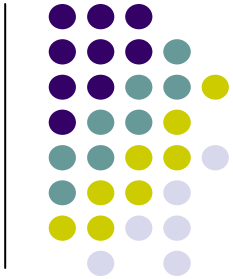

Receiver assumptions

- Echo suppression: 60dB
- NEXT suppression: 40dB
- FEXT suppression: 20dB
- ADC speed: 825MHz
- Ideal ADC resolution: 9bits
- PAR at input to ADC: 14dB
- Echo cancellation prior to ADC: 25dB
- Additive Gaussian noise at receiver: -150dBm/Hz

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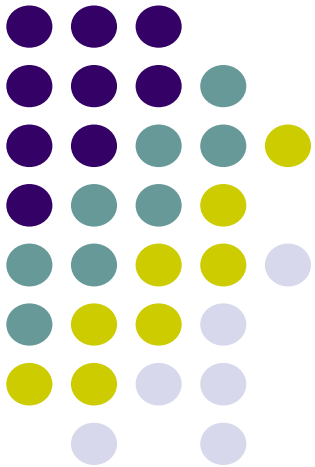
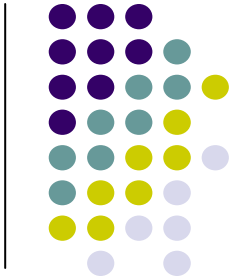
Implementation



Teranetics

NEC

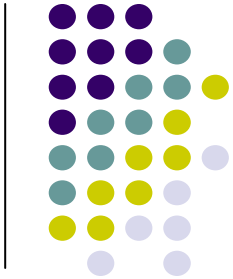


Implementation Complexity

- Digital Gates: 4M if operated at Fs
  - This is not a recommendation to operate digital at Fs
- Power: 8W assuming 90nm process
  - Digital: ~3.5W
  - Analog: ~4.5W
- Tradeoffs possible between power and gate count

Teranetics NEC

LDPC-PAM12 Proposal Summary



- Achieves 5-6dB of margin on approved channel models 1-4
  - Required to meet 10G objectives with sufficient margin
- Low Intrinsic latency of ~160ns
- Very similar parameters to multiple PHY proposals (THP, LDPC, Symbol rate ~800MHz)