Analysis of comments on D2.1

Editorial Staff 802.3an

(650) 704 7686
skasturia@teranetics.com

Introduction

- Draft 2.1 has been online; sympathy goes to
  - Brad Booth for Clause 1, 30 & 44
  - Eric Lynskey for Clause 28 & 55.6
  - Mike McConnell for Clause 45
  - Jose Tellado for PCS and PMA sections
  - Sandeep Gupta for the PMA Electrical
  - Chris DiMinico for the Link Segment
  - Terry Cobb for the MDI and environmental specification
- The draft has been updated from D2.0
- We have ~247 comments (204 are new)
  - ~168 are T & TR
    - 104 are TR (71 are new TRs), 64 are T
  - ~79 are E & ER
    - 14 are ER (only 4 new ERs), 65 are E

Clarification on commenting instructions

- For subclause, put in the full descriptions, e.g., 55.7.1 rather than 7.1
- For subclause, when identifying figures/tables/equations, do also put in the associated subclause number
  - For example, put: 55.7.1 Figure 55-1 do NOT just put : Figure 55-1

Comment stats by sections

- On clause 28: 15
  - TR: 3, T: 6, ER: 0, E: 6
- On clause 45: 31
  - TR: 1, T: 10, ER: 0, E: 20
- On clause 55: 176
  - TR: 94 (65 new), T: 47, ER: 11, E: 24
  - On PMA electricals: 11
    - TR: 8 (2 new), T: 3, ER: 0, E: 0
  - On Management: 6
    - TR: 3, T: 2, ER: 0, E: 1
  - On link segment: 33
    - TR: 17 (8 new), T: 9, ER: 4 (0 new), E:3
  - On MDI: 6
    - TR: 4 (2 new), T: 2, ER: 0, E: 0
  - On PCS/PMA & other: 120
    - TR: 62 (50 new), T: 31, ER: 7, E: 20
- On whole draft or clauses 1, 30, 30B, 44: 25
  - TR: 6, T: 1, ER: 3, E: 15

Clause 28 – Eric Lynskey

- Comment stats: TR: 3, T: 6, ER: 0, E: 6
- Minor items or issues (no major issues this time around)
  - Comment 179, NLP Receive Link Integrity Test
  - Cleanup and coordination between 28 and 45
  - Ordering of unformatted pages
- Editorials to discuss in Task Force
  - 184

Clauses 1, 30, 44; Anx. 30B – Brad Booth

- Clause 1 Comment stats: E: 4
- Clause 30 Comment stats: ER: 1, E: 1
  - Remove unchanged material
- Clause 44 Comment stats: TR: 1, ER: 1
  - Comment #236 should be resolved by the normative comment on Clause 55 delay parameters
  - Remove unchanged material

Clause 45 – Mike McConnell

- Comment stats: TR: 1, T: 10, ER: 0, E: 20
- Refinement

Clause 55.1-4 – PCS/PMA: Jose Tellado

- Comment stats: Total: 120 (including 55.11, 55.12)
  - TR: 62 (50 new), T: 31, ER: 7, E: 20
  - Includes 55.11 (Delay) and 55.12 (PICS)
- Major items or issues
  - Delay constraints
  - PHY control (Start-up)
    - Refinements to: Info Field, Power Backoff, State machine, Variables,
- It is proposed that we deal with ER comments as follows:
  - Approve: Comments #9, #63, #64, #65, #20329, #20332, #20351.
  - Disapprove: None

Clause 55.1-4 – PCS/PMA: Jose Tellado

- PHY control (start-up)
  - Comments (~60, which corresponds to ~50%)
  - Most comments aim to increase clarity and prevent interoperability problems
  - Main topics include refinements or clarification of:
    - InfoField
    - PBO
    - THP
    - PHY control state diagram
    - State diagram conventions
    - Timer, counters and variable definition

Clause 55.11 – PCS/PMA: Jose Tellado

- Delay Constraints
  - Comments (10):
  - Draft 2.1 specifies a maximum latency of ~10 microsec
  - Shimon Mueller, Hugh Barrass, Pat Thaler, David Law, Geoff Thompson suggested reducing the max latency (~2.5 microsec)
  - Recommendation:
    - Task force to discuss and reduce the maximum latency

- See text on Delay Text slide

Clause 55.5 – PMA elec.: Sandeep Gupta

- Comment stats: TR: 8 (2 new), T: 3, ER: 0, E: 0

- Major items or issues
  - SFDR definition: comment #48, #119, #20579 open from D2.0
  - TX PSD refinements: #114, #134
  - Additional test mode requested to measure impedance balance" #101
- Resolved comments that have not been closed
  - #20275 Shall/should; coupler definition; Alien noise modeling
  - #20579 SFDR definition
  - #20363 Common mode noise rejection
  - #20691 PSD ripple
  - #20693 Impulse noise immunity
  - #20696 Zero at Fs/2 in TX PSD

Clause 55.6 – Management: Eric Lynskey

- Comment stats: TR: 3, T: 2, ER: 0, E: 1

- Items or issues (no major issues this time around)
  - Cleaning up of 45 and 55.6 register names
  - Comment 84, MASTER-SLAVE fault condition

Clause 55.7 – Link Segment: Chris DiMinico

- Comment stats: TR: 17 (8 new), T: 9, ER: 4 (0 new), E:3
- Refinement

Clause 55.8 – MDI: Terry Cobb

- Comment stats: TR: 4 (2 new), T: 2, ER: 0, E: 0

- Major items or issues
  - Impedance balance
  - Refinement

Delay – 50.3.7

50.3.7 WIS data delay constraints

The sum of the transmit and receive data delays for any implementation of the WIS shall not exceed 14336 BT. Transmit data delay is measured from the input of a given unit of data by the PCS at the WIS service interface to the presentation of the same unit of data by the WIS to the PMA at the PMA service interface. Receive data delay is measured from the input of a given unit of data by the PMA at the PMA service interface to the presentation of the same unit of data by the WIS to the PCS at the WIS service interface. The time required to insert or process any necessary overhead or stuff octets must be included as part of the data delay incurred by the WIS. No constraint is placed on the individual values of the transmit and receive data delays for a given implementation, provided their sum falls within the above limit.

Delay – 51.3.3

51.3.3 Delay Constraints

The PMA receives a one bit data stream from the PMD and presents a sixteen bit wide data unit to the PMA client. Received bits from the PMD are buffered to facilitate proper deserialization of the rx_data-group<15:0> to the PMA client. These functions necessitate an internal PMA delay of at least sixteen bit times. In practice, this serial to parallel conversion may necessitate even longer delays of the incoming data stream.

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers will conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The sum of transmit and receive delay constraints for the serial PMA/PMD sublayer shall be no more than 512 BT. The serial PMA/PMD sublayer includes the serial PMA, the serial PMD, and two meters of fiber.

Delay – vs. cable length

- Clause 44 covers how to account for media delay

The term 10GBASE-R, specified in Clauses 49, 51, and 52, refers to a specific family of physical layer implementations based upon 64B/66B data coding method. The 10GBASE-R family of physical layer implementations is composed of 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER.

The term 10GBASE-W, specified in Clause 49 to Clause 52, refers to a specific family of physical layer implementations based upon STS-192c/SDH VC-4-64c encapsulation of 64B/66B encoded data. The 10GBASE-W family of physical layer standards has been adapted from the ANSI T1.416-1999 (SONET STS-192c/SDH VC-4-64c) physical layer specifications. The 10GBASE-W family of physical layer implementations is composed of 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

All 10GBASE-R and 10GBASE-W PHY devices share a common PCS specification (see Clause 49). The 10GBASE-W PHY devices also require the use of the WAN Interface Sublayer, (WIS) (Clause 50).

Specifications of each physical layer device are contained in Clause 52 through Clause 54 inclusive.

44.1.4.5 WAN Interface Sublayer (WIS), type 10GBASE-W

The WIS provides a 10GBASE-W device with the capability to transmit and receive IEEE 802.3 MAC frames within the payload envelope of a SONET STS-192c/SDH VC-4-64c frame.

44.1.5 Management

Managed objects, attributes, and actions are defined for all 10 Gigabit Ethernet components. Clause 30 consolidates all IEEE 802.3 management specifications so that 10/100/1000 Mb/s and 10 Gb/s agents can be managed by existing network management stations with little or no modification to the agent code.

44.2 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

44.3 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. Table 44–2 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay in bit time as specified in 1.4 and pause_quanta as specified in 31B.2.

Equation (44–1) specifies the calculation of bit time per meter of fiber or electrical cable based upon the parameter n, which represents the ratio of the speed of electromagnetic propagation in the fiber or electrical cable to the speed of light in a vacuum. The value of n should be available from the fiber or electrical cable manufacturer, but if no value is known then a conservative delay estimate can be calculated using a default value of $n = 0.66$. The speed of light in a vacuum is $c = 3 \times 10^8$ m/s. Table 44–3 can be used to convert fiber or electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

$$\text{cable delay} = \frac{10^{10}}{nc} \text{ BT/m} \qquad (44\text{–}1)$$

Delay – Proposed text

55.11.7 Delay constraints

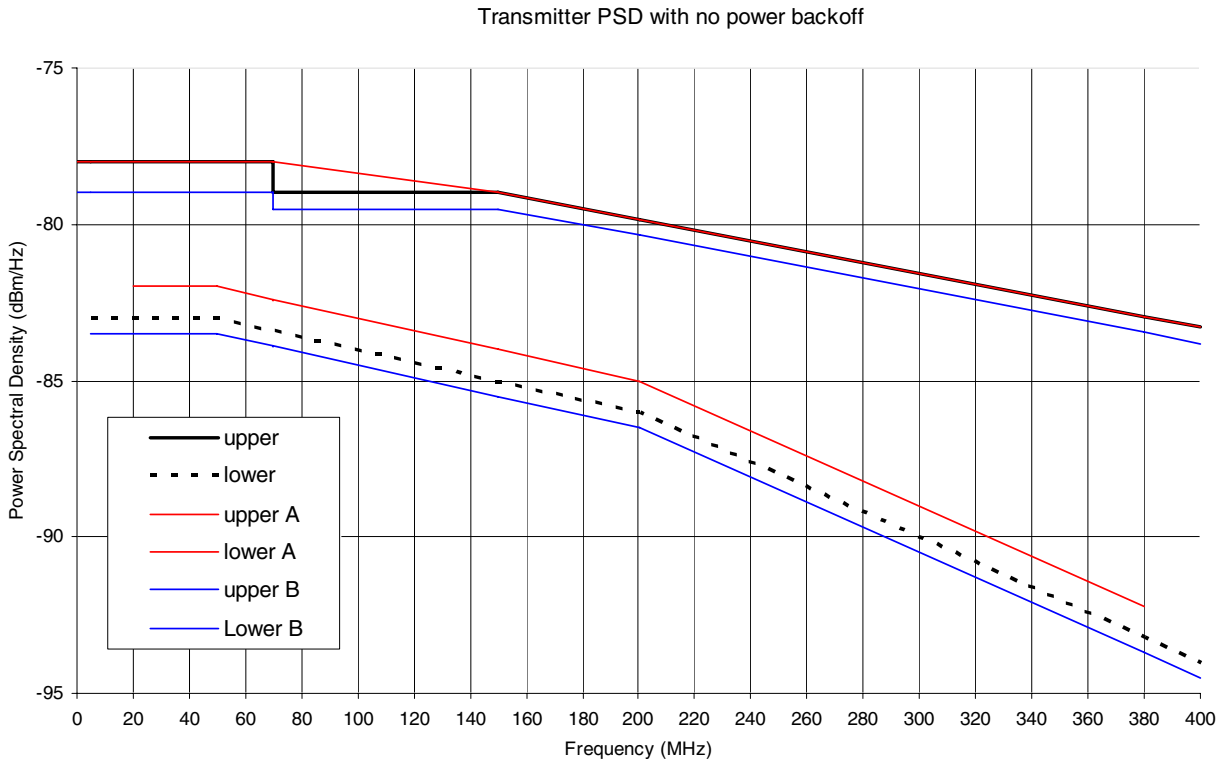
In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementors must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of a 10GBASE-T transceiver shall not exceed 25,600 BT. Transmit data delay is measured from the input of a given unit of data at the XGMII interface to the presentation of the same unit of data by the PHY to the MDI interface. Receive data delay is measured from the input of a given unit of data at the MDI interface to the presentation of the same unit of data by the PHY to the XGMII interface. The time required to insert or process any necessary overhead or stuff octets must be included as part of the data delay incurred by the 10GBASE-T PHY.

Note that the physical medium interconnecting two PHYs introduces additional delay in a link. Equation (44-1) specifies the calculation of bit time per meter of electrical cable and Table 44-3 can also be used to convert electrical cable delay values specified relative to the speed of light or in nanoseconds per meter.

Round-trip delay through a link consisting of two compliant PHYs and any 55.7 compliant media connecting them shall not exceed 51,200 BT plus the media delay (as computed using equation 44-1 or Table 44-3).

PSD masks



- Reduce frequency range of lower PSD mask
  - Currently it goes from 5MHz to 400MHz
  - New proposal is 20MHz to 380MHz
- Remove step in upper PSD
  - Straight line fit from 70MHz to 150MHz
- Narrow the PSD mask range
  - By 0.5dB or by >=1dB
- Lower the PSD masks by 0.5dB

Clause 45 formatting errors

If the Auto-Negotiation advertisement register (Register 4) is present, (see 28.2.4.1.3), then this register is a copy of the Auto-Negotiation advertisement register (Register 4). In this case reads to the AN advertisement register (7.16) will report the value of the Auto-Negotiation advertisement register (Register 4), writes to the AN advertisement register (7.16) will cause a write to occur to the Auto-Negotiation advertisement register (Register 4).

45.2.7.7 AN LP base page ability register (7.19)

Support for 10GBASE-T requires support to store the link partner (LP) base page ability register as shown in Table 45–121. All of the bits in the AN LP base page ability register are read only. A write to the AN LP base page ability register shall have no effect. Register 7.19 is a copy of register 5, if present (See 28.2.4.1).

Table 45–121—AN LP base page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.19.15	Next page	See 28.2.1.2	RO
7.19.14	Acknowledge	See 28.2.1.2	RO
7.19.13	Remote fault	See 28.2.1.2	RO
7.19.12	Extended next page	1 = Extended next page will be used 0 = Extended next page will not be used	RO
7.19.11:5	Technology ability field	See 28.2.1.2	RO
7.19.4:0	Selector field	See 28.2.1.2	RO

[a]RO = Read Only

45.2.7.7.1 Extended next page (7.19.12)

When set to one bit 7.19.12 indicates that the link partner has indicated support for extended next page. When set to zero bit 7.19.12 indicates that the link partner does not support extended next page.

45.2.7.8 AN XNP transmit register (7.22, 7.23, and 7.24)

45.2.7.9 The auto-negotiation extended next page (XNP) transmit register contains the next page link code word to be transmitted when extended next page is enabled by setting bit 7.0.13 to one. The contents are defined in 28.2.3.4. On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid extended Next Page Message Code that the device wishes to transmit. A write to registers 7.23 or 7.24 does not set mr_next_page_loaded. Only a write to register 7.22 will set mr_next_page_loaded to true as described in 28.2.4.1.8. Therefore, when updating the three register set, 7.23 and 7.24 register values should be written first followed by register 7.22. **AN LP XNP ability register (7.25, 7.26, and 7.27)**

Support for 10GBASE-T requires support for extended next pages and the provision of an AN LP XNP ability register (registers 7.25, 7.26, and 7.27) to store link partner extended next pages as shown in Table 45–122. All of the bits in the AN LP XNP ability register are read only. A write to the AN LP XNP ability register shall have no effect.