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Modifications to LDPC Proposal offering Lower Symbol Rate and Lower Latency

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Agenda

- Motivation for Lower Symbol Rate.
- PAM12 Coded Modulation
  - Set Partitioning.
  - Gray Mapping for Coded Bits.
  - A Good Constellation for THP.
  - Gray Mapping for Uncoded Bits.
- An Alternate Code with Lower Latency.
- Simulation Results.

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Lower Symbol Rate

- Rao's proposed code operates at 1 GHz symbol rate.
- There is no significant increase in channel capacity of CAT6e after 850 MHz @ 100m.
- Higher symbol rate requires more analog and digital power and area.
- All PAR requirements can be met with lower symbol rates.

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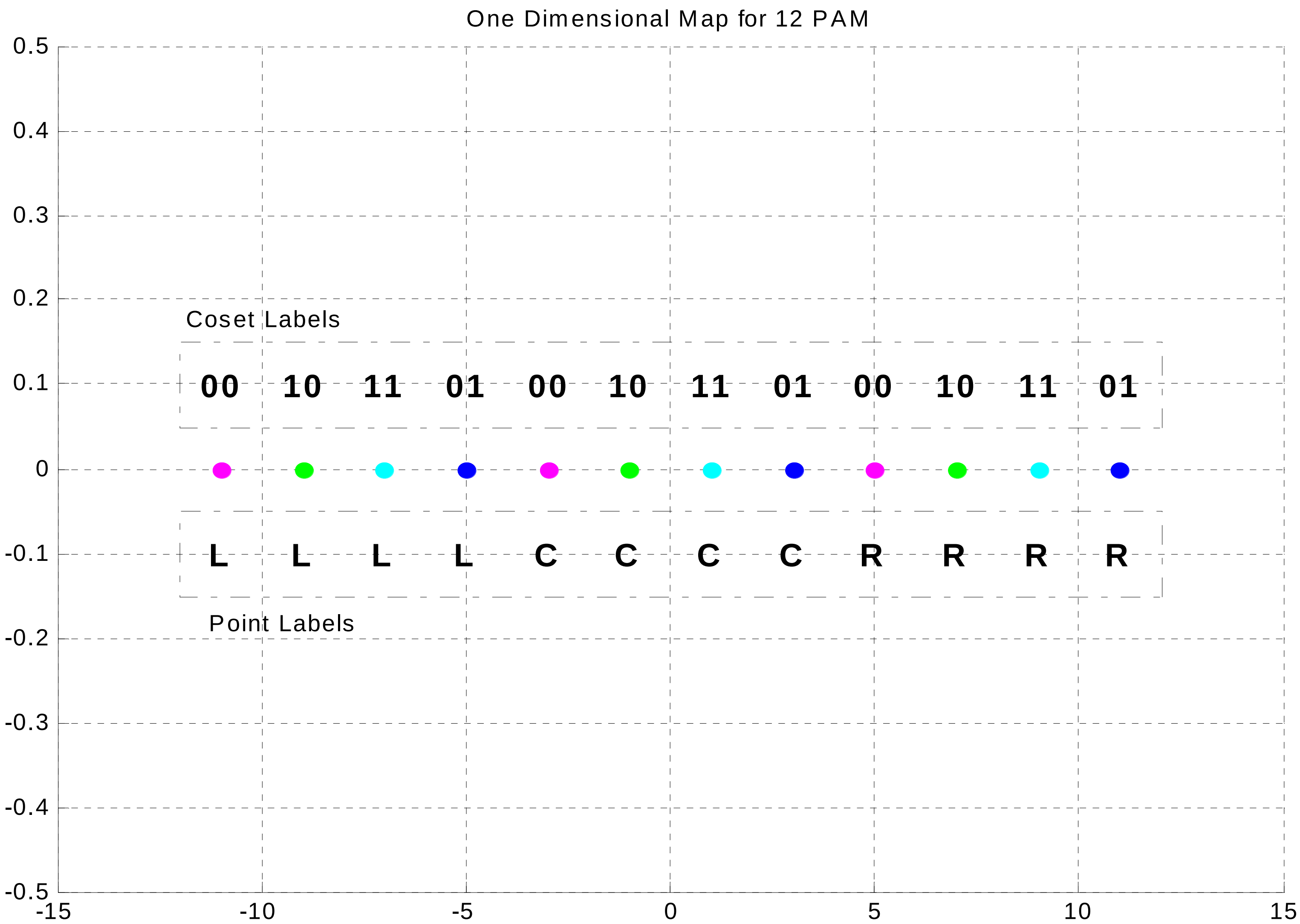
12PAM Set Partitioning

- Following Rao's proposal:
  - 12 dB set partitioning.
  - 4 cosets per dimension.
  - Gray mapping for coded bits (cosets).
- Each 1D coset now has 3 points, L(left), C(center), R (right).
- Each 4 D coset has 81 points, that can carry 6 bits.

One Dimensional Map



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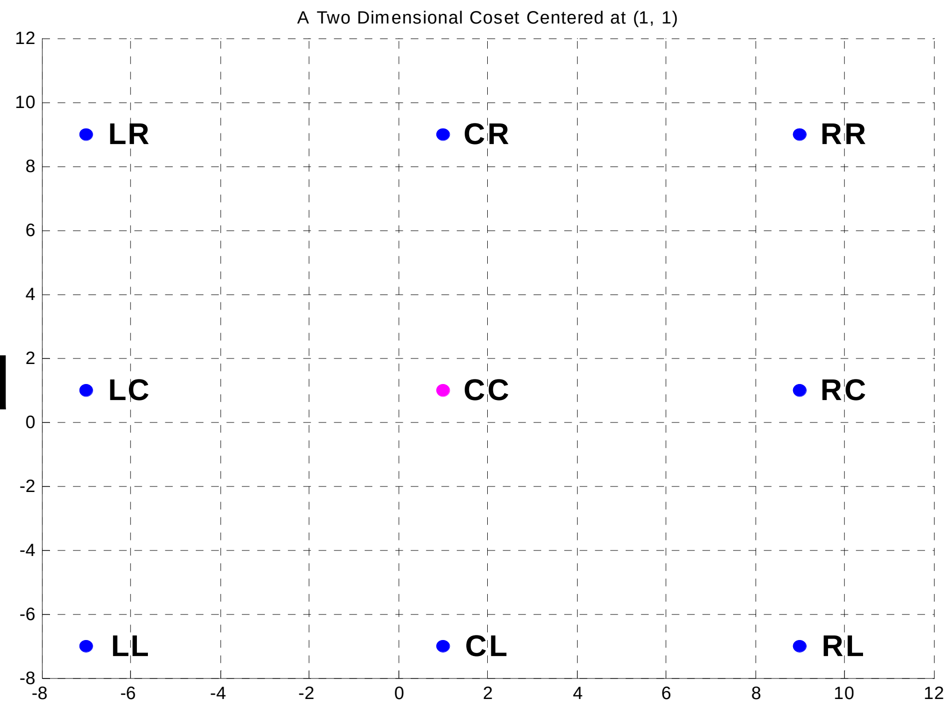
2D View of the Constellation

- Each 2D coset contains 9 points.
- Each 2D coset can carry 3 bits.
- One point is extra and can be removed or used for control.



A Good Constellation for THP

- For an i.i.d. input, the output of the THP tends to be uniform i.i.d.
- The average and the peak of the THP output power is:
  – Independent of the average input power.
  – Dependent of the peak input power.
- A good choice is to remove the point in the middle.

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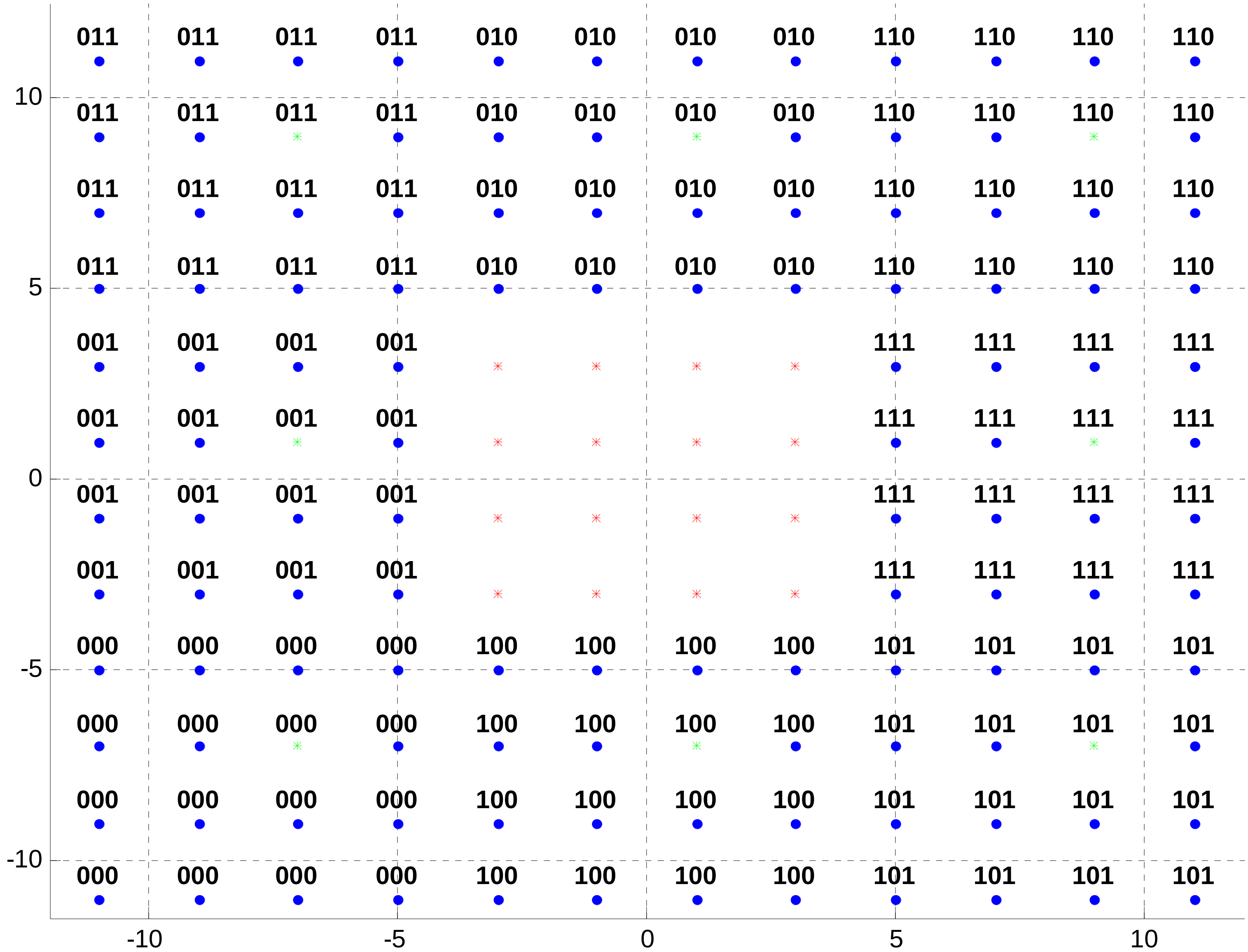
Gray Mapping for Uncoded Bits

- The 8 point coset results in a symmetric constellation.
- Optimize the BER for the uncoded bits by Gray mapping.
- A small table of 8 entries defines the whole constellation.

LL	000
LC	001
LR	011
CR	010
RR	110
RC	111
RL	101
CL	100

The Mapping of the Uncoded Bits in Two Dimensions



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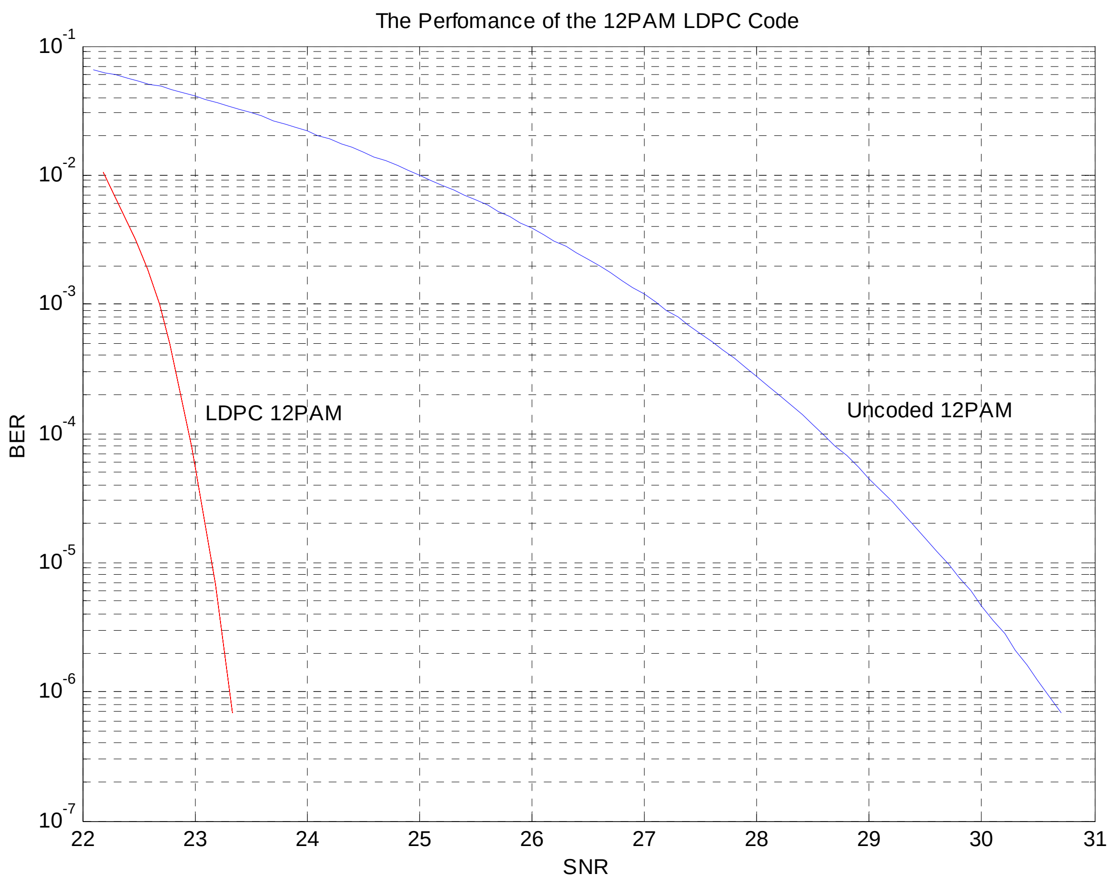
A 12PAM Code

- Use the (2048, 1723) RS based LDPC code from Rao’s proposal.
- 8 coded bits and 6 uncoded bits per symbol interval.
- Symbol Rate = 843 MHz for 7.3% packet overhead (same as Rao’s proposal).
- Symbol Rate = 825 MHz for 5% packet overhead.
- Exact symbol rate and overhead can be further optimized.

Simulation Results



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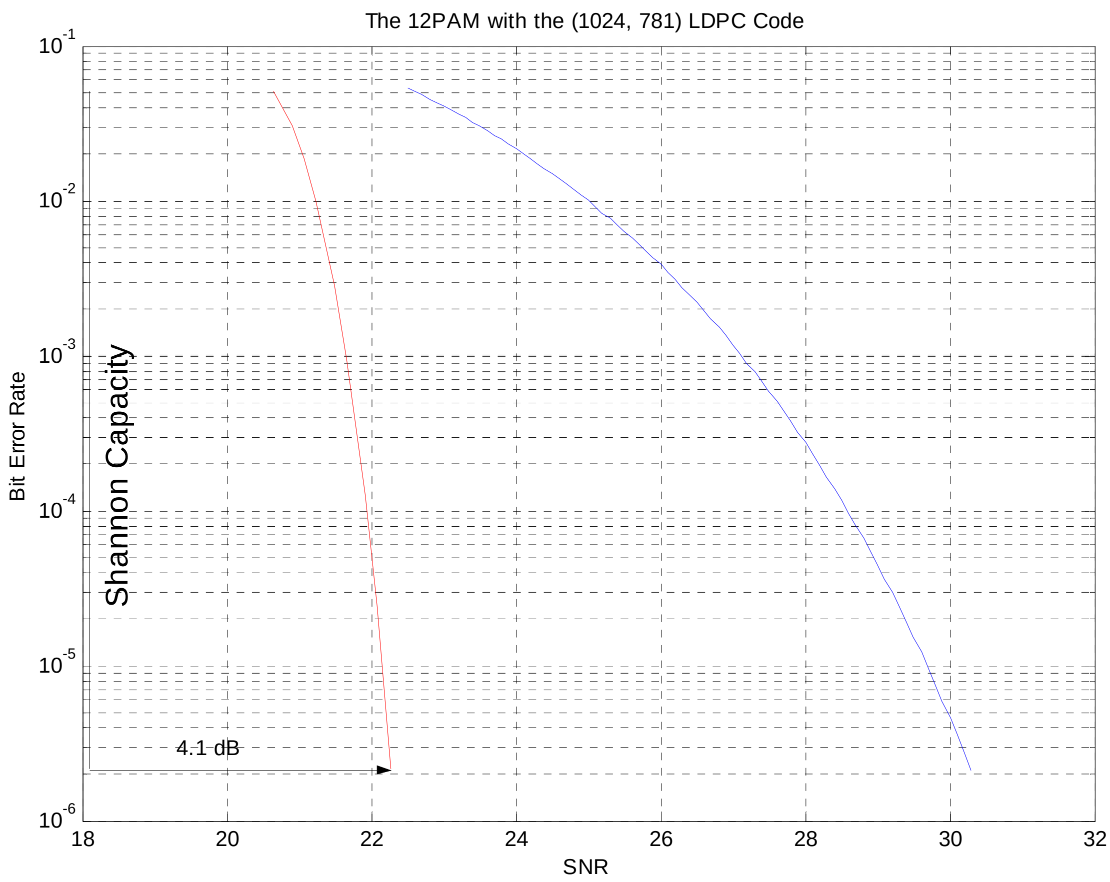
Performance

- More simulations need to be done for an accurate estimate of the performance.
- For 2*0.841 + 1.5 = 3.182 bit/symbol, the Shannon Bound requires SNR = 19.1 dB.
- Therefore at 1e-6, gap to the capacity is about 4.2 dB.
- The performance is comparable to Rao's code.

A Lower Latency Code

- Another code from the same class used in Rao’s proposal.
- Djurdjevic’s LDPC (1024, 781) code constructed from the RS(32, 2, 31).
- Variable Node Degree = Check Node Degree = 32.
- Each symbol carries 3.02 information bits.
- Symbol Rate 850 MHz for 3% overhead.

Simulation Results



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Performance

- More simulations need to be done to estimate the performance at 1e-12.
- For 2*0.7627+1.5 = 3.03 bits/sec the Shannon Bound is 18.16 dB.
- The gap to capacity at 2e-6 is 4.1 dB.
- The performance is comparable to Rao’s code.

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Summary

Code	Symbol Rate (MHz)	Latency (ns)
Rao's Code	1000	256-512
12PAM + (2048, 1723)	825	310-620
12PAM + (1024, 781)	850	150-300
8PAM + (1024, 781)	1000	128-256