Precoder Based 10GBASE-T Architecture Proposal

IEEE P802.3an
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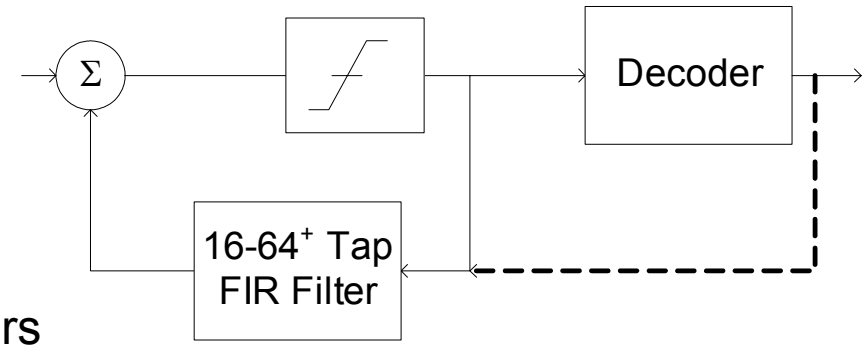
1Gbps Receiver: *the DFSE Loop*

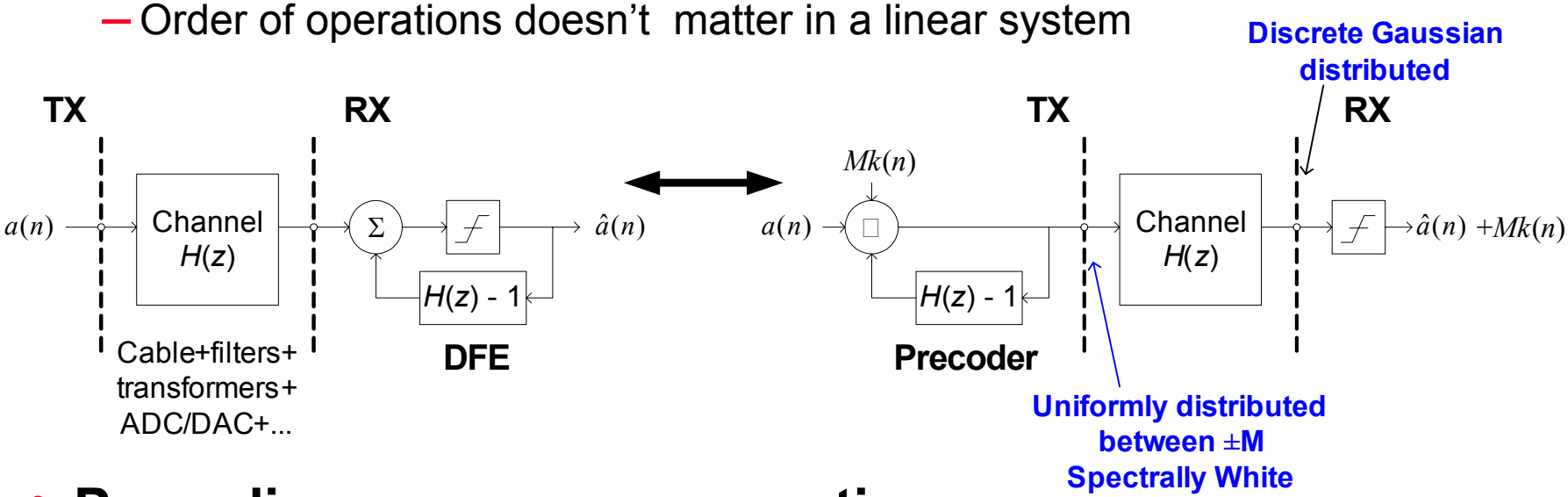
- **DFE cannot be separated from channel coding**
  - Catastrophic error propagation
  - Zero-delay decisions irreconcilable with basic idea of channel coding
  - Reduced state, parallel decision feedback TCM used in most receivers



- **Severely restricts decoder complexity**
  - Incompatible with block codes
- **Critical timing path introduced**
  - 1Gbps receiver does not scale well to 10Gbps

Precoding Avoids DFSE Critical Timing Path

- **Precoding moves DFE to transmitter**
  - Order of operations doesn't matter in a linear system

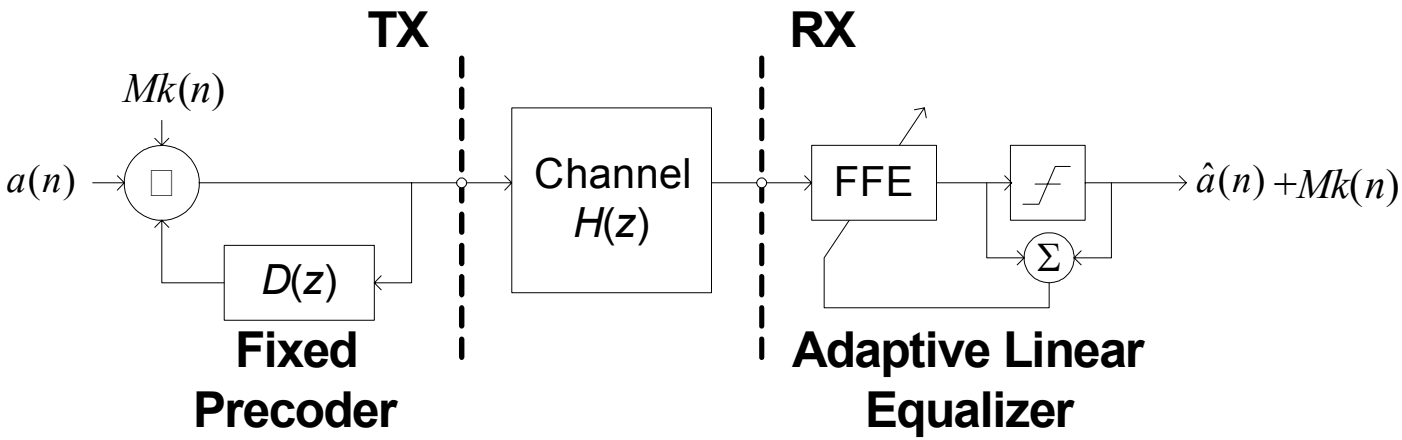


- **Precoding: no error propagation**
  - TX DFE operates on ideal, uncorrupted symbols

- **Precoding permits more powerful codes**
  - DFE decoupled from channel coding

Precoder Adaptation Not Necessary

- **Programmable precoding***
  - Precoder coefficients chosen at start-up to approximately match channel response
  - Adaptive linear RX equalizer removes residual ISI



- **Coefficients are a function of cable length**
  - Pre-store in small look-up table

* Gerstacker, Fischer, Huber, "A Transmission Scheme for Twisted Pair Lines with Coding, Precoding, and Blind Equalization," Globecom '97, pp 52-56

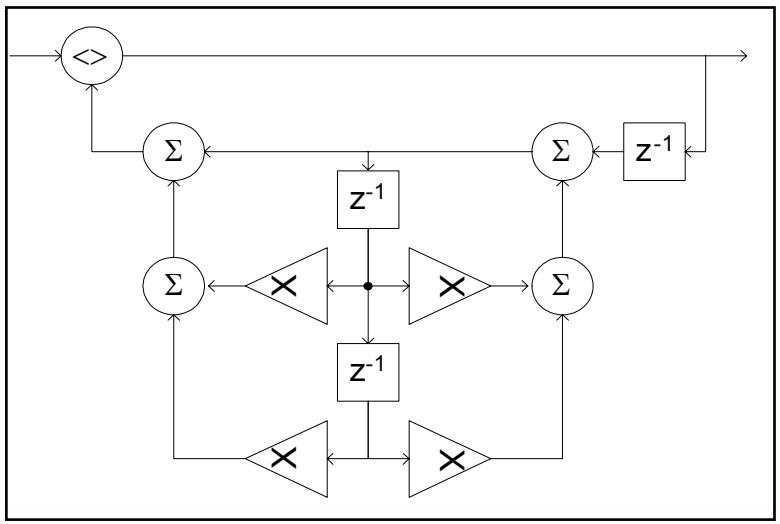
Number of Precoder Coefficients Reduced over 10x with IIR Model

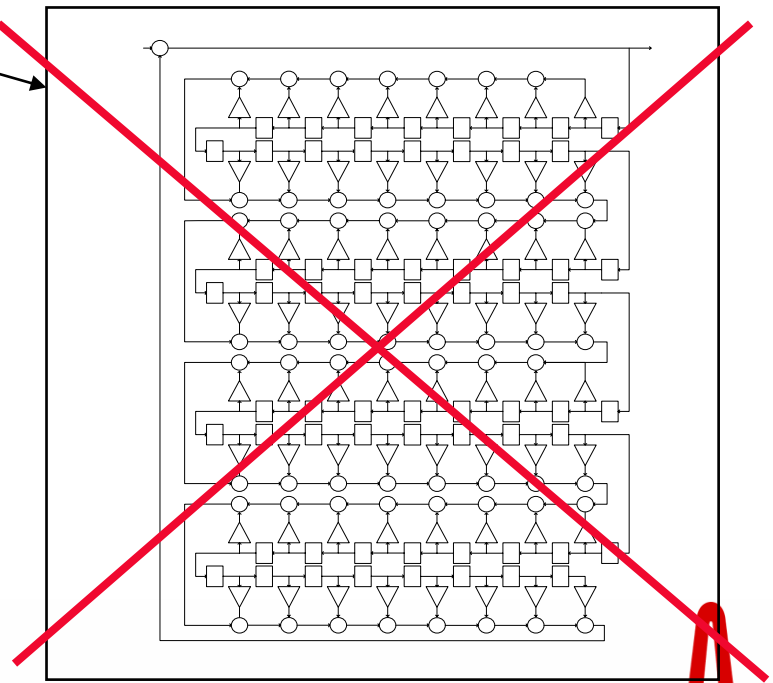
- Overall channel is accurately modeled by 2nd order IIR

$$H(z) = \frac{\left(1 - z^{-1}\right)\left(1 + \delta z^{-1}\right)}{1 - \alpha z^{-1} + \beta z^{-1}}$$

Only 3 coefficients

This instead of this

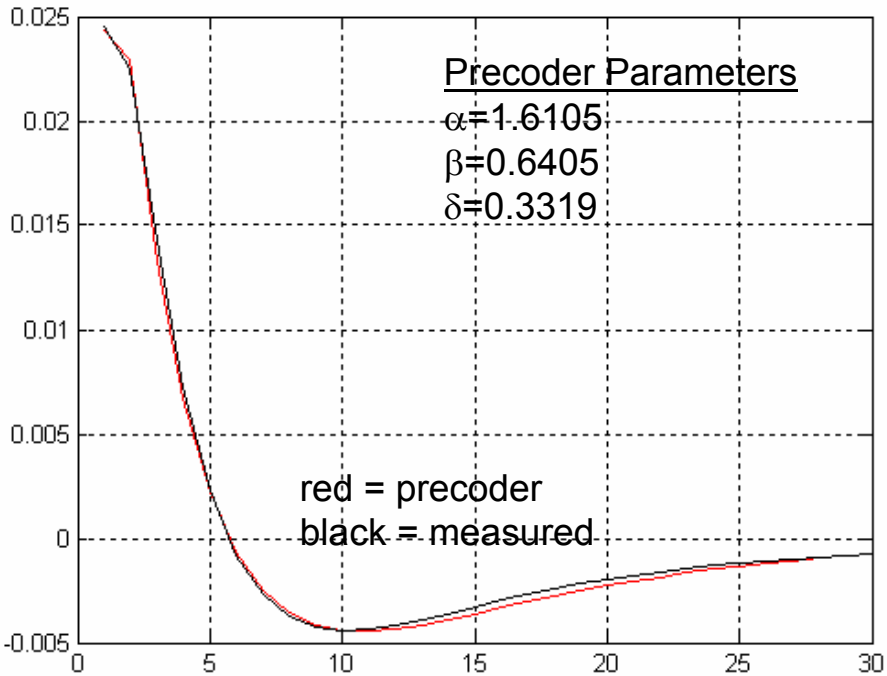




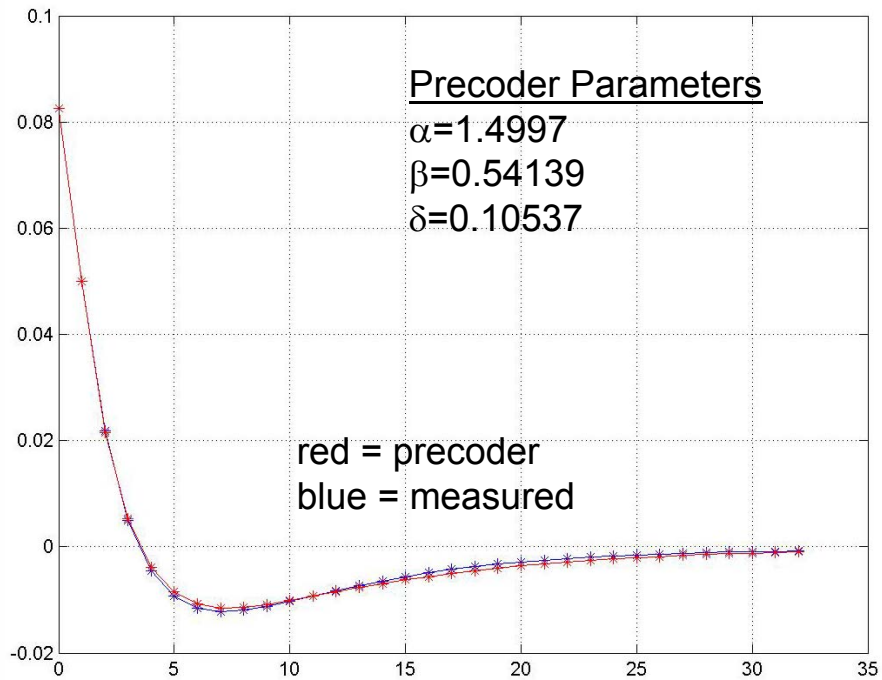
IIR Model a Good Match to UTP

- **Parameter values pre-computed to match cable response (compromise precoding)**
  - Tabulated vs length

Example: 100m Cat 7



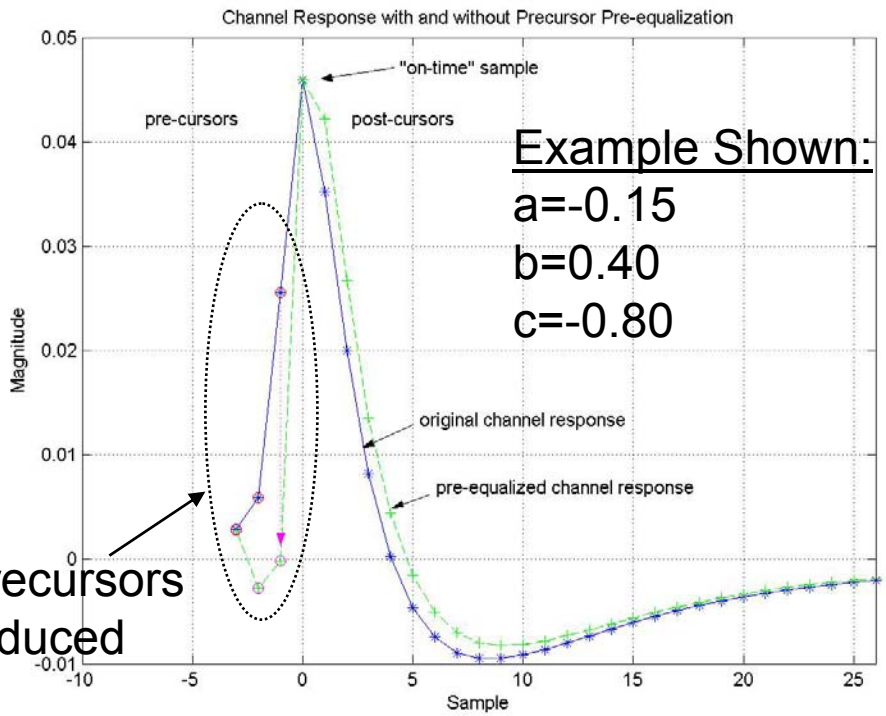
Example: 55m Cat 6



Simpler ADC and Start-up with TX Precursor Equalization

- **Worst case channel response has ≈3 significant precursors**
  - Merge Precursor pre-equalizer with transmit filter

$$T(z) = \left(1 + az + bz^2 + cz^3\right)z^{-3}$$

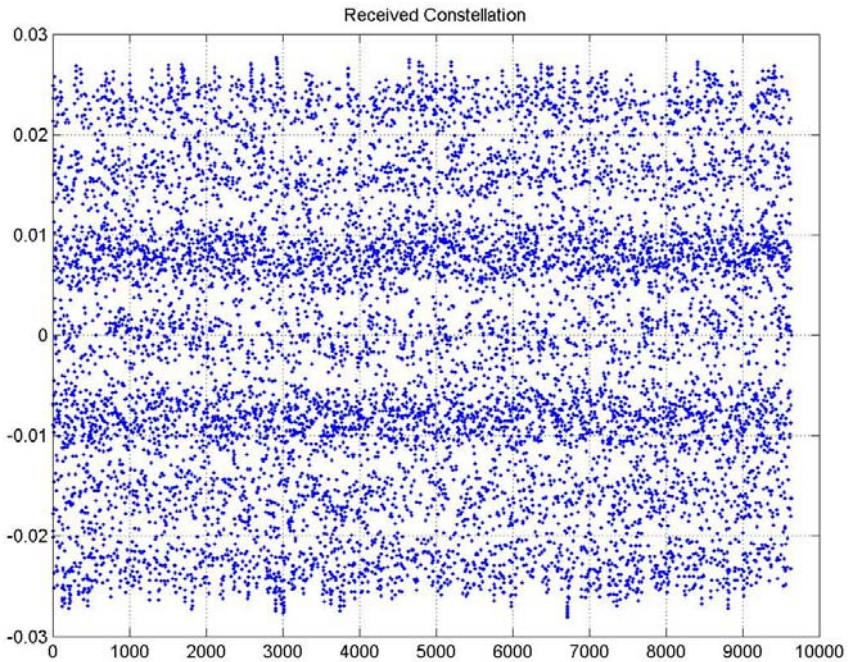


Precursors reduced

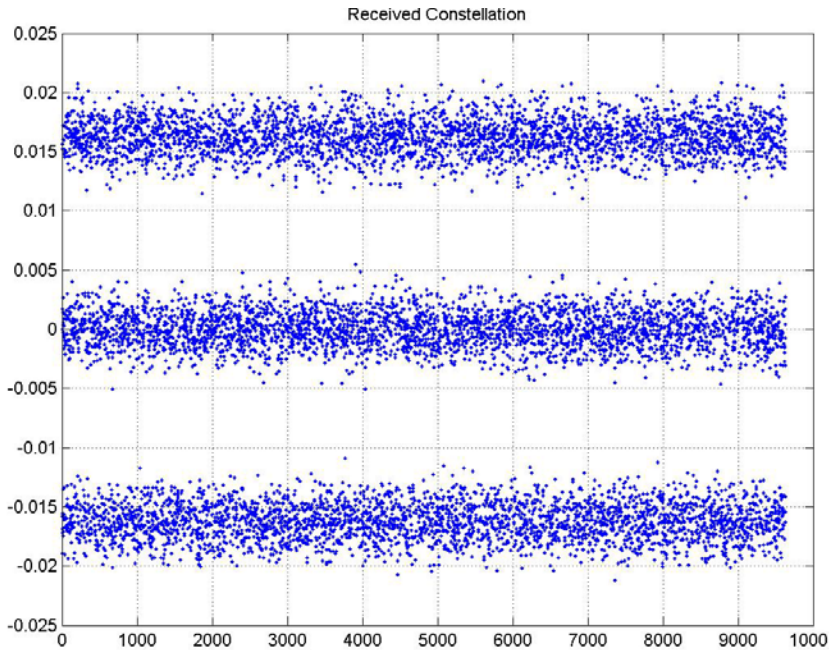
- ✓ Reduces dynamic range of signal at the ADC
- ✓ No noise enhancement
  - small power enhancement
- ✓ Opens eye at t=0 to permit decision directed startup
- ✓ Adds small negative precursor to assist timing recovery

Precursor Pre-equalized Channel at Start-up *(reduced constellation)*

No Precursor Pre-equalization



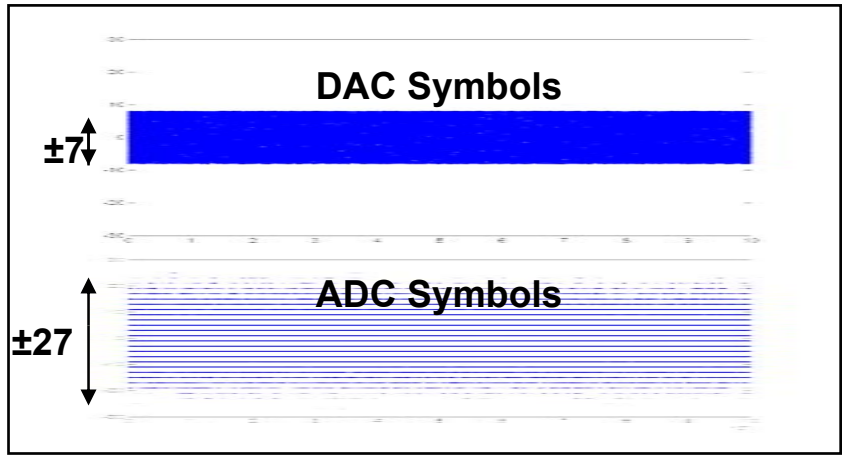
With Precursor Pre-equalization



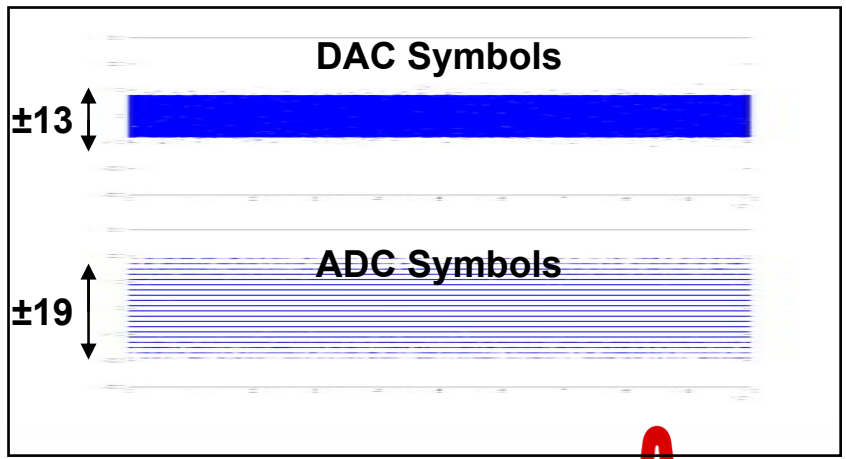
- **Precursor pre-equalization permits simple decision directed start-up**
  - Blind start-up not necessary

DLP Permits Tradeoff Between DAC Complexity and ADC Complexity

- **Conventional THP**
  - RX dynamic range unconstrained
  - ADC more complex than DAC



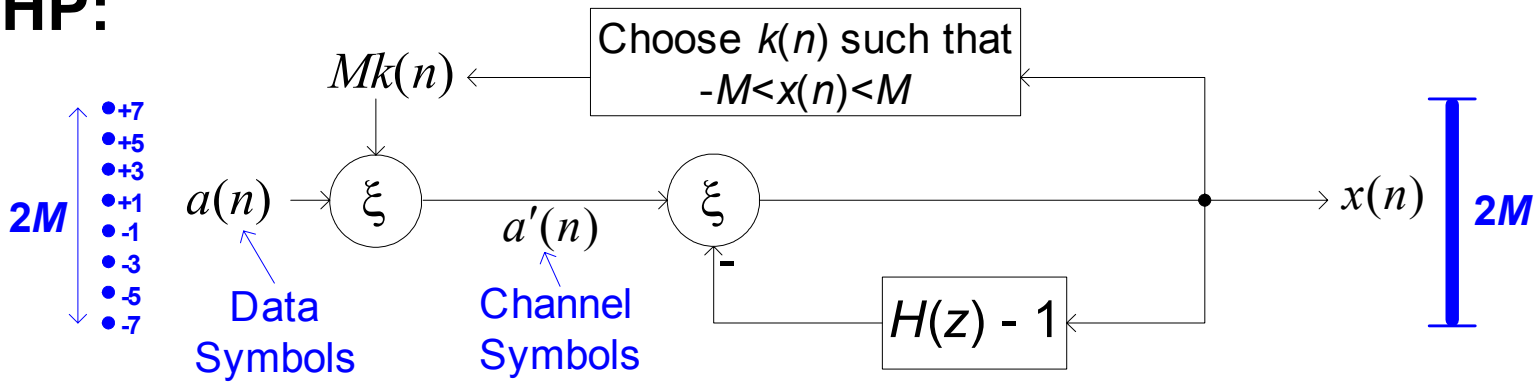
- **Dynamics Limited Precoding (DLP)***
  - RX dynamic range constrained
  - Balanced ADC and DAC complexity



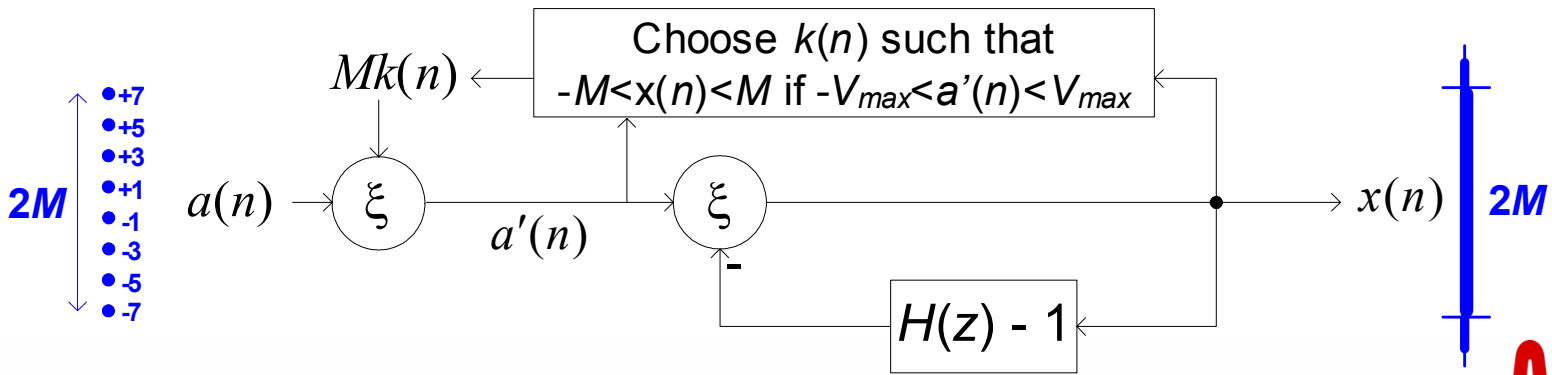
* Fischer, Gerstacker, Huber, "Dynamics Limited Precoding, Shaping, and Blind Equalization for Fast Digital Transmission over Twisted Pair Lines," IEEE JSAC, Dec 1995

DLP: A Simple Modification to THP

- **THP:**



- **DLP:**



Proposed Precoder Features

- **IIR Channel Model**

$$H(z) = \frac{\left(1 - z^{-1}\right)\left(1 + \delta z^{-1}\right)}{1 - \alpha z^{-1} + \beta z^{-2}}$$

- **Transmit filter**

$$T(z) = \left(1 + az + bz^2 + cz^3\right)z^{-3}$$

- **Stationary parameter values**
  - At startup, cable length is determined and used to select precoder coefficients from a ROM

- **Dynamics limited precoding**

Precoder Rationale

1) Why precoding vs DFSE ?

- Decouples DFE and decoder
- Permits more powerful coding
- Simplifies timing closure
- No error propagation

2) Why IIR precoder ?

- Reduced complexity

3) Why compromise precoding ?

- Eliminates need for back channel
- Makes IIR practical

4) Why precursor pre-equalization ?

- Simplifies start-up sequence
- No noise enhancement
- Reduced ADC complexity

5) Why dynamics limited precoding ?

- Reduced dynamic range at ADC input

Precoding vs DFSE: Disadvantages

- **Expanded constellation at receiver**
  - However:

w/o precoding		Precoding
signal + ISI	≈	signal + expanded levels

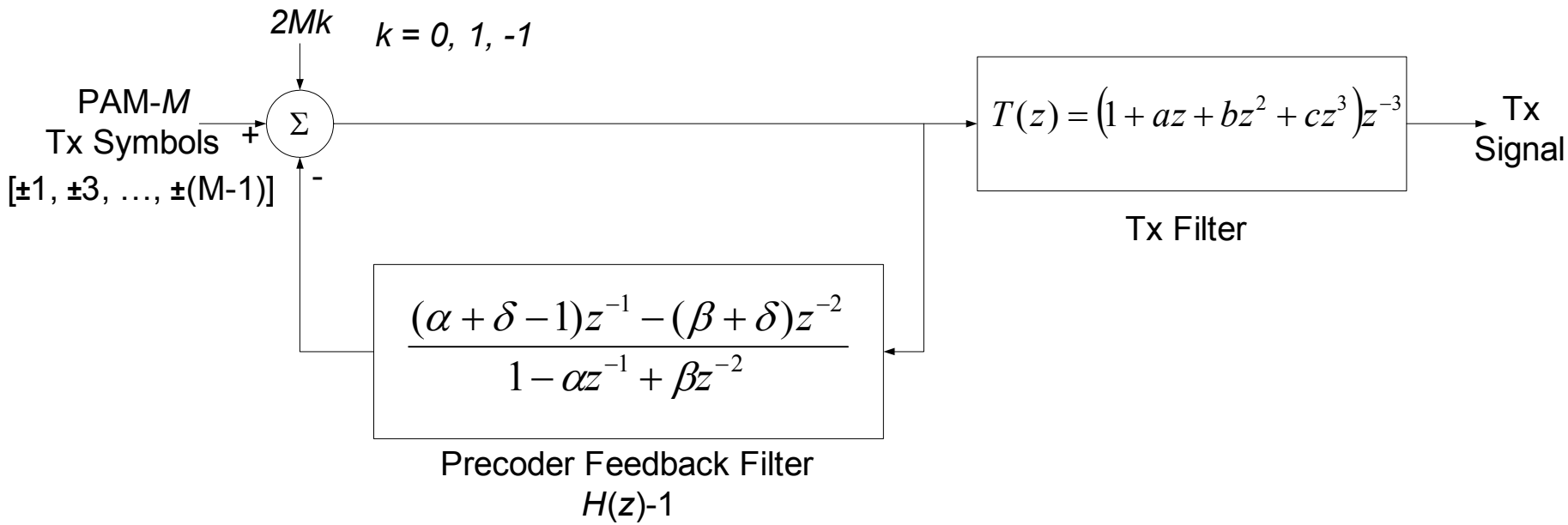
Not a real disadvantage

- **Increased transmit DAC complexity**
  - M-level DAC → multi-bit DAC
- **Power enhancement from Tx pre-equalizer**
  - Approx equivalent to noise enhancement if moved to Rx
- **Not a direct sub/super-set of 1000BT**
  - Enough similarities to permit resource sharing

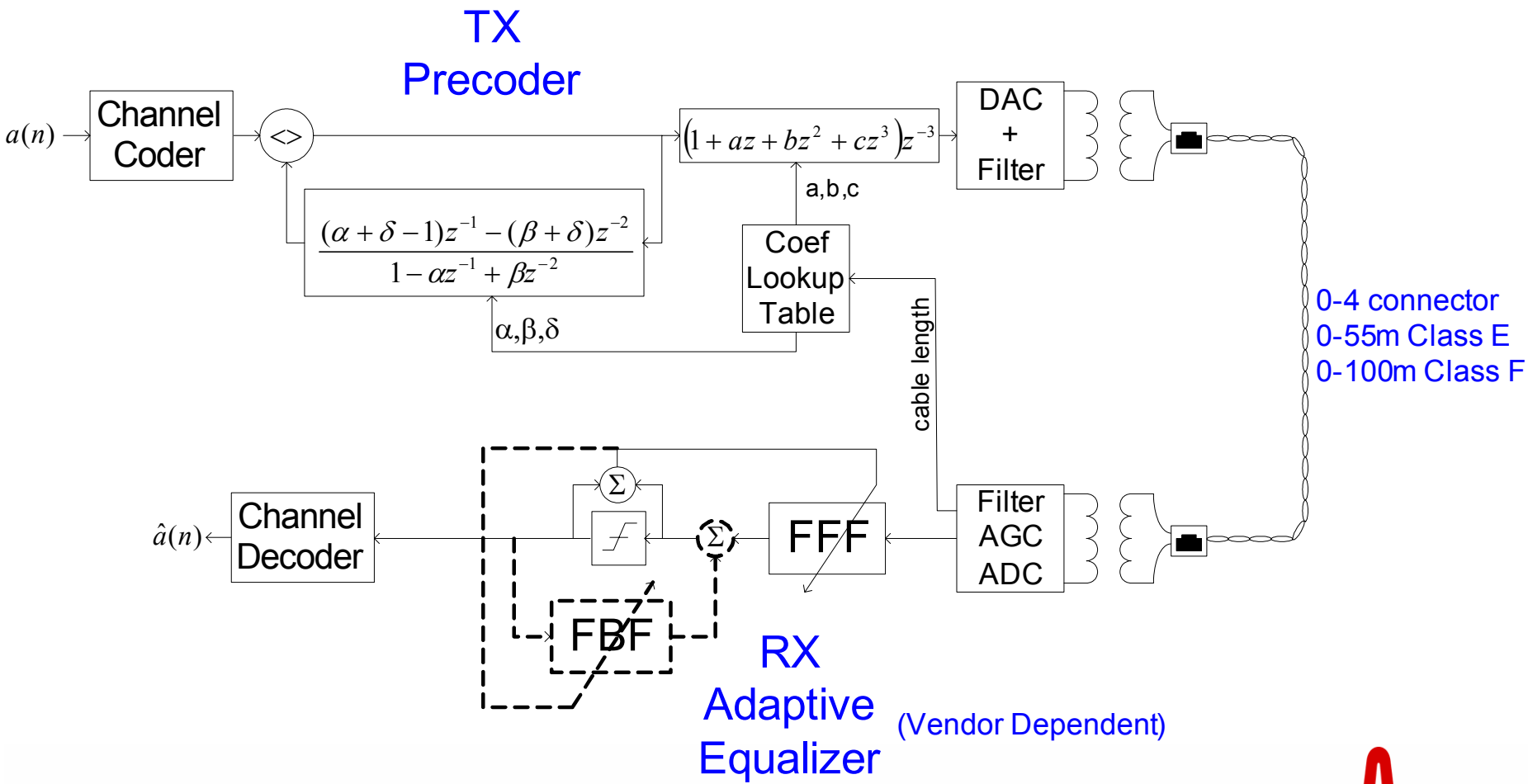
Not a real disadvantage

Proposed Precoder

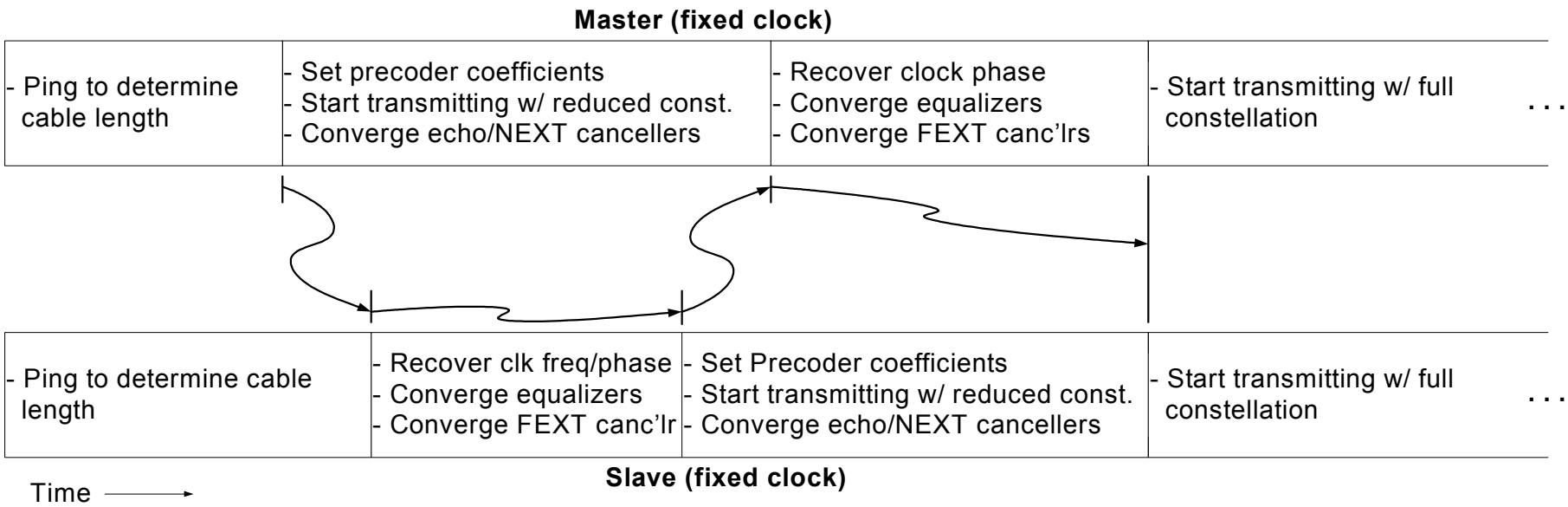
- **Dynamics limited compromise IIR precoder with precursor equalization**
  - $\alpha,\beta,\delta,a,b,c$ vs cable length pre-stored in look-up table



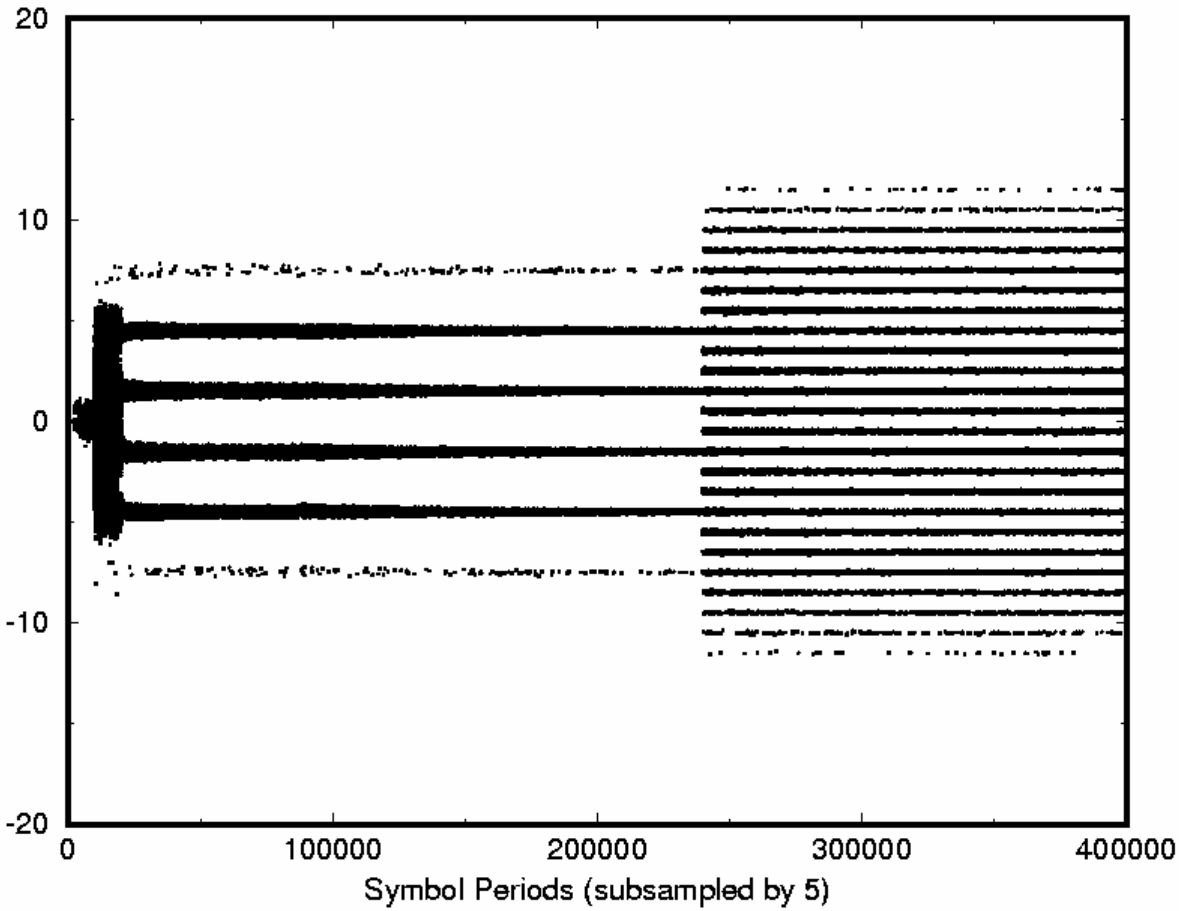
Overall System (1 wire)



Start-up Protocol Similar to 1G



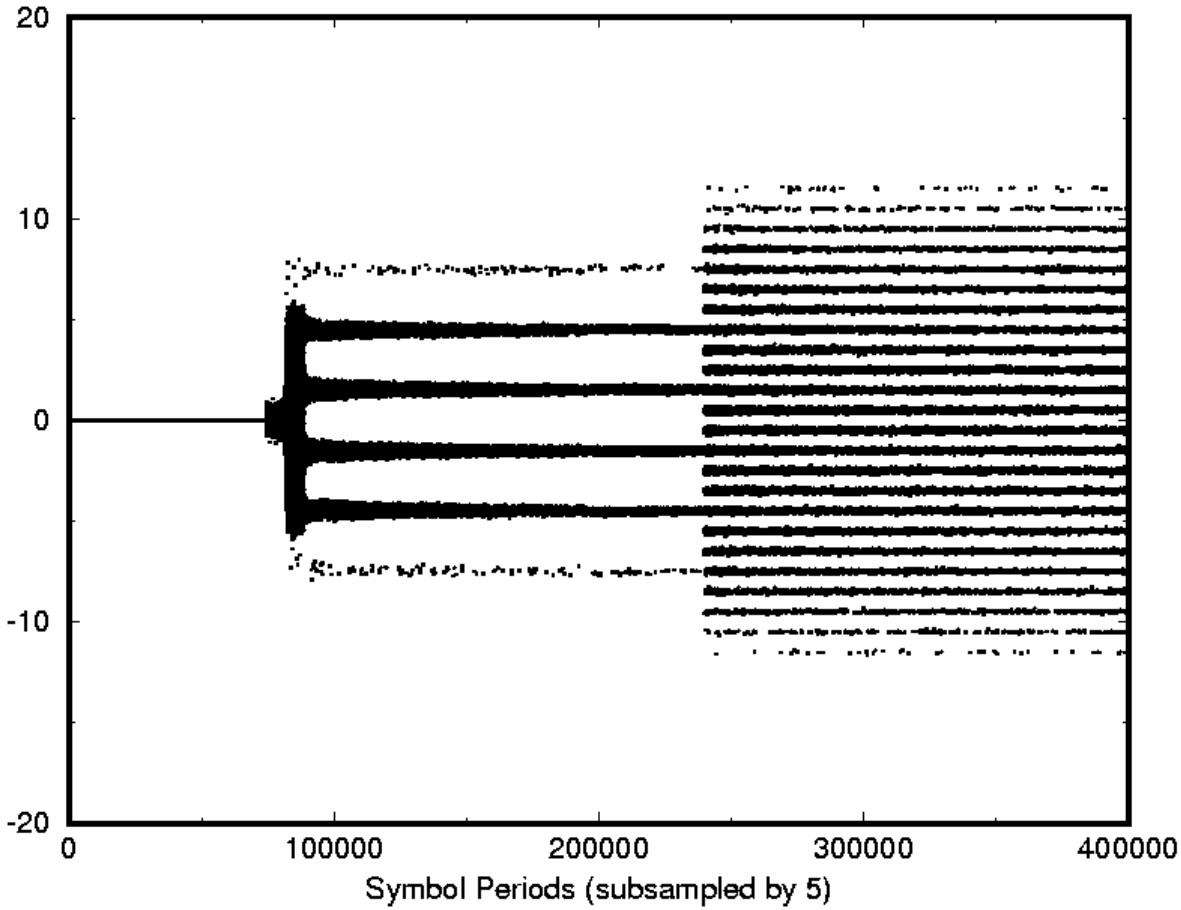
Eye Pattern at the Slave (PAM-8)



SNR at the Slicer=35dB

Ideal Conditions, only for the purpose of discussing the precoder and the startup protocol
Not an indication of the performance to expect from a real receiver

Eye Pattern at the Master (PAM-8)



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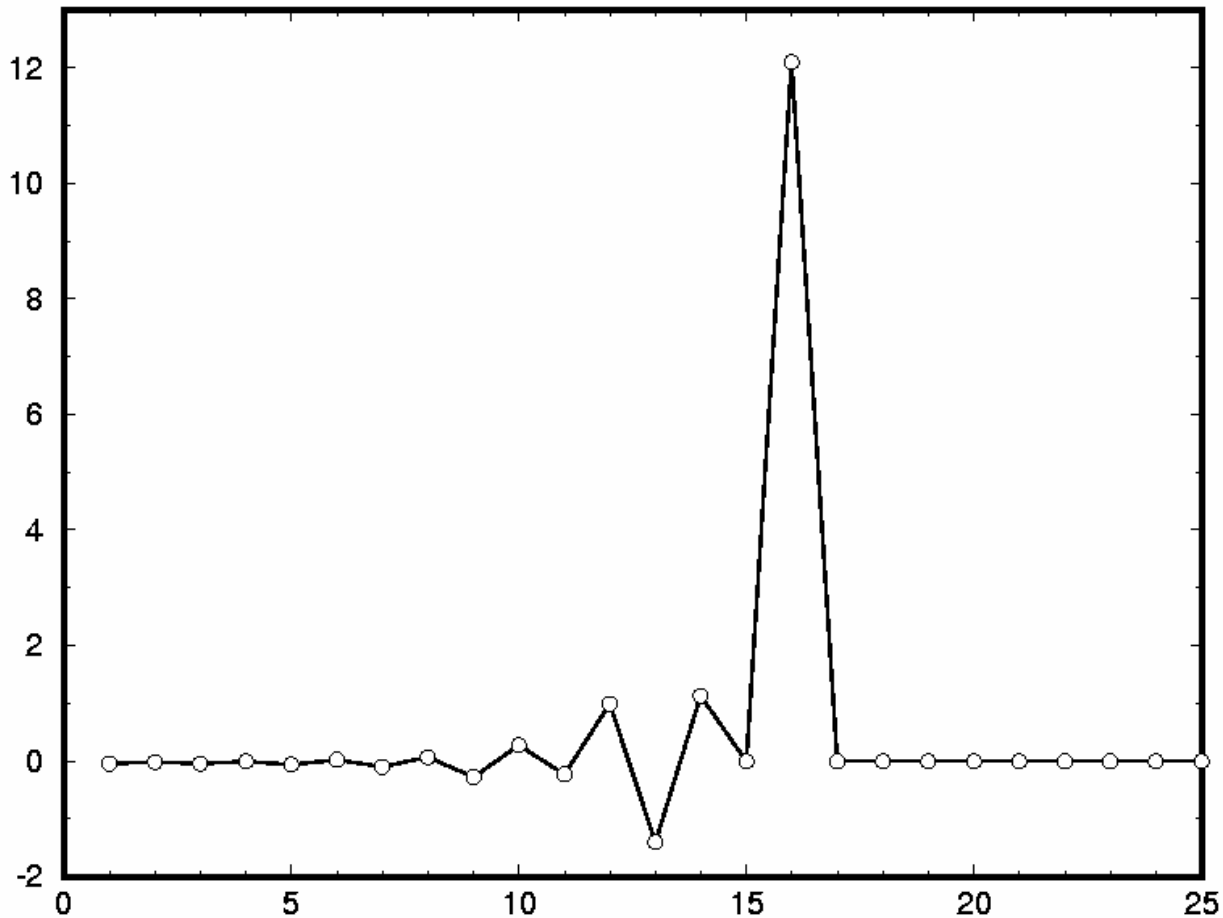
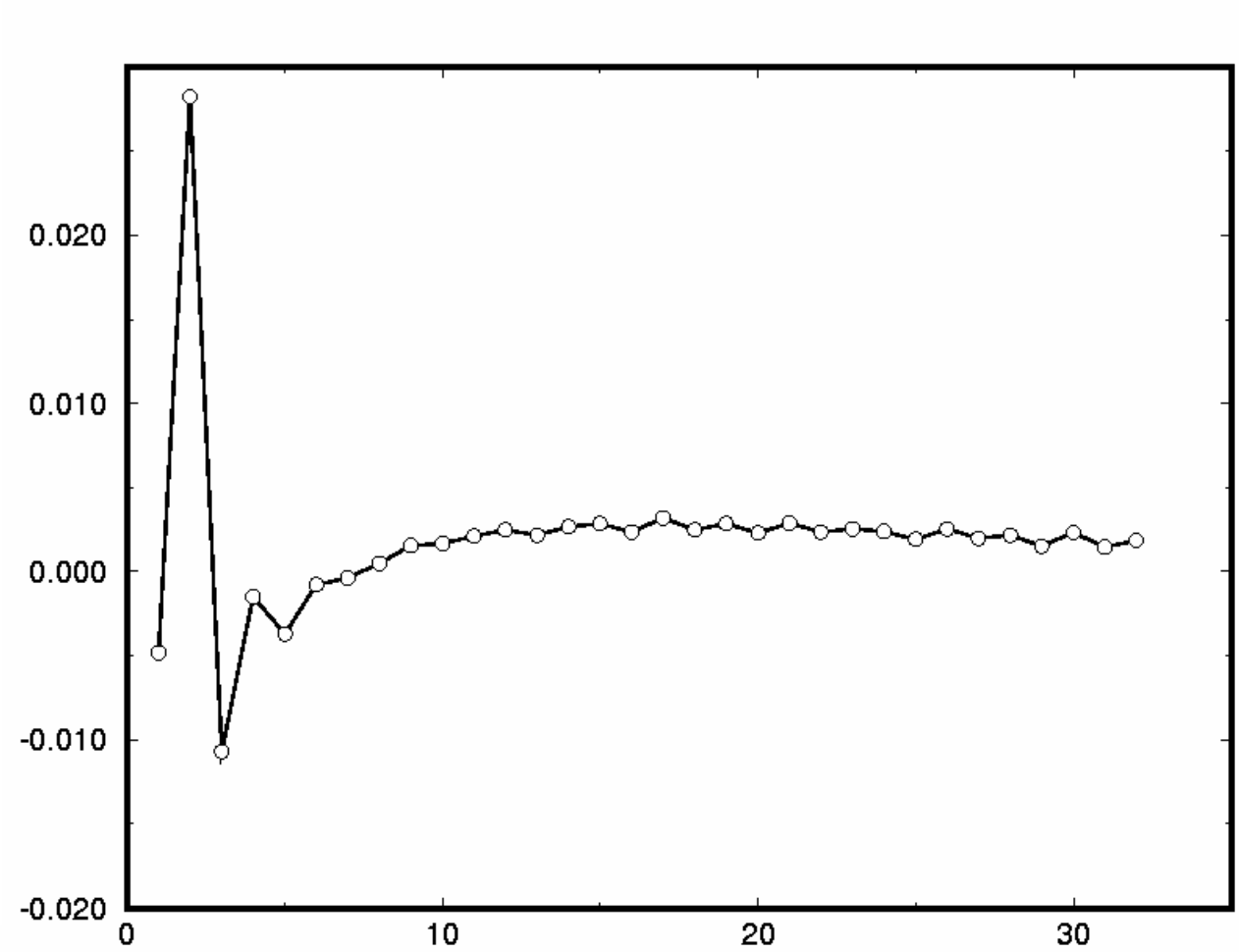
FFE Coefficients



Good matching of the precoder to the channel means small FFE coefficients => low noise enhancement

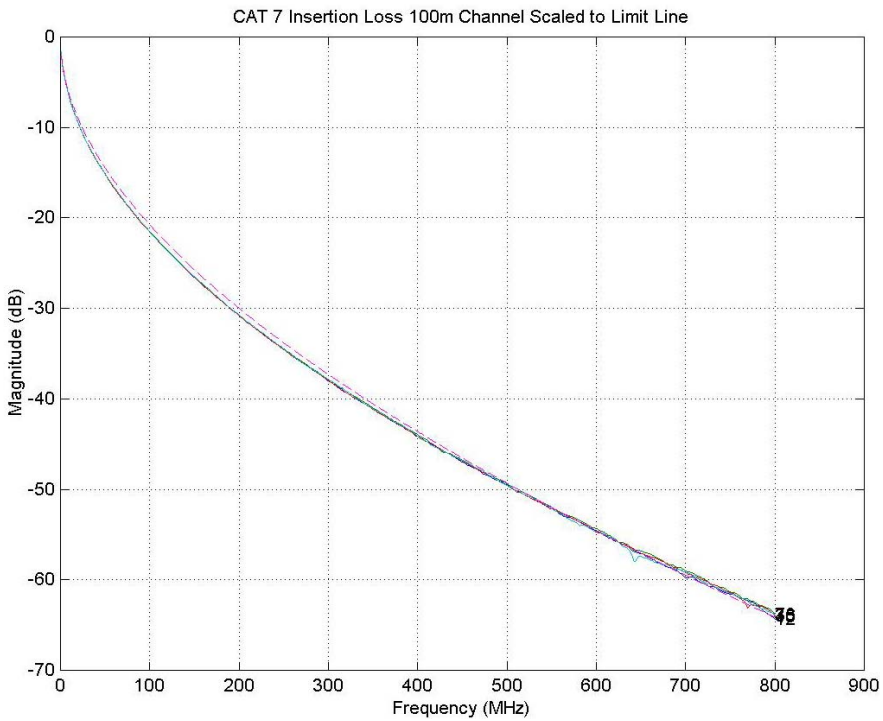
DFE Coefficients

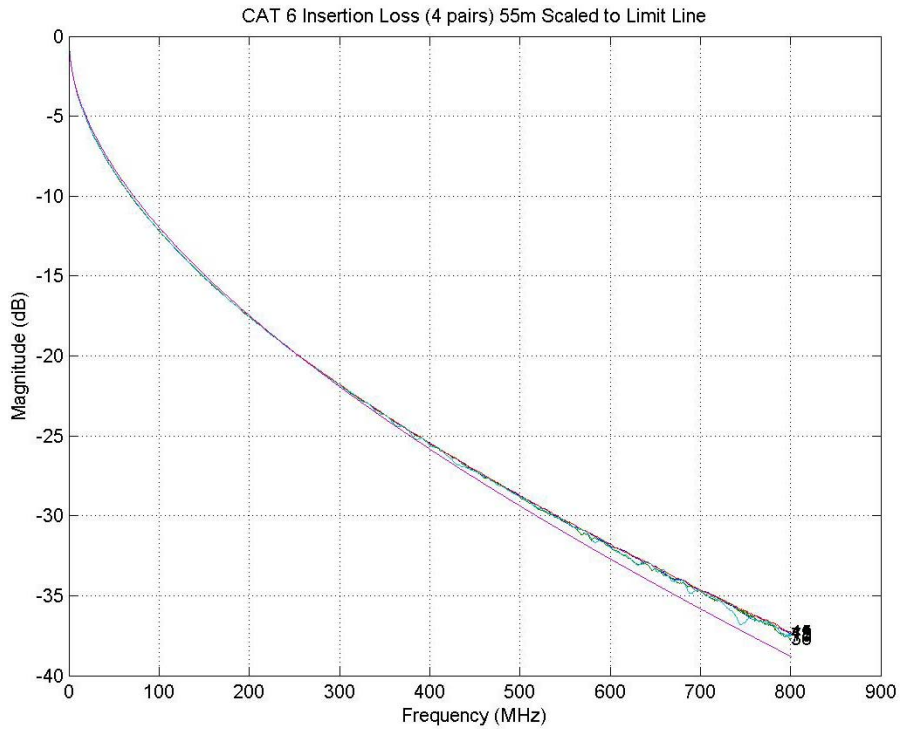


Good matching of the precoder to the channel means small DFE coefficients => low error propagation

System Simulation Channel Models

- 100m scaled Cat 7 model
- 55m scaled Cat 6 model



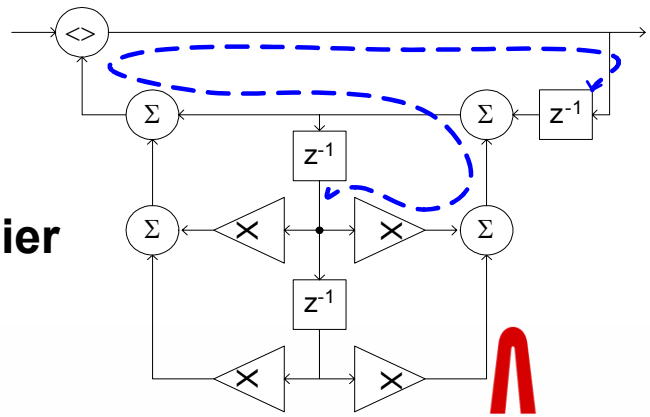


- Measured data linearly scaled (in dB) to touch limit line at maximum rated bandwidth

Open Issues for Further Investigation

- **Cable length (or insertion loss) determination**
- **Tabulation of precoder filter parameters**
  - Evaluation of sensitivity
- **Amount of Rx dynamic limiting (DLP)**
  - Tx power vs Rx complexity tradeoff
- **Precoder worst case timing path**
  - Several possibilities to improve

1 multiplier
4 adders



Conclusions

- **Precoding permits more powerful channel codes**
  - Removes decoding operation from the DFE feedback loop
- **An IIR precoder is well matched to UTP channels**
  - Order of magnitude fewer coefficients than FIR
  - Well known parallel processing techniques can be applied to the precoder
- **Precoder adaptation not necessary with short RX equalizer**
  - Coefficients can be set at startup from a LUT based on cable length
- **Use of DLP and transmit filtering allows tradeoffs between complexity of the ADC and DAC**