A Low Power / Low Latency 10G AFE In CMOS

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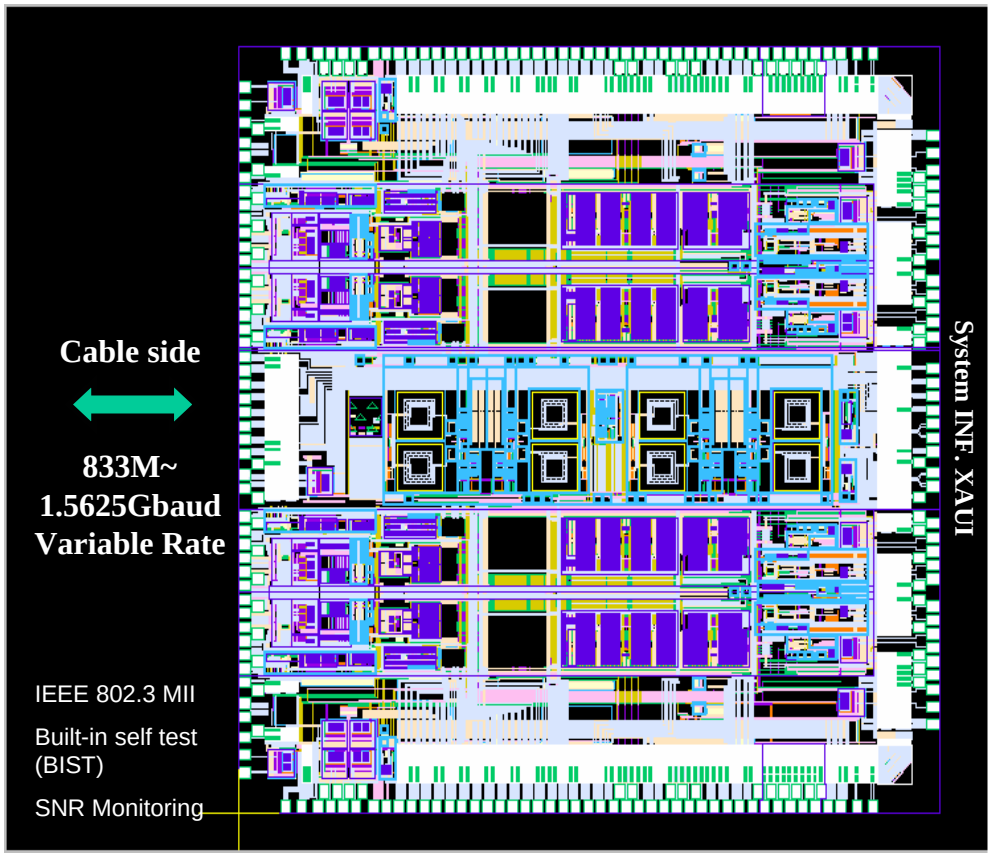
KEYEYE COMMUNICATIONS

Low Power, 380mW / CH



Channel Power	
Transmitter	130mW
Receiver Line-up	120mW
Analog FIR	100mW
PLL	30mW
	380mW
X 4 =	1.52W
VCO and Others	140mW
Total (4 Channels)	1.66W

(1.56G baud Mode)

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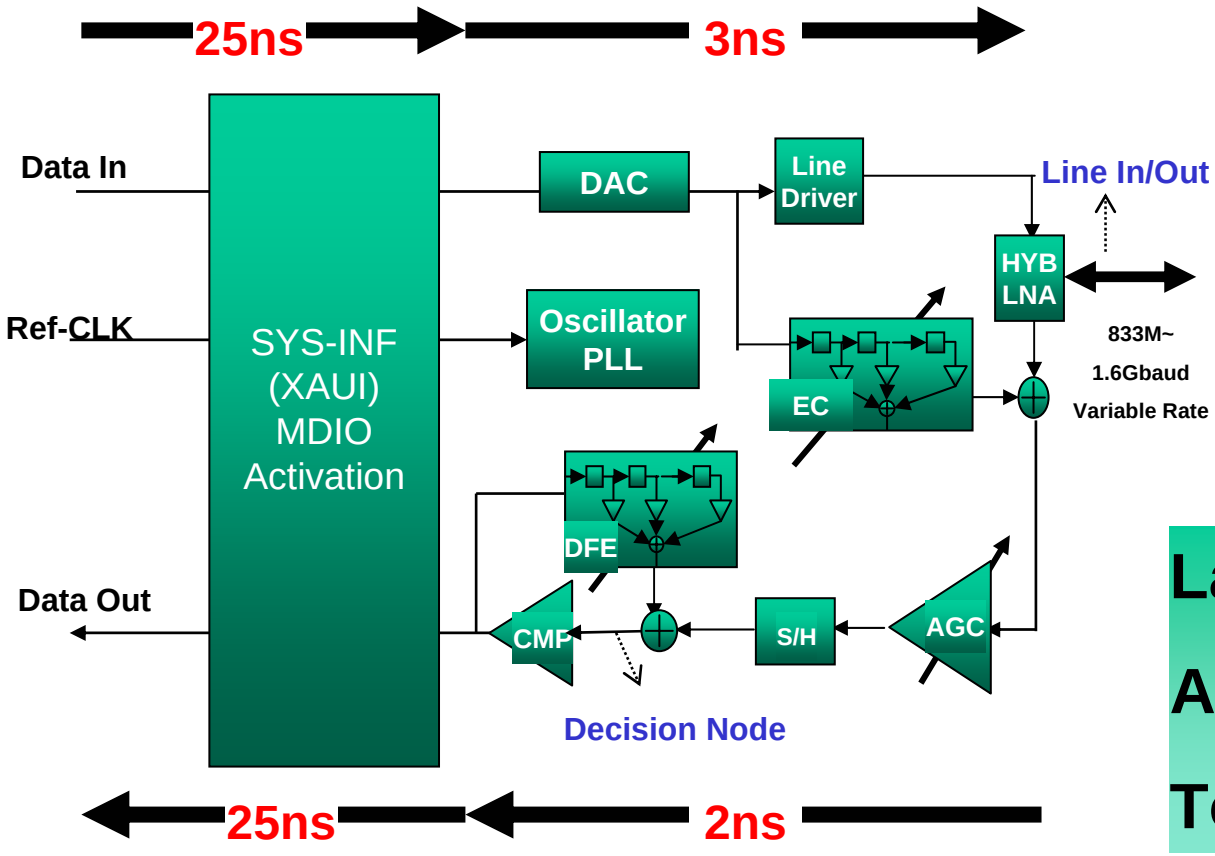
Low Latency

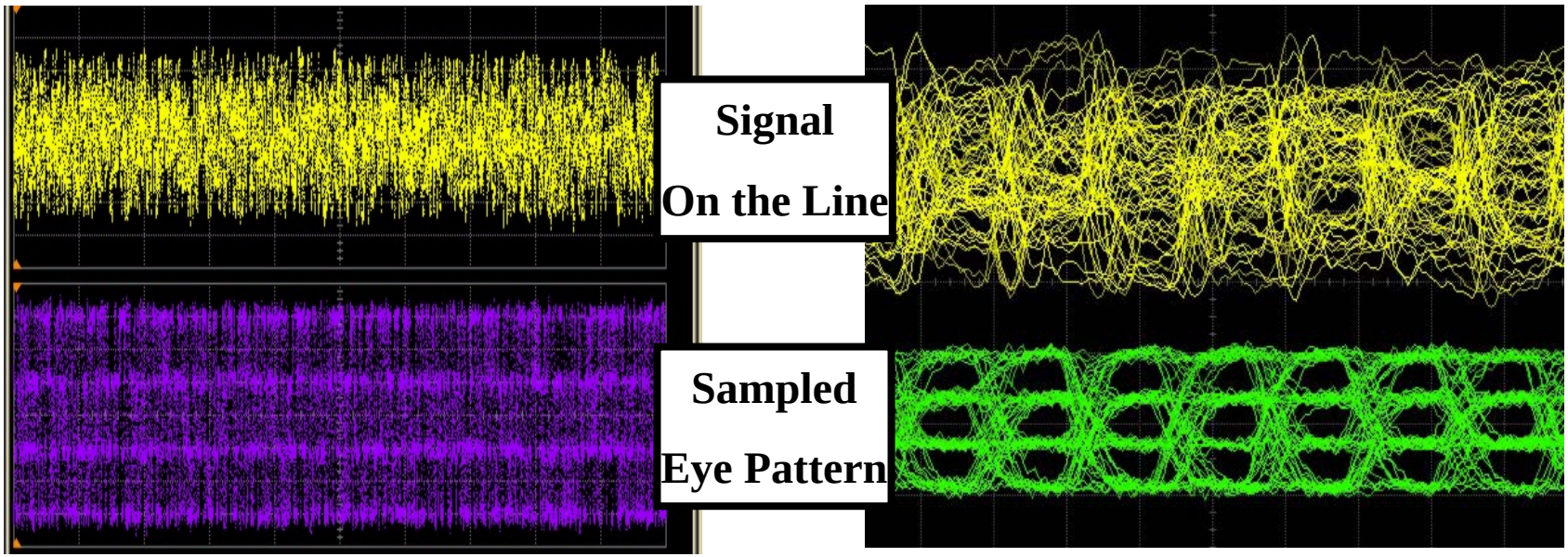


Latency:

AFE Only	**5ns**
Total Txcr	**55ns**

1.56GBaud Mode

Captured Waveforms



4PAM Eye Pattern, 1.56G Baud

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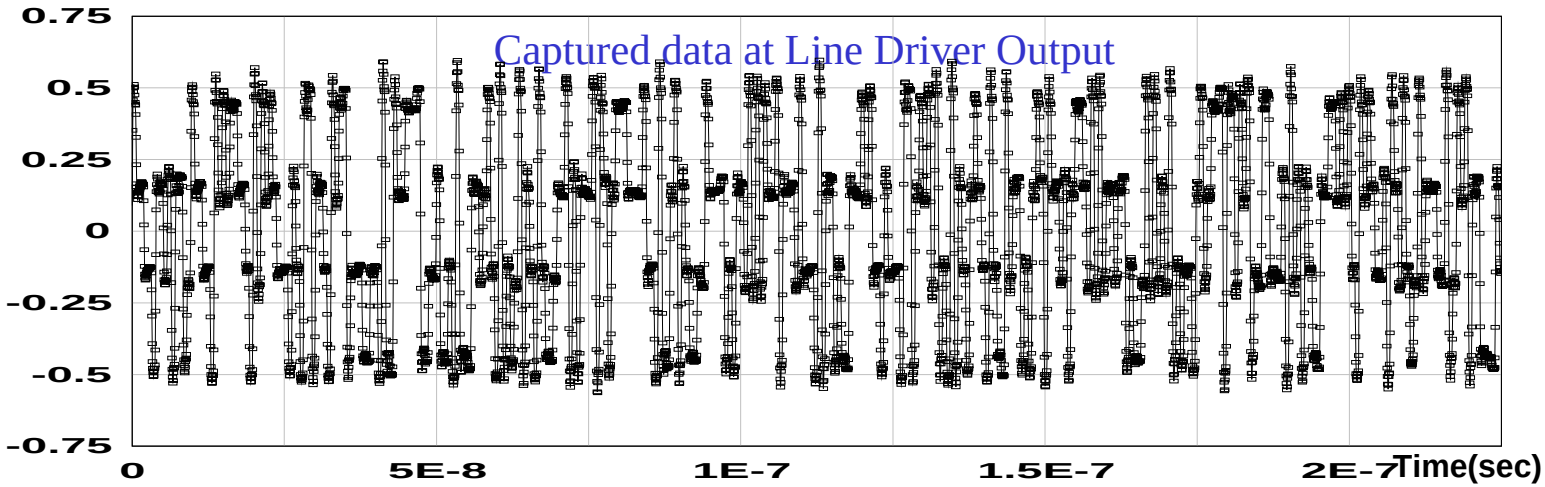
Key Elements of A High Performance AFE

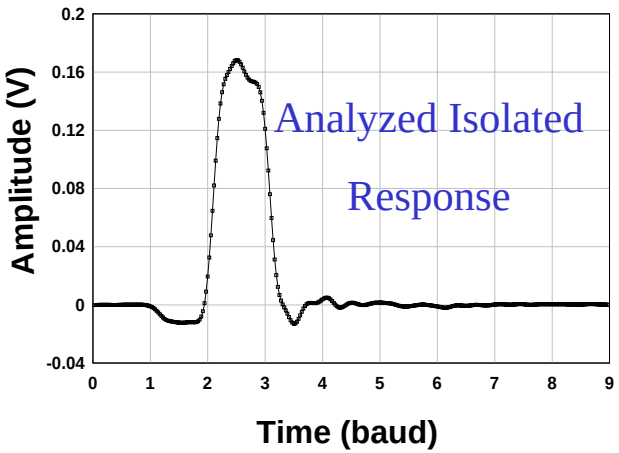
- Highly Linear Line Driver / Hybrid
- Analog Pre-Echo Canceller (Adaptive FIR) Pre-Processing, Low Noise Floor
- Fine Resolution Comparator / ADC
- Low Jitter Oscillator

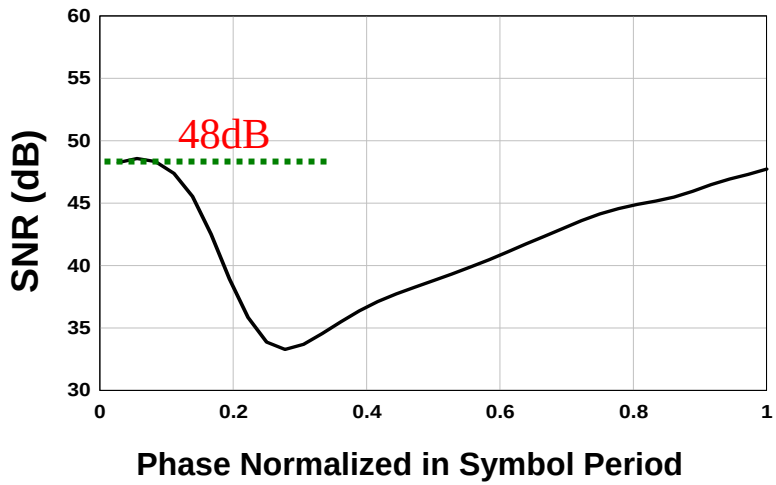
Measured Results:

833M baud Mode

Line Driver With 48dB of Linearity







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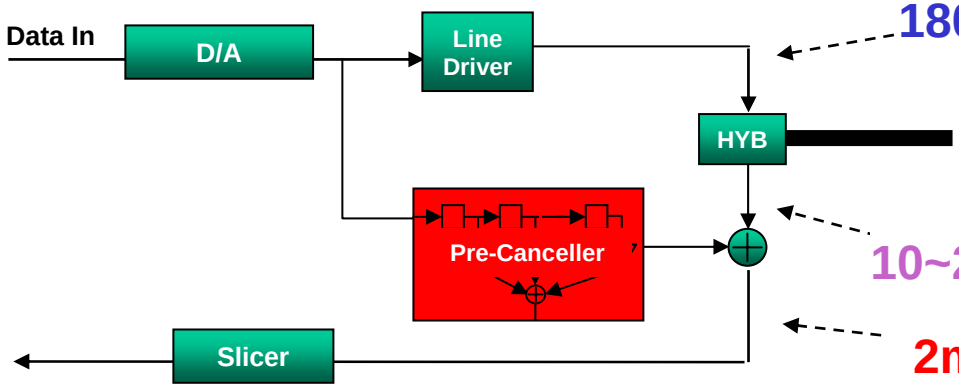
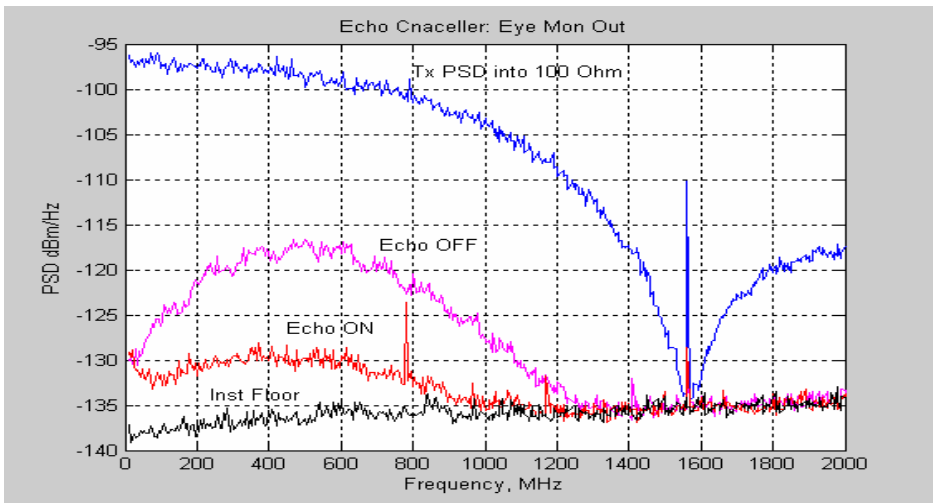
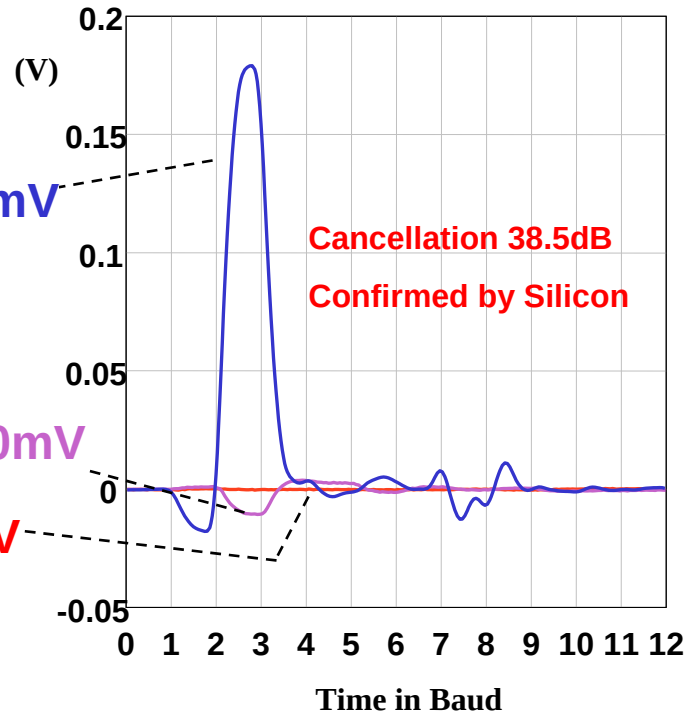
Measured Results:

Analog Pre-Echo Canceller (Adaptive FIR)







Analog Pre-Echo Canceller gains 10~20dB

At least 2 bit Reduction of ENOB for A/D Requirement

Noise Floor 130~-140dBm/Hz

2mV Comparator Resolution

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Measured Results:
Oscillator Jitter

Jitter < 3ps

from –5 to 85 deg.C

Jitter Requirement

from previously presented papers

4ps (Broadcom, Vativ, Marvel)

3ps (NEC Electronics)

6ps (SolarFlare)

Temp. Coef = 0.008ps/deg

Measured from –5 to 85 degC

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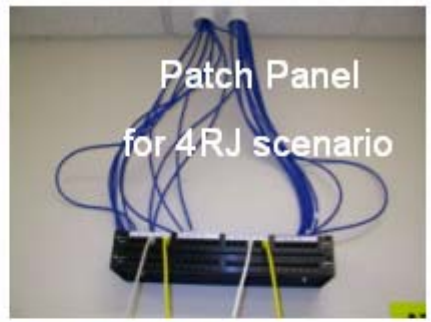
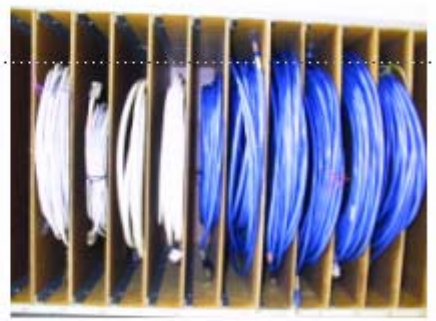
Measured Results:

Reach Performance





Cables for 2RJ scenario

Error Free Reach	Full Duplex	35m
	Simplex	50m

Summary

- Highly Liner (48dB) Line Driver
- 38dB Cancellation by Analog Pre-Echo Canceller
- Fine Resolution Comparator / ADC
- Less than 3ps Jitter from –5 to 85degC
- Power Consumption: 380mW / Channel
- Latency: 5ns(AFE Core) and 55ns including Scrambler / De-Scrambler and SYS-INF.

A Low Power / Low Latency AFE at 833M up to 1.6G baud has been proven in silicon