On Loop Timing and 10GBASE-T

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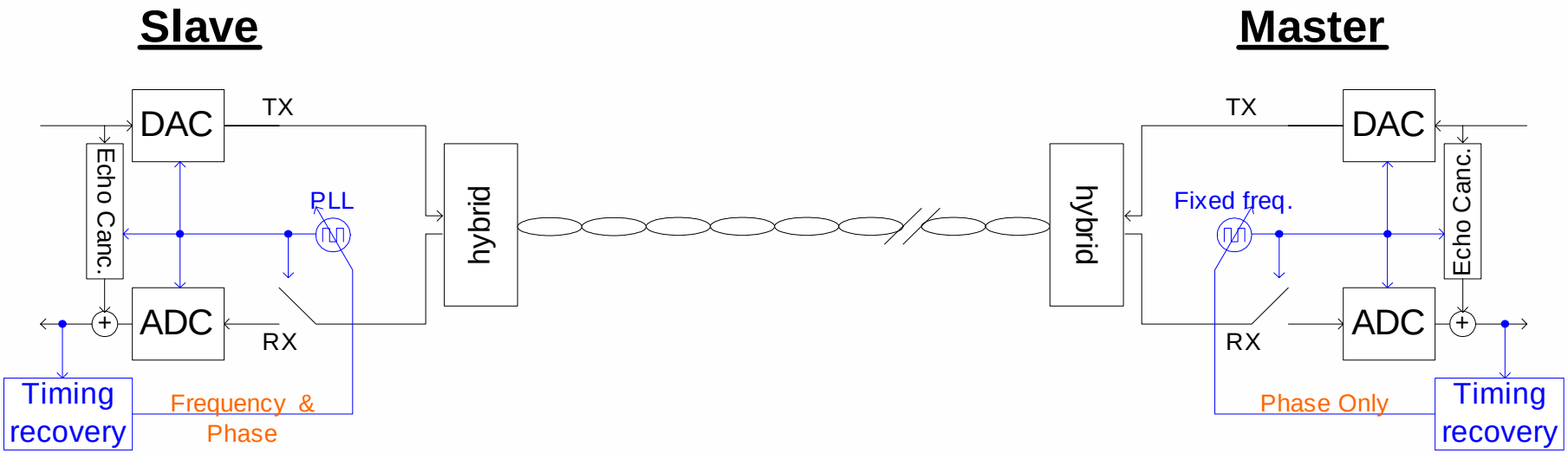
Loop Timing

- Echo & NEXT cancellation generally require the transmitter and receiver to be clocked from the same source



- Master side driven from a fixed frequency clock
- Slave side recovers clock from Master
  - Transmits with recovered clock

4-Channel Loop Timing Implementation Challenges

- See powell_1_0904.pdf for details
- Each channel requires independently controlled phase
  - Multiple VCO's have interaction difficulties
  - Phase selectors require large number of phases for 50dB+ echo suppression
- Analog PLL loop delay restricts FFE implementation options
  - FFE delay inside loop
  - Stability and loop bandwidth considerations

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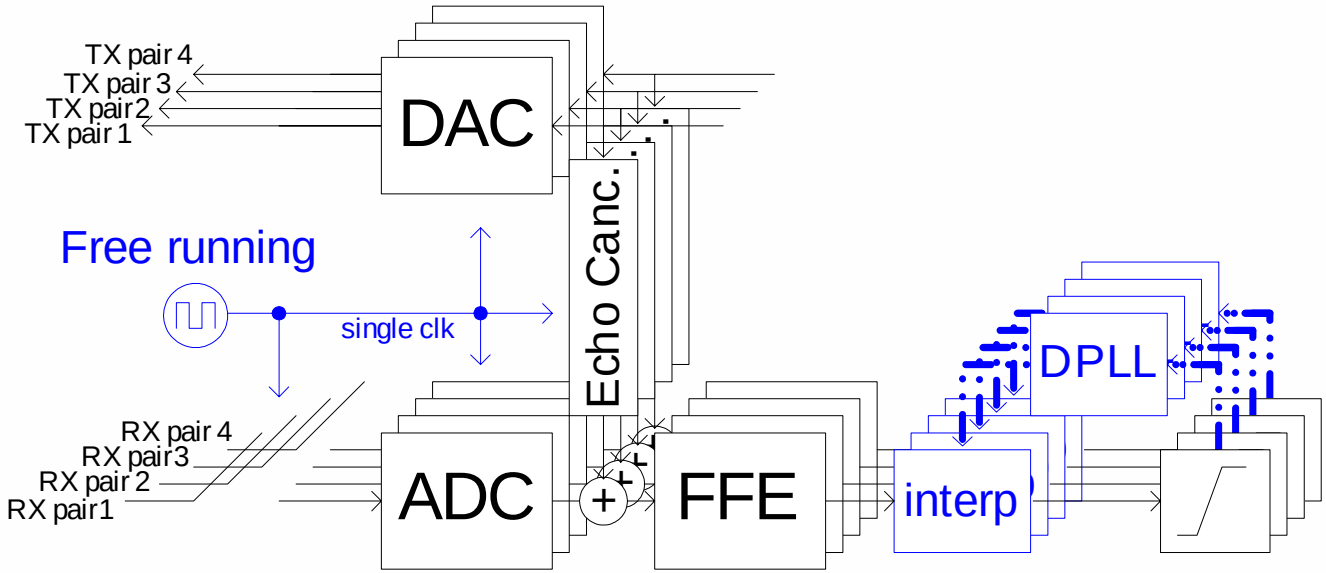
Alternative to Loop Timing

- Move timing recovery after FFE
  - Digital interpolator instead of analog VCO or phase selector



  - Analog PLL per channel not required
  - Removes requirement for large phase selector
  - Single clock for all 4 channels

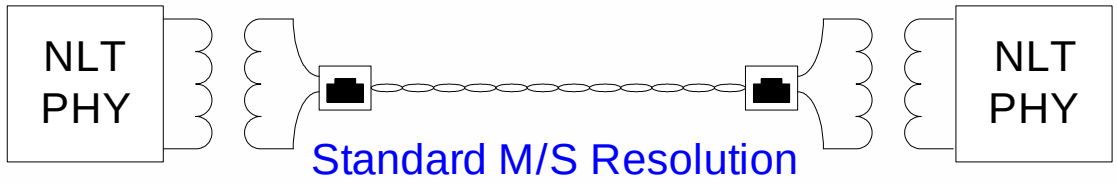
Making Loop Timing Optional

- Loop timing capability is advertised on the 10GBASE-T abilities page during autonegotiation
- Standard can accommodate both loop timed (LT) and non-loop timed (NLT) PHYs
  - Proper assignment of master and slave ends
- Simple algorithm
  - If both ends are of the same type: use standard m/s resolution
  - Otherwise: LT end is force slave and NLT end is force master

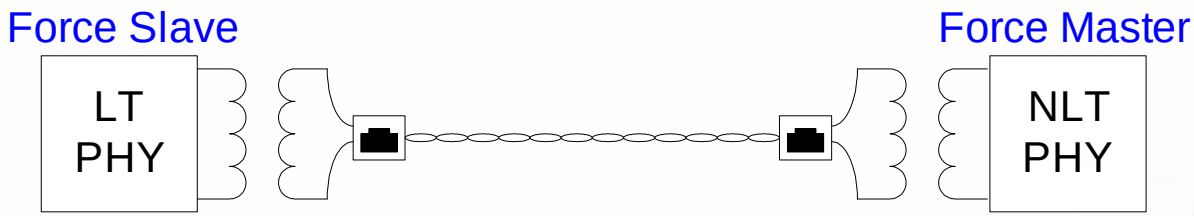
Assignment of Master and Slave

Case I

Case II



Case III



Proposal Summary

- Advertise loop timing ability as part of autonegotiation
  - Utilize “gigabit” master/slave resolution if abilities match
  - Force assignment of master and slave if abilities differ
- Permits PHY vendors flexibility in timing recovery implementation
  - Traditional “gigabit” loop timing approach works without modification
  - All-digital approaches can be implemented

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