800Ms/s PHY for 10GBASE-T: Coding, Framing, Mapping

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Agenda

- **Resolved Technical issues in the 802.3an Task Force**
- **Outstanding Technical issues in the 802.3an Task Force**
  - Meeting requirements on False Packet Acceptance Rate
  - Robustness (EMI susceptibility on existing cables)
- **Proposed Coding, Framing, Mapping for 800Ms/s 10GBASE-T PHY**
  - Achieving robust EMI susceptibility
  - LDPC Code selection
  - Simulation results

Resolved Technical Issues

- **800Ms/s Pulse Amplitude Modulation (PAM) Signaling**
- **Low Density Parity Check (LDPC) Error Correction Coding with two potential options:**
  - 1024 block-length family of Reed Solomon based Djurdjevic LDPC codes
  - 2048 block-length family of Reed Solomon based Djurdjevic LDPC codes
- **Tomlinson-Harashima Pre-coding**
  - Pre-coder fixed during startup, with a small number of settings

Outstanding Technical Issues

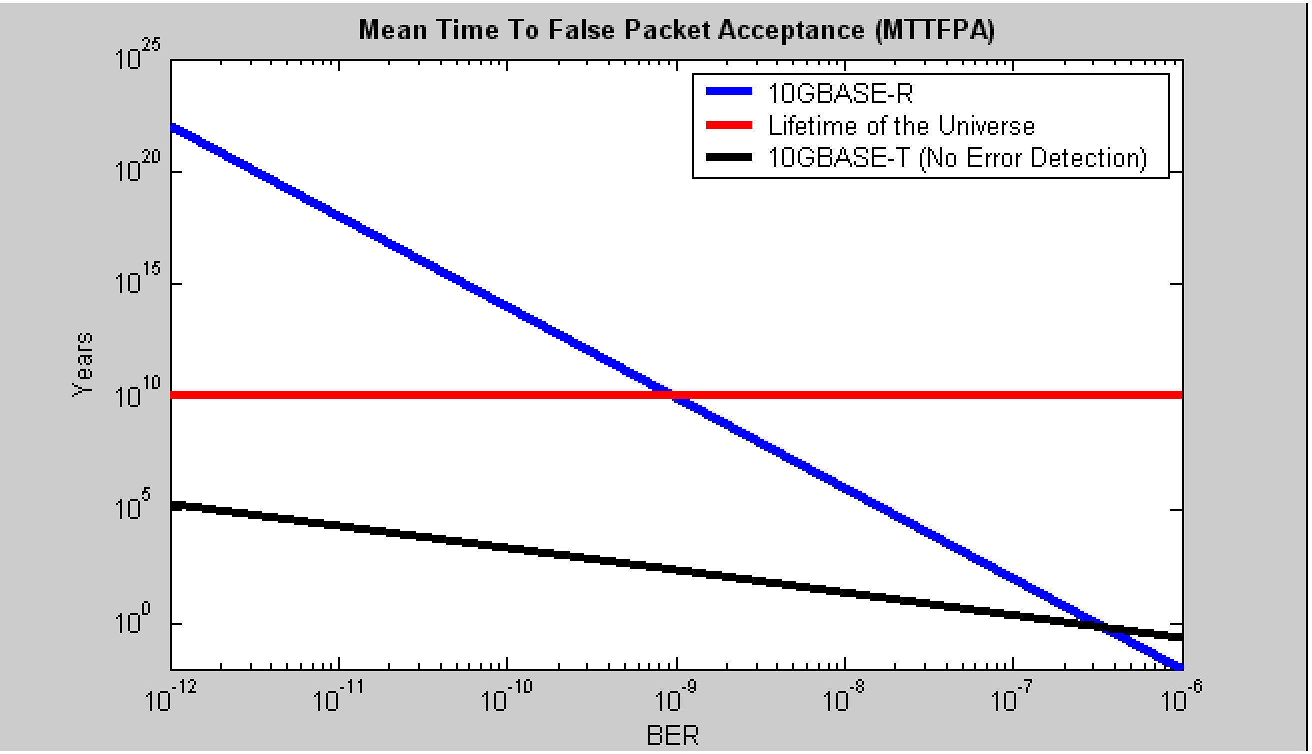
- **Analyze the effect of burst errors on the False Packet Acceptance Rate at the receiver**
  - Determine additional error detection capability required to meet Ethernet goals
- **How to deal with 20+ dB increase in EMI penalty with respect to 1000BASE-T?**
- **Coding, Framing, Mapping**
  - What block length and rate of LDPC code?
  - What bit-to-symbol mapping to use?

False Packet Acceptance Rate

- **If a damaged packet is accepted as valid, this has the potential to hard crash a computer system (walker_1_0300.pdf, slide 7).**
  - In past Ethernet standards, Mean Time to False Packet Acceptance (MTTFPA) was designed to be > several tens of billions of years to mitigate the occurrence of such problems over millions of Ethernet node deployments. GbE achieved 60billion years.
- **For 10GBASE-T systems with LDPC block codes, errors occur in bursts.**
  - Conservative assumption: every such error burst is undetected by the error correcting code that produced it. This assumption is reasonable for 1E-12 BER since such errors don't appear often in simulations.
  - Conservative assumption: probability that the 64B/65B code detects these error bursts is 0.
- **Probability of a single bit error = Desired BER / Expected Burst Length = $P_S = (P_E / B_L)$**
- **Probability of a burst error occurrence in a packet of length L bits is approximately $L*P_S$**
- **Probability that the burst error is undetected by the CRC is $L*P_S*2^{-32}$**

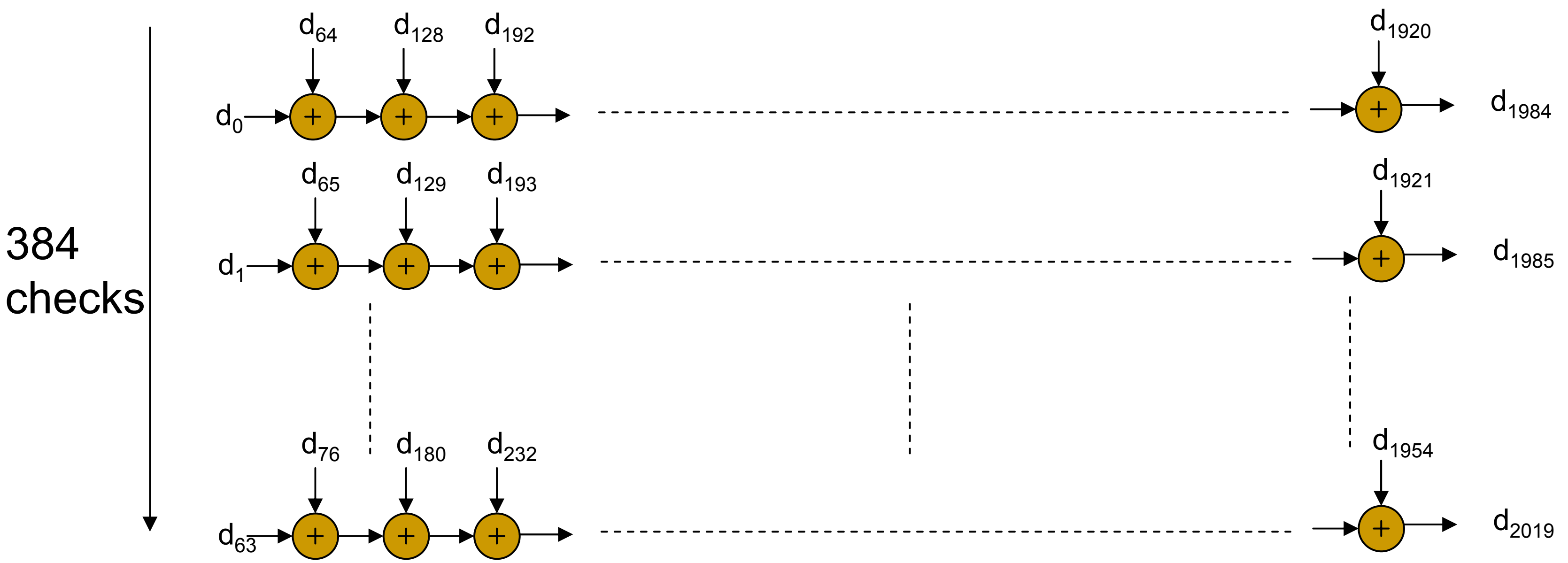
Mean Time to False Packet Acceptance (MTTFPA)

- **Mean Time to False Packet Acceptance (MTTFPA) is**
  - MTTFPA = T_{bit}*L/(L*P_S*2^{-32}) = 218K years for a Mean Burst Error length of 16 bits and a desired BER of 1E-12.



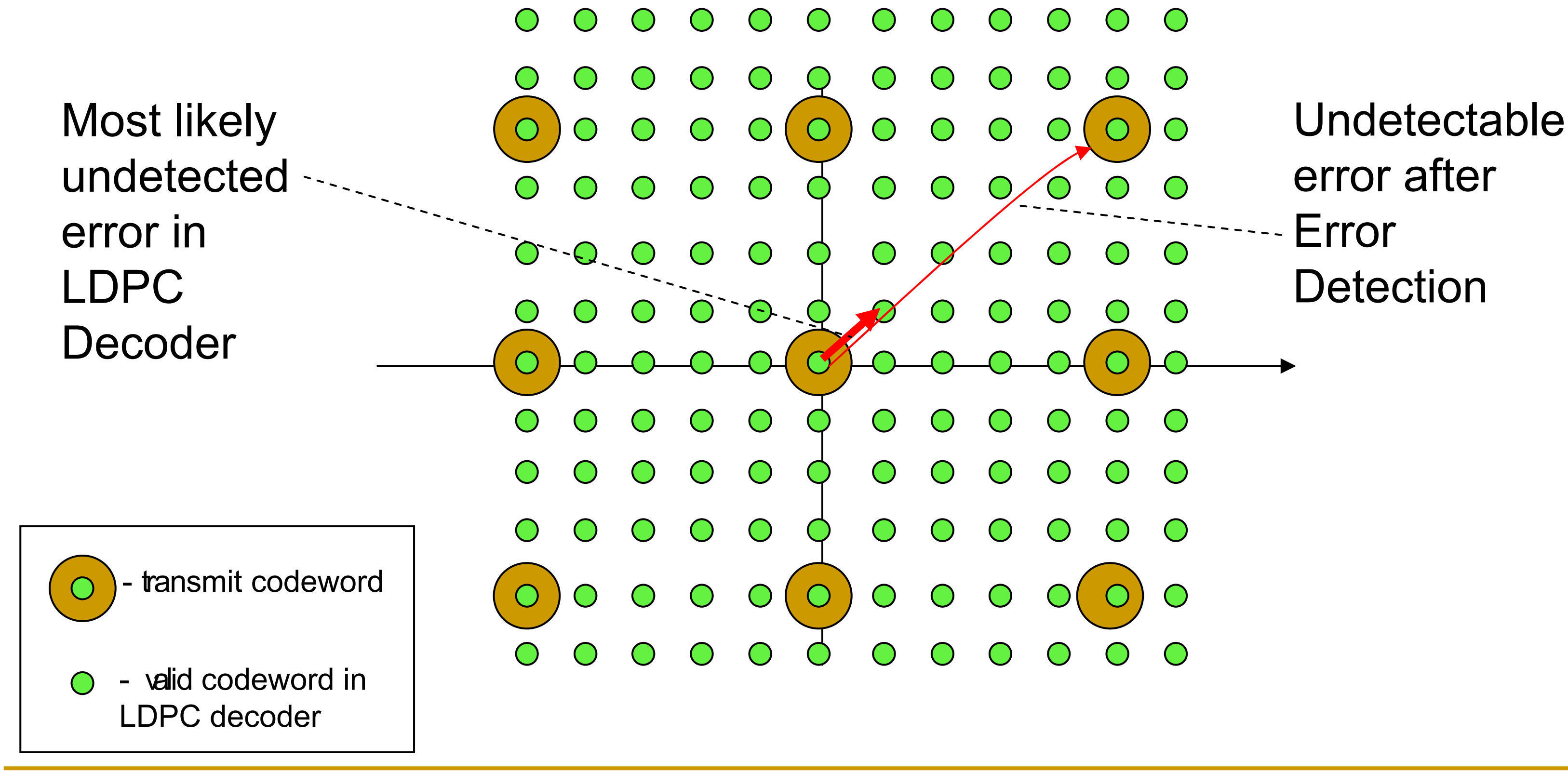
Increasing MTTFPA (General Principle)

- **In a system that uses an Error Correcting code that causes burst error events, reduce the Error Correcting capability of the receiver by a fraction of a dB and use it for Error Detection.**
  - For 10GBASE-T system under consideration, the LDPC Error Correcting code consists of Parity check equations (i.e., CRC-like bits computed with XOR gates!)



Increasing MTTFPA

- **Sufficient number of independent parity check equations from the same layered block code result in robust Error Detection.**



Increasing MTTFPA

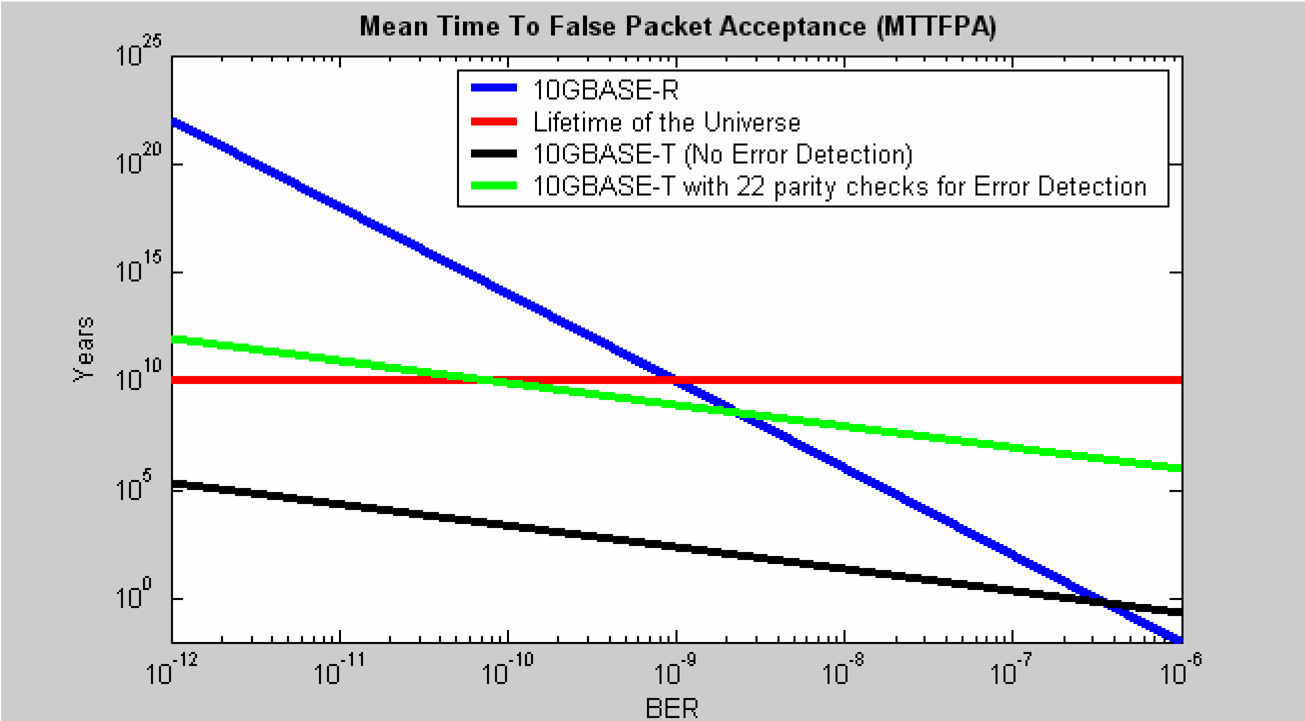
- **For LDPC coded bits, use some independent parity check equations from the layered Djurdjevic codes for Error Detection**
  - Assumes that the remaining parity check equations result in robust Error Correction in the LDPC decoder.

Column weight in Djurdjevic construction	#information bits in 1024 block length RS-LDPC code (additional parity checks)	#information bits in 2048 block length RS-LDPC code (additional parity checks)
5	**893**	**1765**
6	**877 (16)**	**1723 (42)**
7	**861 (16)**	**1681 (42)**
8	**845 (16)**	**1649 (32)**
9	**839 (6)**	**1627 (22)**
10	**833 (6)**	**1605 (22)**
11	**827 (6)**	**1583 (22)**
12	**821 (6)**	**1561 (22)**

2K codes provide a large number of independent parity checks for each additional column weight.

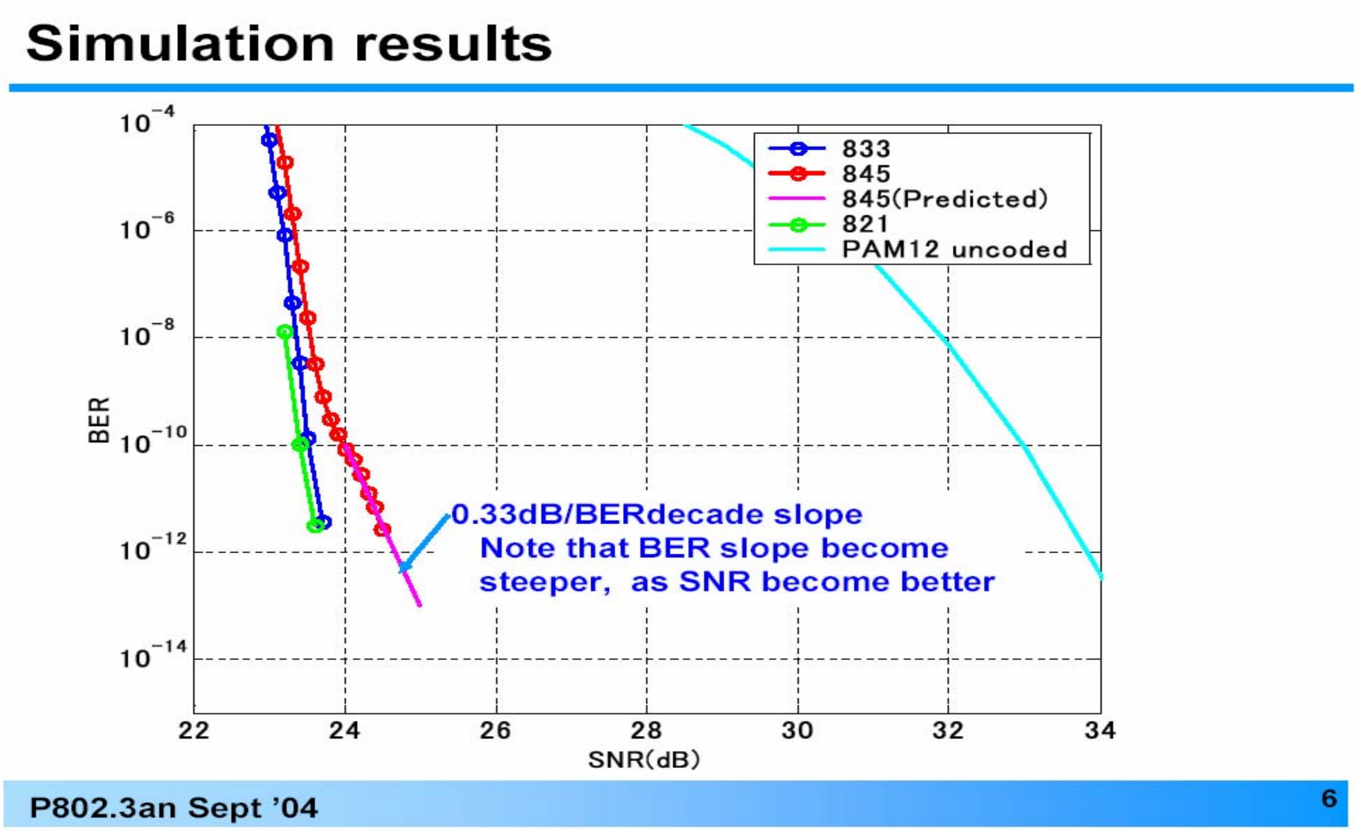
Increasing MTTFPA

- **Adding Error Detection capability with K Independent Parity check equations**
  - Assuming uniform distribution of valid codewords, increases MTTFPA by a factor of 2^K (for K=22 and 1E-12 BER, MTTFPA > **914** Billion Years)



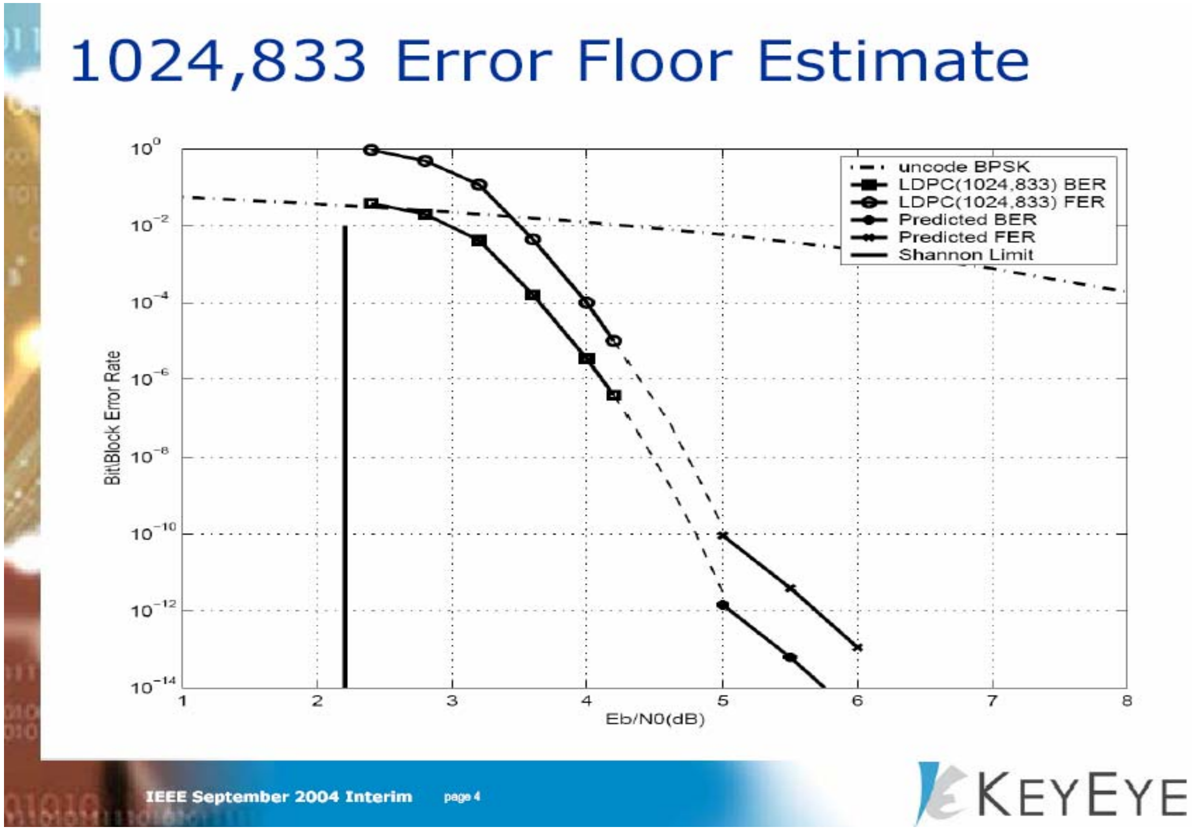
Increasing MTTFPA (1K codes)

(from seki_1_0904.pdf)



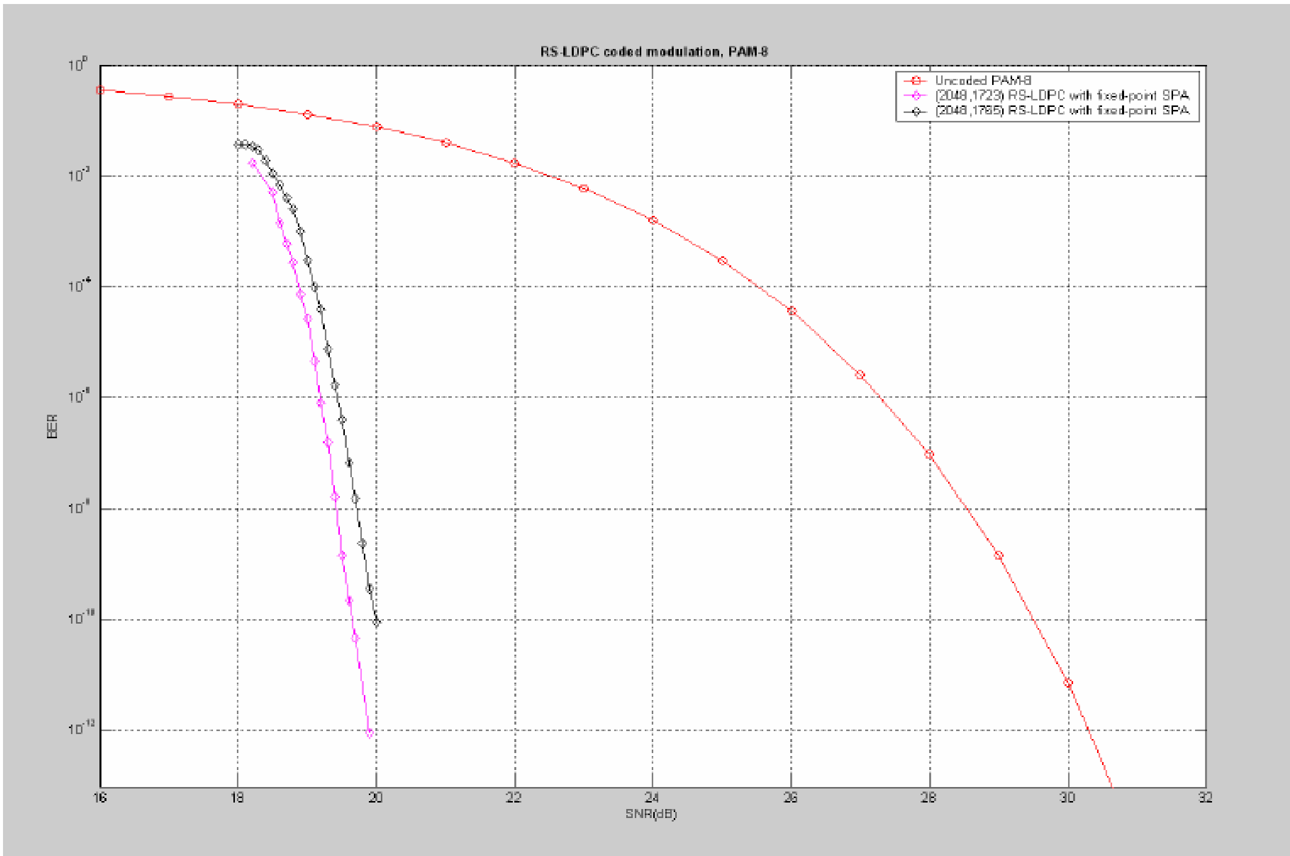
Increasing MTTFPA (1K codes)

(from lee_1_0904.pdf)



Increasing MTTFPA (2K codes)

(from rao_3_0904.pdf)

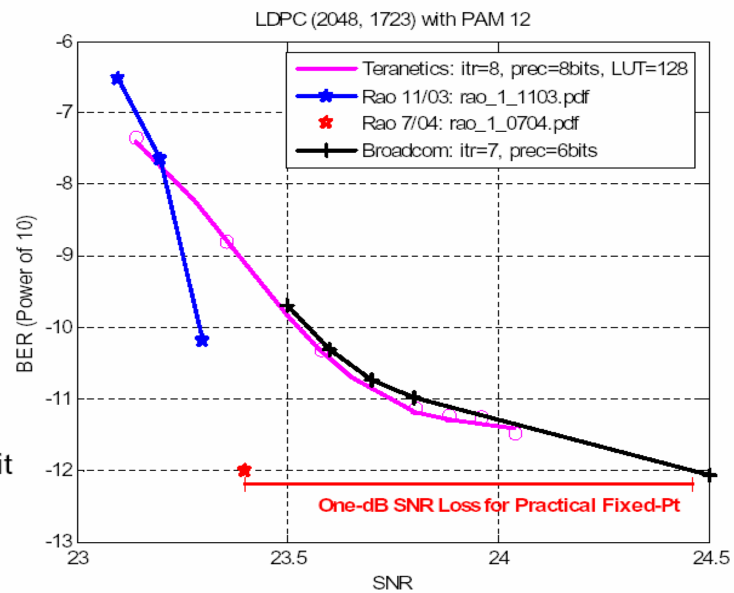


Increasing MTTFPA (2K codes)

(from tellado_1_0904.pdf)

LDPC(2048,1723) PAM12 Performance

- Significant BER slope degradation observed below 1E-11 for practical implementations of LDPC SPA decoder
  - Slope change occurs at theoretically predicted point
- Broadcom results use 7 iterations with 6 bit LUT (64 entries)
- Teranetics results use 8 iterations with 7 bit LUT (128 entries)
- Rao's results use 12 iterations with 12 bit LUT (4096 entries).
- A typical LDPC decoder will have 100s or 1000s of LUTs
  - Rao's LUTs are > 40x larger.
- Typical FEC decoders require 3-5 bit fixed point math



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Increasing MTTFPA (coded bits)

- **Difficult to provide required Error Correction AND Error Detection with reasonable column weight and complexity using 1K codes.**
  - Even if we use code with column weight of 14, i.e., (1024,809) code, the Error Correcting performance of the (1024,833) code is barely acceptable (lee_1_0904.pdf, slide 4).
- **With 2K codes, we need to use codes with column weight of 8 or better to achieve consensus on acceptable Error Correction and Error Detection performance**
  - (2048,1649) code or better as the base code with 22 or more parity check equations to be used for Error Detection.

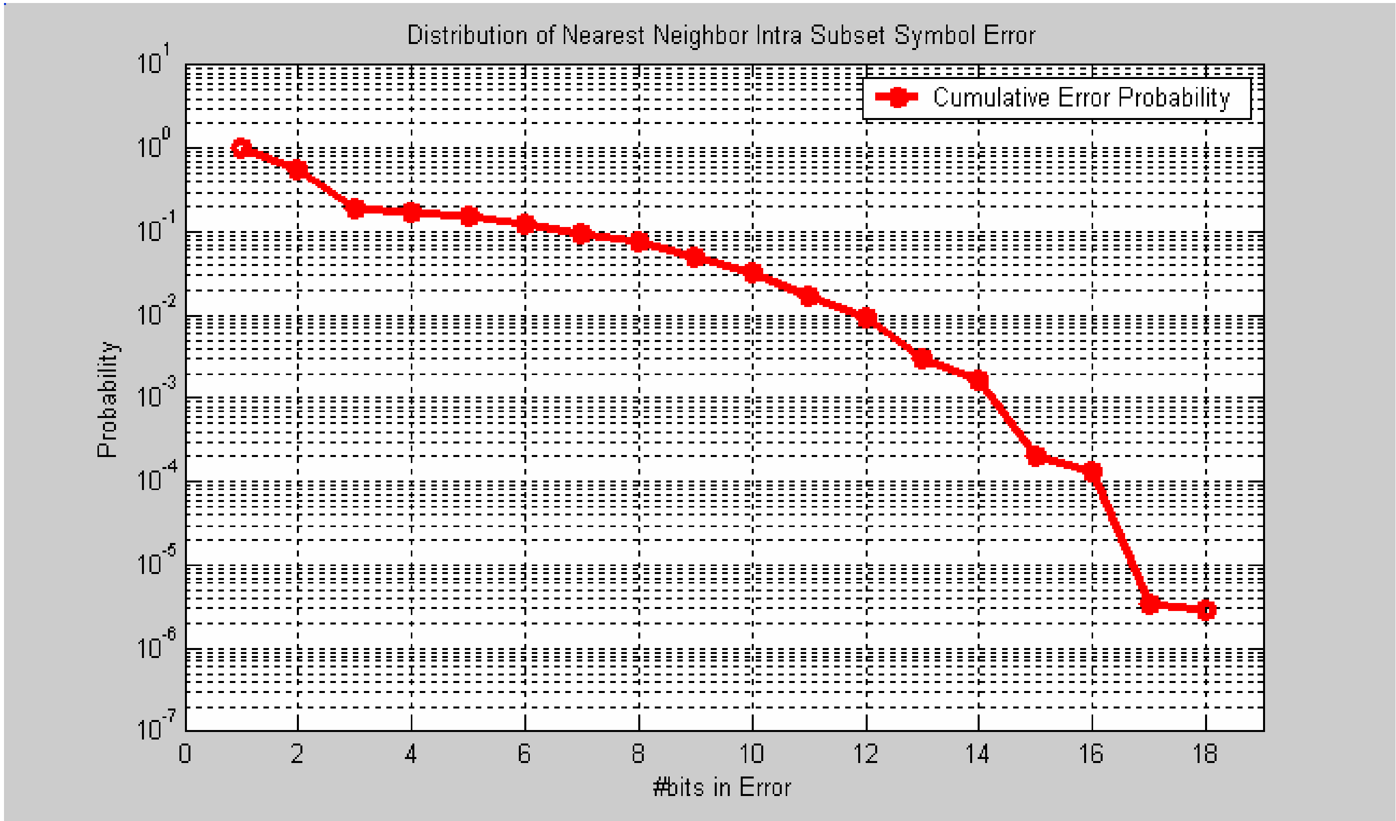
Increasing MTTFPA (un-coded bits)

- **For un-coded information bits, i.e., transmit bits that are NOT protected by the LDPC code, it is very desirable to ensure that the constellation is Gray mapped, even under THP expansion.**
  - Nearest neighbor co-set symbol error (Intra-Subset error) should result in at most 1 bit error.

- **If a non-Gray mapped constellation is used, then**
  - A detailed, enumerative analysis needs to be conducted on the types and positions of the burst errors that can occur and checked against the Ethernet CRC to assess the probability that the CRC will detect the burst errors, OR
  - A separate Error Detection code should be added to protect the un-coded information bits.
  - Burst errors from non-Gray mapped constellations are not randomly distributed – they occur in bunches and the CRC error detection assessment requires detailed enumerative analysis, as in walker_1_0100.pdf, slide 14.

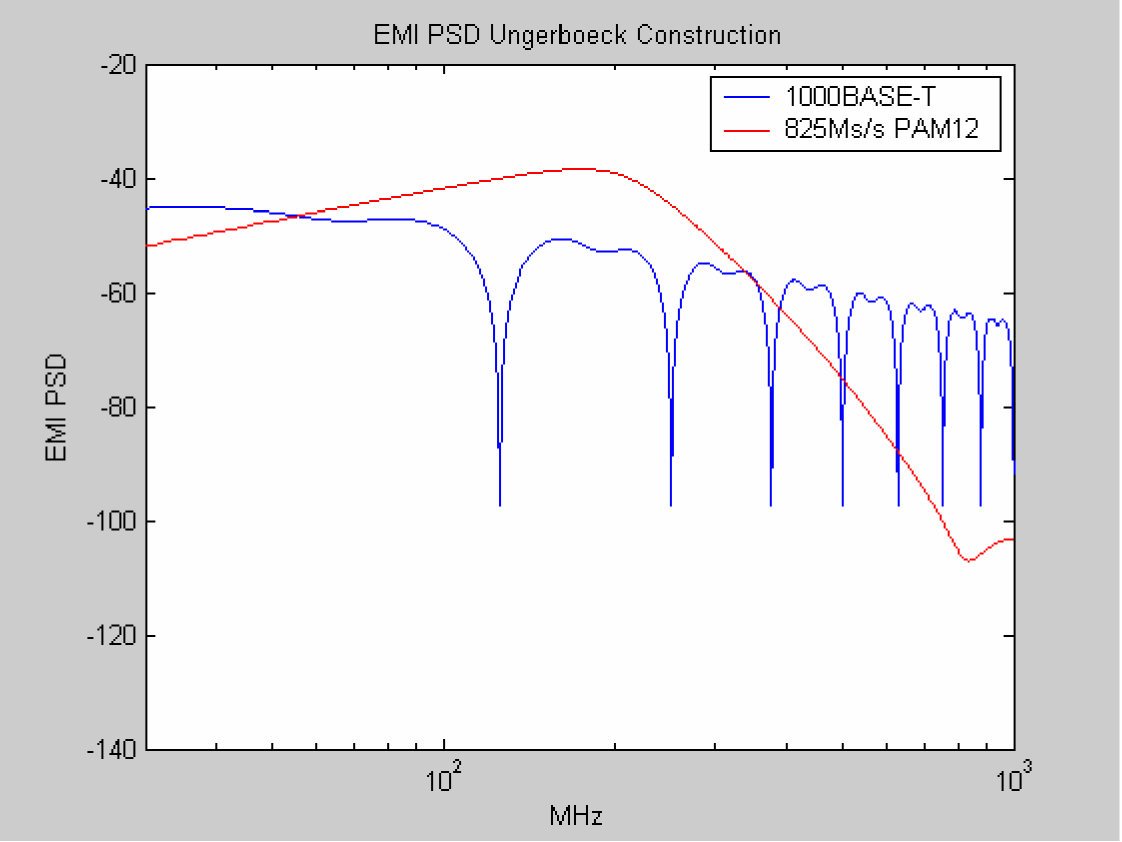
Non Gray Mapping among 12D-PAM12 uncoded bits

- **Nearest Neighbor symbol error in the 12D-PAM12 uncoded bits can result in up to 18 bit errors after Ternary-to-Binary de-mapping.**



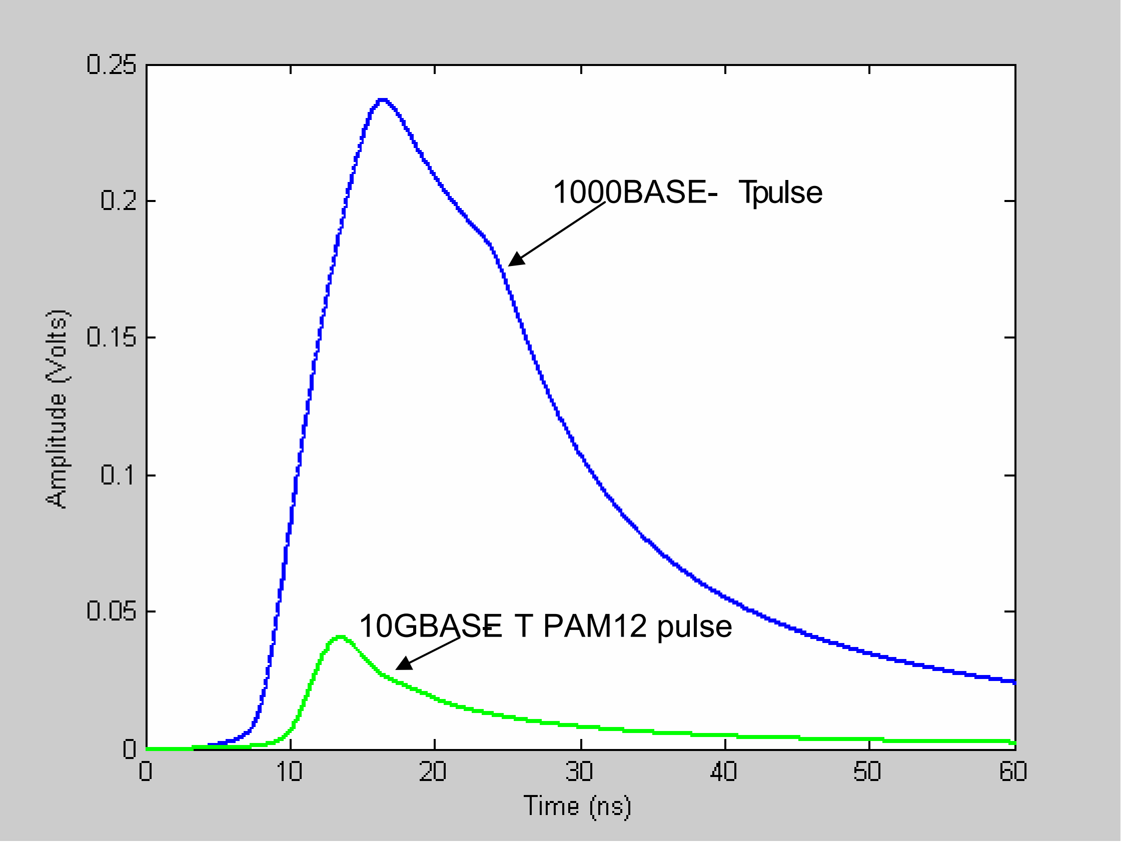
Emissions Penalty over 1G

EMI PSD peak is **6.6dB** higher than that of 1G



Susceptibility Penalty over 1G

Susceptibility and impulse noise tolerance penalty is at least **15.3dB** over 1G after 100m cabling

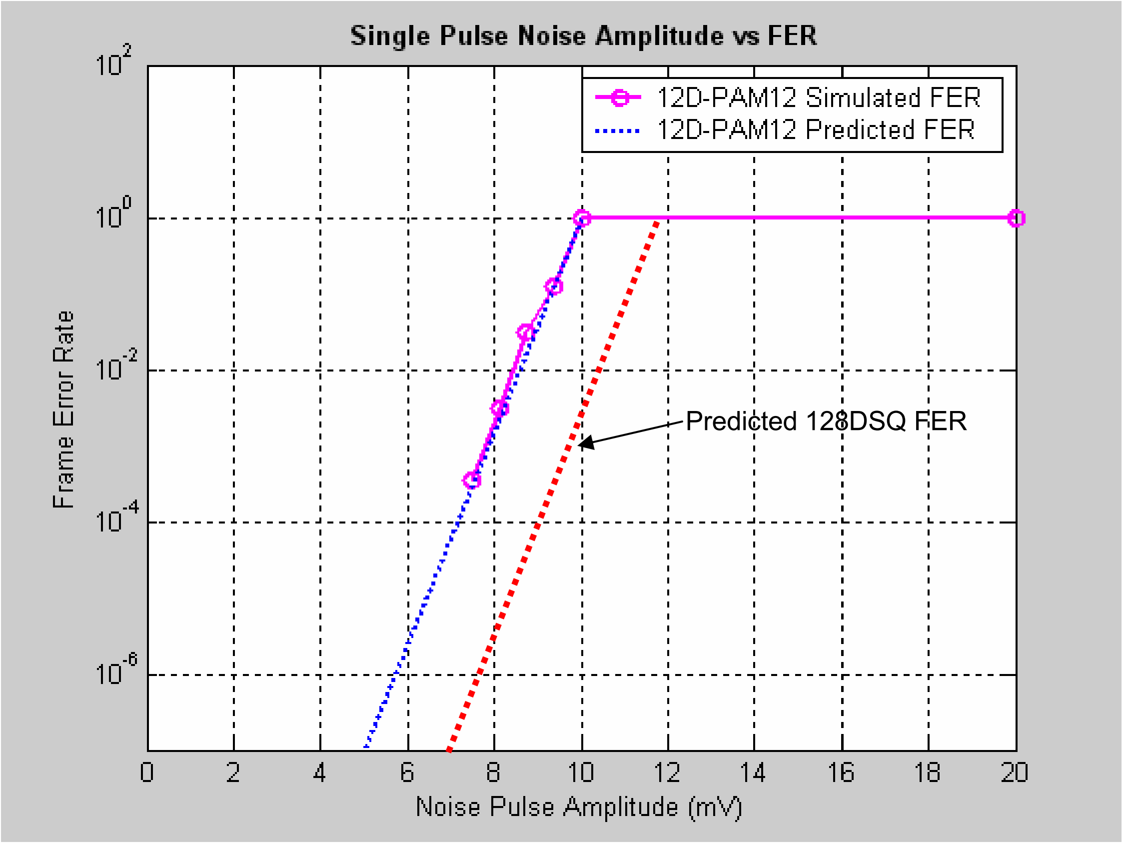


Can 100m objective of the 802.3an PAR be met with such susceptibility to EMI ingress and impulse noise?

First Robustness Test

- **Consider a 12D-PAM12 receiver operating at an SNR of 27.0dB (i.e. with 3dB margin over 1E-12 BER)**
  - Assume that the residual error at the input of the LDPC decoder is additive White Gaussian noise corresponding to an SNR of 27.0dB
- **In each LDPC block,**
  - Apply a "noise" pulse of amplitude X mV for exactly 1 symbol period, at a position chosen randomly.
  - X is referenced with respect to the input of the receiver after a 100m CAT-6 cable.
  - Assume that the main tap of the FFE has a gain of 2.0 (i.e., 6.0dB)
    - Note that this FFE gain is smaller than the value reported on the reflector.
- **Measure the Frame Error Rate of the LDPC decoder as a function of the amplitude of the noise pulse, X.**
- **Test emulates instantaneous clock jitter noise, Echo nonlinearity noise, etc.**

First Robustness Test Result

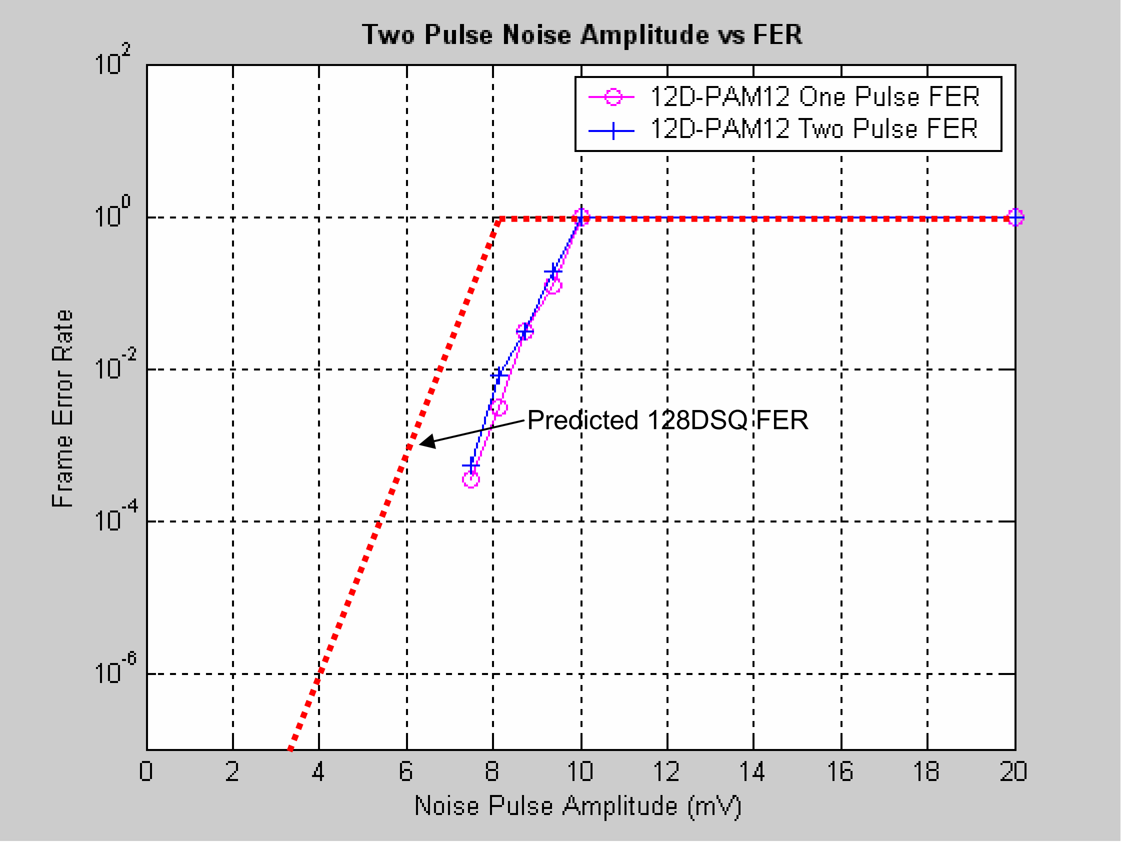


NOTE: All Frame errors were due to Intra-Subset Symbol errors, i.e. undetected by LDPC decoder

Second Robustness Test

- **Consider a 12D-PAM12 receiver operating at an SNR of 27.0dB (i.e. with 3dB margin over 1E-12 BER)**
  - Assume that the residual error at the input of the LDPC decoder is additive White Gaussian noise corresponding to an SNR of 27.0dB
- **In each LDPC block,**
  - Apply TWO “noise” pulses of amplitude X mV over 2 consecutive symbol periods, at a position chosen randomly.
  - X is referenced with respect to the input of the receiver after a 100m CAT-6 cable.
  - Assume that the main tap of the FFE has a gain of 2.0 (i.e., 6.0dB)
    - Note that this FFE gain is smaller than the value reported on the reflector.
- **Measure the Frame Error Rate of the LDPC decoder as a function of the amplitude of the noise pulse, X.**
- **Test emulates correlated instantaneous clock jitter noise over two pairs, etc.**

Second Robustness Test Result



NOTE: All Frame errors were due to Intra-Subset Symbol errors, i.e. undetected by LDPC decoder

Third Robustness Test (suggested by George Zimmerman)

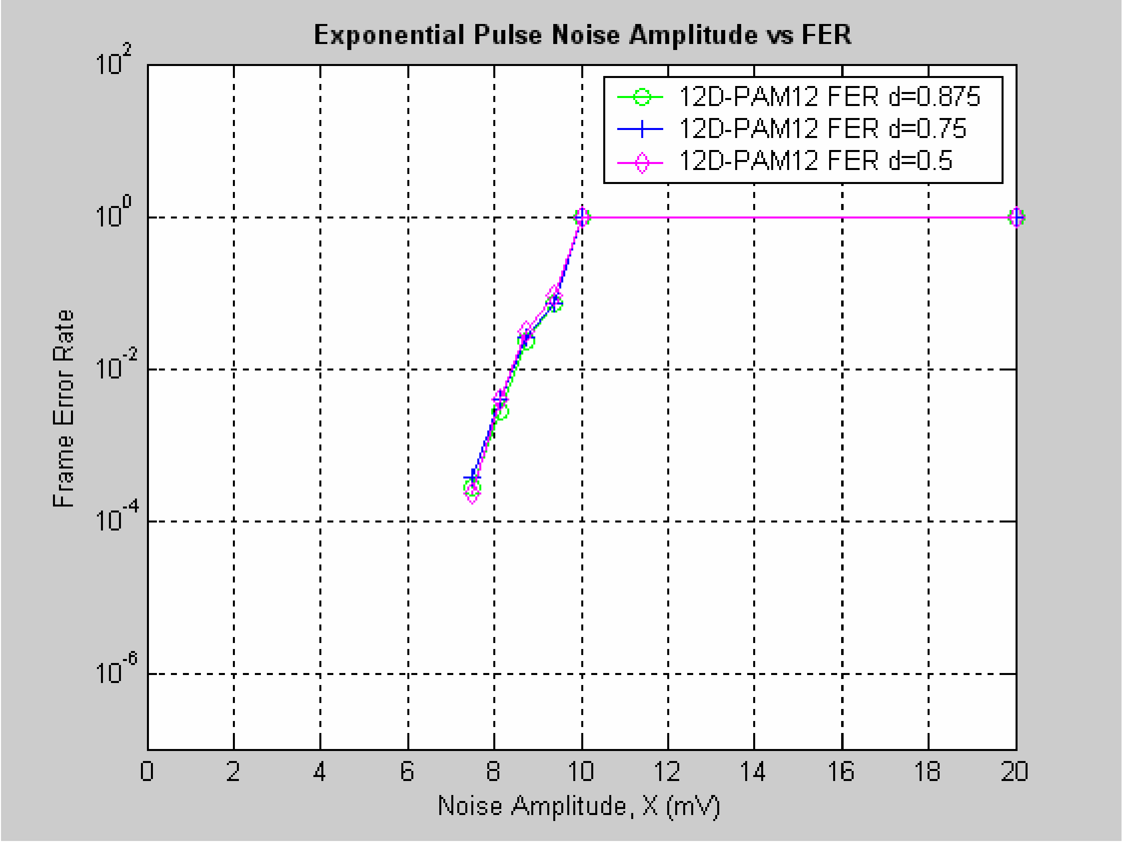
- **Consider a 12D-PAM12 receiver operating at an SNR of 27.0dB (i.e. with 3dB margin over 1E-12 BER)**
  - Assume that the residual error at the input of the LDPC decoder is additive White Gaussian noise corresponding to an SNR of 27.0dB

- **In each LDPC block,**
  - Apply a train of “noise” pulses of amplitudes, X mV, dX mV, d^2X mV, … over consecutive symbol periods, for some d<1.0.
  - X is referenced with respect to the input of the receiver after a 100m CAT-6 cable.
  - Assume that the main tap of the FFE has a gain of 2.0 (i.e., 6.0dB)
    - Note that this FFE gain is smaller than the value reported on the reflector.

- **Measure the Frame Error Rate of the LDPC decoder as a function of the amplitude of the noise pulse train, X, and the decay factor, d.**

- **Test emulates impulse noise coupling onto wire.**

Third Robustness Test Result



NOTE: All Frame errors were due to Intra-Subset Symbol errors, i.e. undetected by LDPC decoder

Proposed Comment Resolution

Outline

Coding, Framing and Mapping consistent with the sense of the Task Force

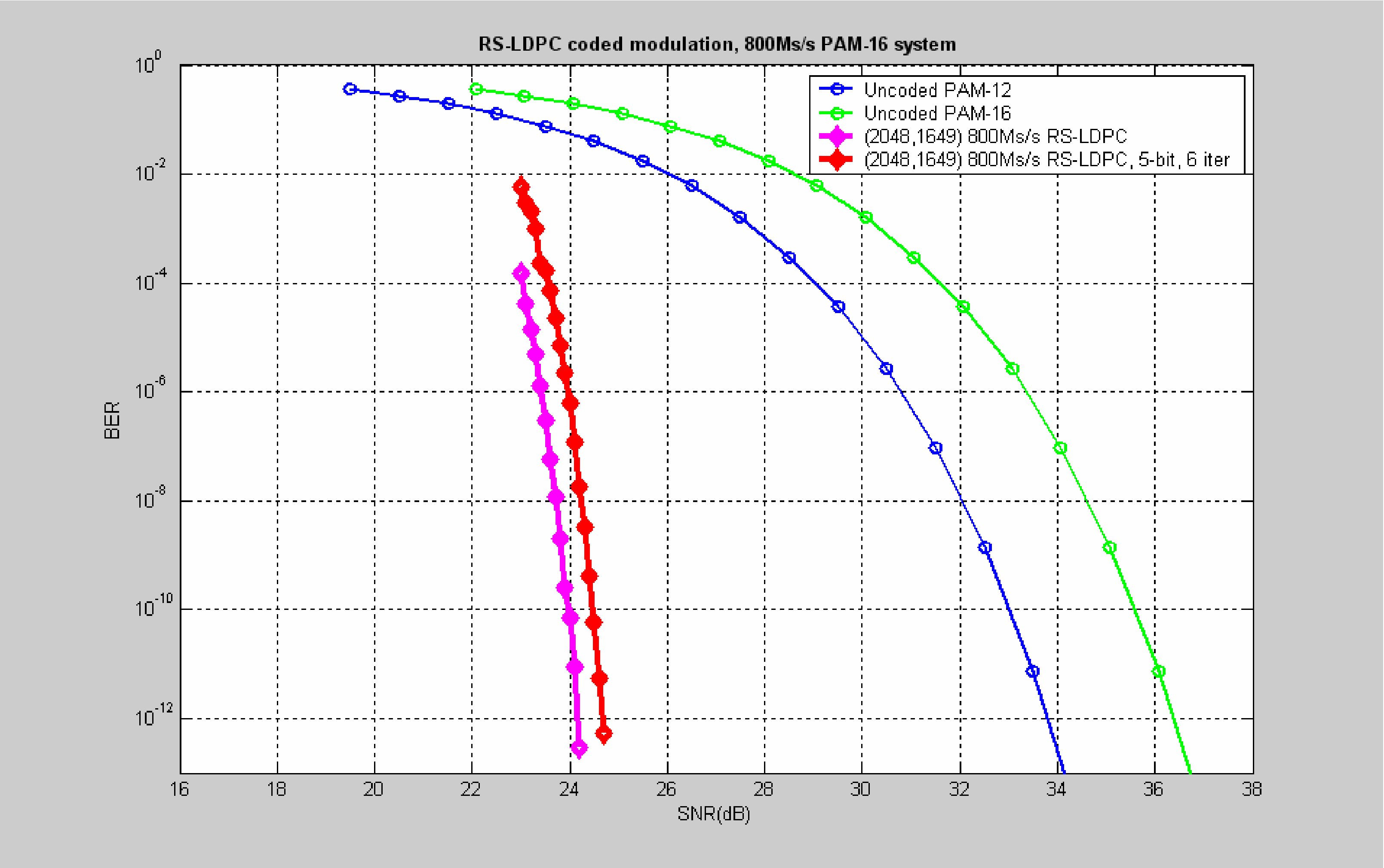
- **800Ms/s Pulse Amplitude Modulation**
- **(2048,1627) RS-LDPC code**
  - For example, (2048,1649) RS-LDPC sub-code can be used for Error Correction
  - 22 parity checks used for Error Detection to ensure acceptable MTTFPA
- **128 symbol framing using 25 64B/65B blocks (1625 bits)**
  - **Low intrinsic latency of 160ns**
- **2048 coded bits are Gray-mapped onto 512 PAM-16 symbols and transmitted over four twisted pairs in 128 symbol periods.**
  - All transmit bits are protected by LDPC decoder – eliminates co-set distance limitation with respect to EMI ingress tolerance.
  - One dimensional mapping
  - Modulo “power of 2” arithmetic throughout.

Bit-to-Symbol Mapping

- +15 = 0000
- +13 = 0001
- +11 = 0011
- +9 = 0010
- +7 = 0110
- +5 = 0111
- +3 = 0101
- +1 = 0100

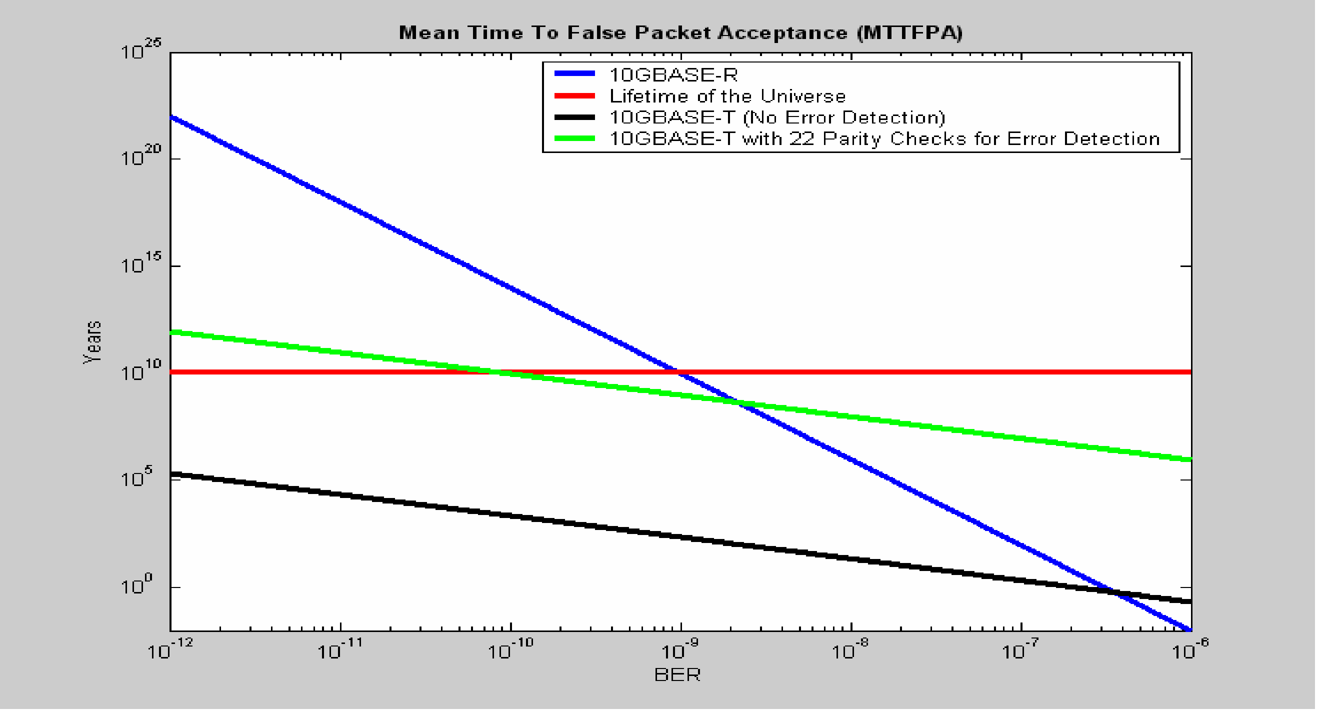
- -1 = 1100
- -3 = 1101
- -5 = 1111
- -7 = 1110
- -9 = 1010
- -11 = 1011
- -13 = 1001
- -15 = 1000

Simulation Results

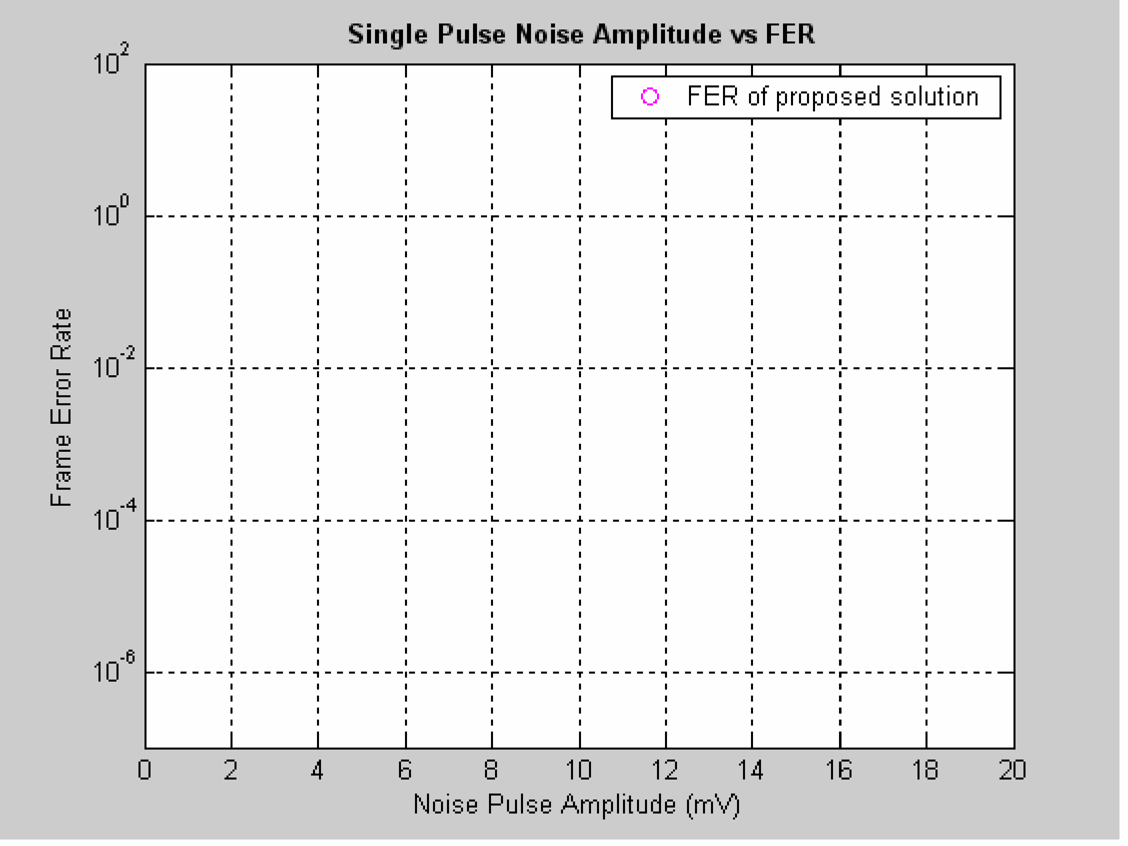


MTTFPA for Proposed Solution

- **Assume 22 parity check equations are used for Error Detection and (2048,1649) code is used for Error Correction**
  - Assuming uniform distribution of valid codewords, for 1E-12 BER, MTTFPA > **914** Billion Years

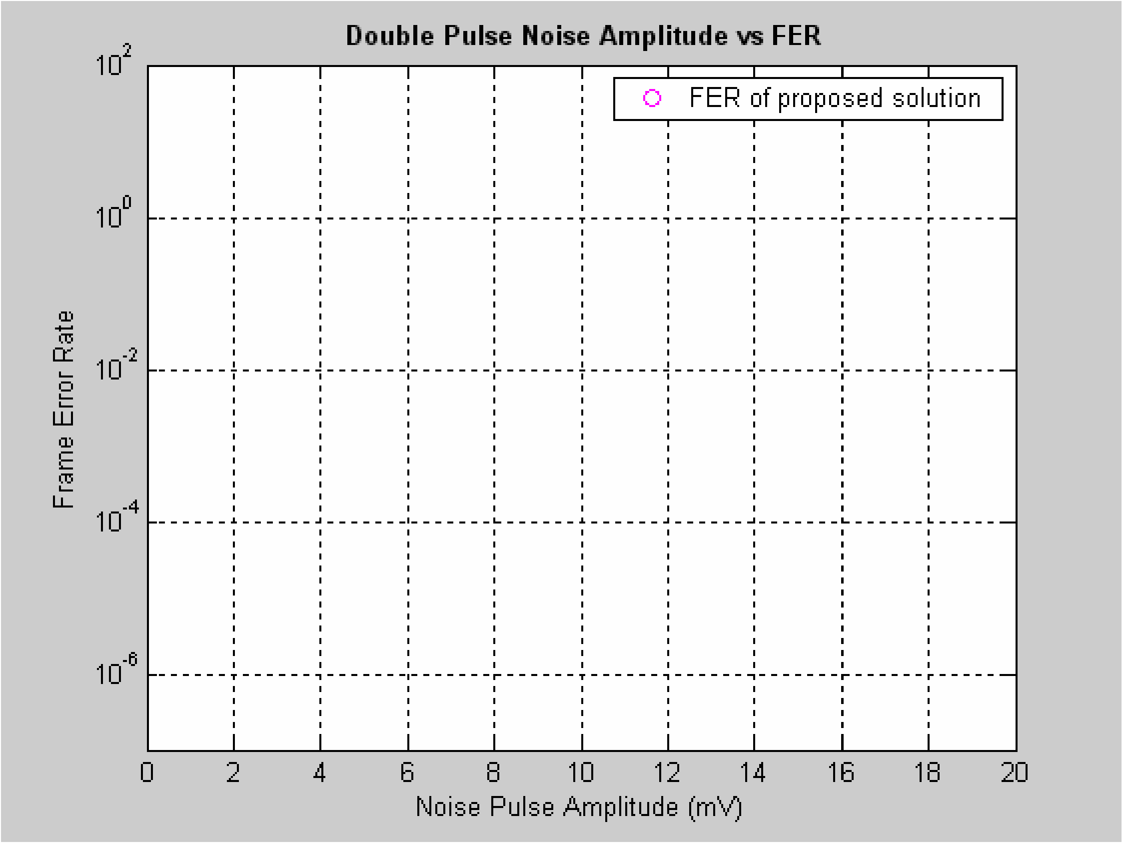


First Robustness Test Result



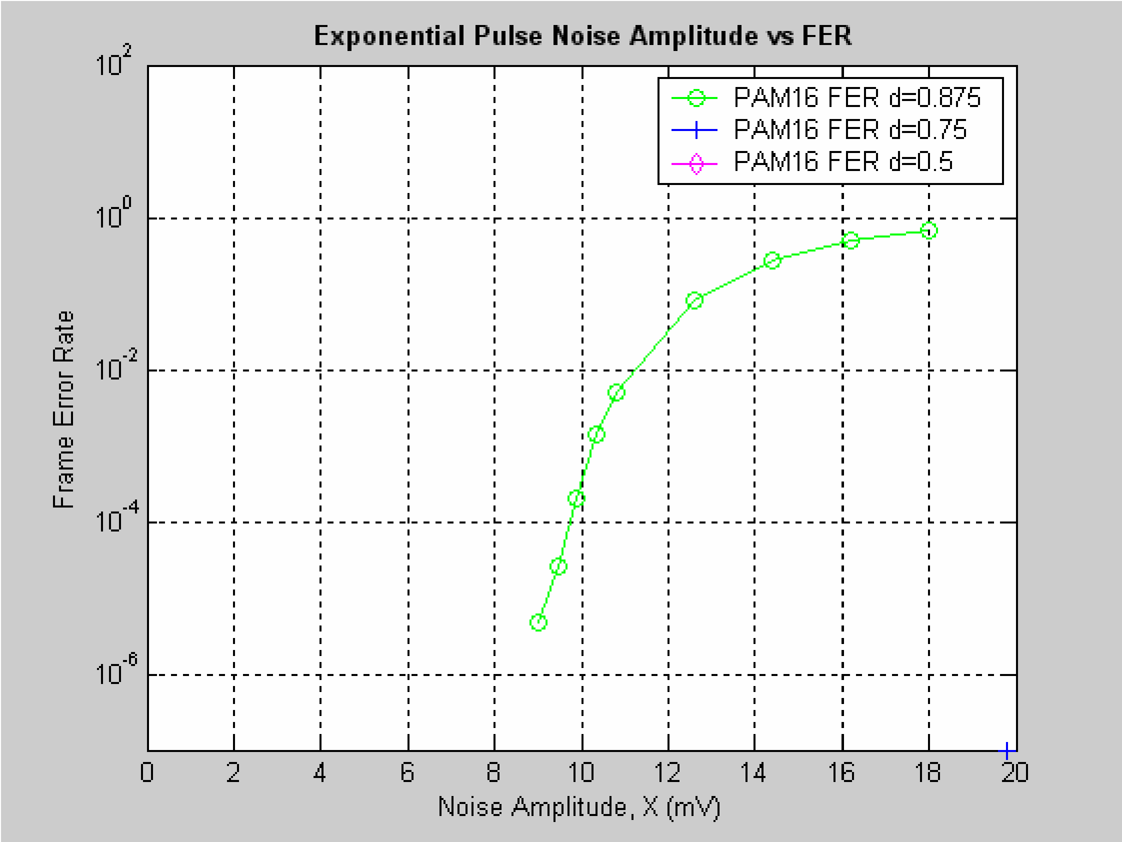
NOTE: No errors seen for 10mV peak and 20mV peak noise simulations for 5E7 blocks.

Second Robustness Test Result



NOTE: No errors seen for 10mV peak and 20mV peak noise simulations for 5E7 blocks.

Third Robustness Test Result



NOTE: Errors simulated at d=0.875 were all detected by the LDPC decoder.

Comparison of 800Ms/s Modulation Schemes

Bits per dimension	PAM8 (for reference only)	12D PAM12	PAM16 -128 DSQ	PAM16 (proposed comment resolution)	Remarks
#Data bits to be transmitted per symbol	2.5391	**3.1738**	**3.1738**	**3.1738**	After 64B//65B encoding, 1625bits/512sym = 3.1738
#bits transmitted after adding code redundancy. Computed as log2(#levels/symbol)	3.0	**3.5850**	**4.0**	**4.0**	For 128 DSQ, 16 levels (4bits) are used. For PAM12, log2(12)=3.5850.
#bits protected by the LDPC code and SPA decoder	2.0	**2.0**	**2.0**	**4.0**	#bits including LDPC parity check overhead.
#Information bits protected by the LDPC code	1.5391 (0.7695)	**1.5905 (0.7953)**	**1.6738 (0.8369)**	**3.1738 (0.7934)**	#information bits (Required rate of LDPC code)
#bits unprotected by the LDPC code	1.0	**1.5833**	**1.5**	**0.0**	For PAM12, 19 unprotected bits /12 symbols = 1.5833. **Unprotected bits are vulnerable to impulse noise and affect robustness of receiver.**
#bits unused in the modulation code space	0.0	**0.0017**	**0.5**	**0.0**	128DSQ uses 2bit repetition code over 2 dimensions.

Concluding Remarks

Proposed Coding, Framing and Mapping for an 800Ms/s 10GBASE-T PHY

- **Uses a robust (2048,1627) RS-LDPC code for guaranteed Error Correction/Detection performance**
  - For example, (2048,1649) RS-LDPC sub-code can be used for Error Correction
  - 22 parity checks used for Error Detection to ensure acceptable MTTFPA as in traditional Ethernet PHYs
- **Achieves low intrinsic latency of 160ns – same as 12D-PAM12 approach.**
- **Uses a simple 1D Gray coded mapping**
- **Eliminates co-set distance limitation with respect to EMI ingress and impulse noise tolerance.**
  - Better suited to meet 100m objectives of 802.3an PAR
  - Better suited for legacy copper installations
- **Uses transmit waveforms indistinguishable from 12D-PAM12 approach after THP.**