Options for Comment Resolution

Sailesh K. Rao
Phyten Technologies, Inc.
srao@phyten.com

Current Status

If we restrict ourselves to 800 Ms/s symbol rate and PAM12 modulation

- **12-level modulation makes it difficult to protect more than 2 bits per symbol with an LDPC code**
  - 12 is 2x2x3 which is a product of powers of different primes, which does not lead to a simple Galois field for coding purposes
  - We've considered an option to combine two separate (binary (GF4) and ternary (GF3)) codes in a symbol interleaved fashion. However,
  - Interleaved block decoders across dual Galois field domains didn't work well
    - **needed to "rob" from the current (1024,833) binary code to provide protection for the GF(3) ternary symbols**
    - **GF(3) ternary symbols fundamentally require high error-propagation mapping/demapping to achieve efficient code point usage (i.e., 12T->19B->12T)**
- **Required code rate to protect all the bits is at least 3.1738/3.5850 = 0.89, which is larger than the rate of all the 1K block codes that have been considered to date.**

Options for comment resolution with All Bits Protected (P)

Proposal	Symbol Rate	#Info Bits/ Symbol	#Protected Bits/ Symbol	#Unprotected Bits/ Symbol	Latency (T)	LDPC Code	Remarks
PAM8-P	1Gs/s (19.6dB)	2.5391	2.5391	0.0	192T	(2304,1979)	Most robust solution for 10GBASE-T
128DSQ-P	833Ms/s (approx. 23dB)	3.0469	3.0469	0.0	192T	(2688,2363)	Potential Compromise with 128 DSQ
PAM16-P	800Ms/s (24.2dB)	3.1738	3.1738	0.0	128T	(2048,1649)	rao_1_1104.pdf
128DSQ	800Ms/s (23.0dB)	3.1738	1.6738	1.5	256T	(2048,1723)	ungerboeck_1_1104.pdf
12D PAM12-T	800Ms/s (23.8dB)	3.1738	1.5905	1.5833	128T	(1024,833)	dabiri_1_1104.pdf

Compromise solutions

The most robust solution is PAM8-P.

If the Task Force is concerned about the 1Gs/s symbol rate, we can compromise with PAM16-P at 800Ms/s.

We can also compromise with the following 128DSQ-P at 833Ms/s:

- **833.33Ms/s Pulse Amplitude Modulation**
- **192 symbol framing using 36 64B/65B blocks (2340 bits)**
  - **2340** bits are protected by LDPC code
  - **Intrinsic Latency less than 128-DSQ proposal**
- **(2688,2363) RS-LDPC code, for e.g.,**
  - **23** bits used for Error Detection to ensure acceptable MTTFPA
- **2688 protected bits are mapped onto 384 128-DSQ symbols.**
  - **All transmit bits are protected by LDPC decoder – eliminates co-set distance limitation with respect to EMI ingress tolerance.**
  - Simple 2-D mapping
  - Modulo “power of 2” arithmetic throughout.