10GBASE-T

Modulation & Coding, Set of Fixed Precoders, and Start-up

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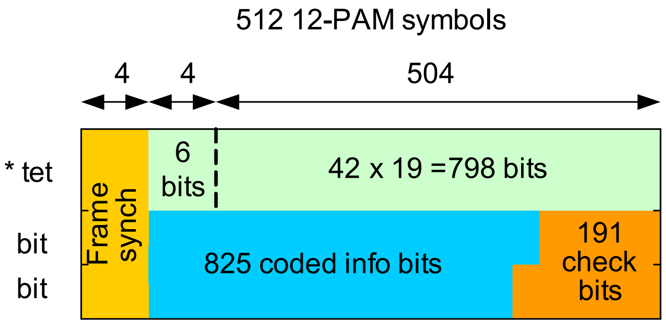
- Modulation, coding, and framing
- Framing details, synch & aux channel bits, and scrambling, etc.
- Set of fixed precoders and power back-off
- Start-up procedure
- Concluding remarks

Modulation, Coding, and Framing

Coding and framing for 12-PAMT (Ottawa, multi-vendor proposal)

12-PAM modulation with LDPC (1016,825) code = shortened LDPC(1024,833)


512 12-PAM symbols

4 4 504

* tet

bit

bit

Frame synch

6 bits

42 x 19 =798 bits

825 coded info bits

191 check bits

* tet = ternary digit

1 x mapping of 6 bits to 4 tets (2^6= 64 out of 3^4=81)

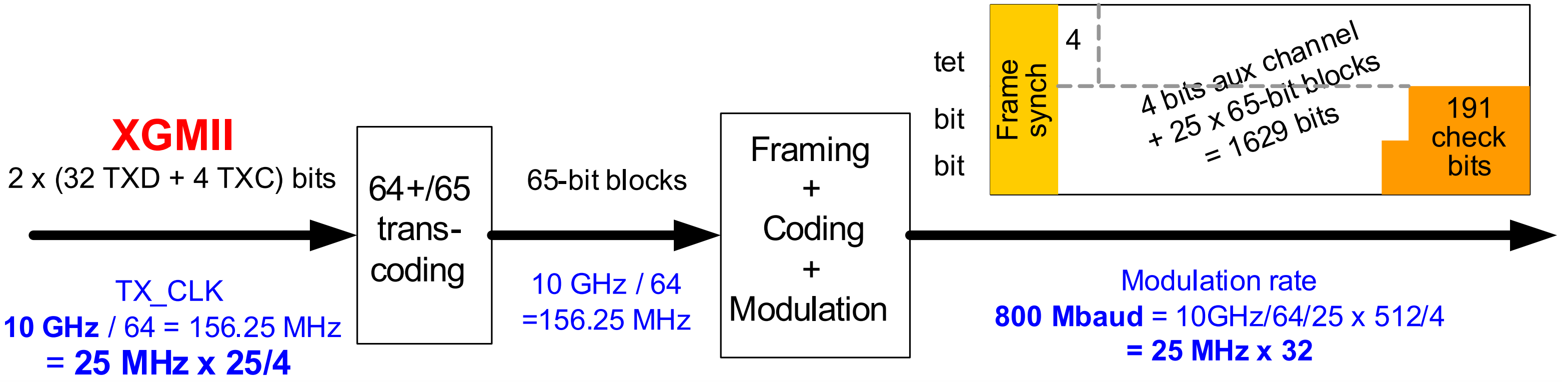
42 x mapping of 19 bits to 12 tets (2^{19}= 524288 out of 3^{12}=531441)

Code Block: 6 + 798 + 825 = 1629 info bits

(3.2321 bit/dim)

Framing and Clocks

PCS Frame = one code block


tet

bit

bit

Frame synch

4

4 bits aux channel + 25 x 65-bit blocks = 1629 bits

191 check bits

XGMII

2 x (32 TXD + 4 TXC) bits

TX_CLK

10 GHz / 64 = 156.25 MHz

= **25 MHz x 25/4**

64+/65 trans-coding

65-bit blocks

10 GHz / 64

=156.25 MHz

Framing + Coding + Modulation

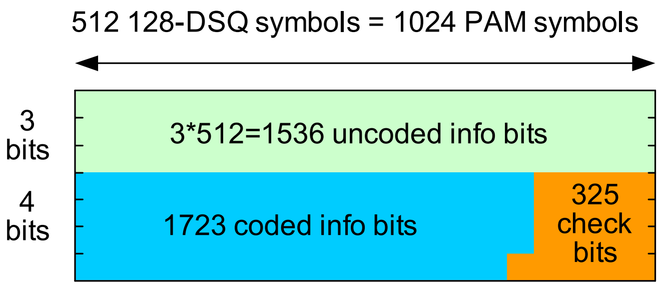
Modulation rate

800 Mbaud = 10GHz/64/25 x 512/4

= 25 MHz x 32

Proposed new coding and framing for 128-DSQ

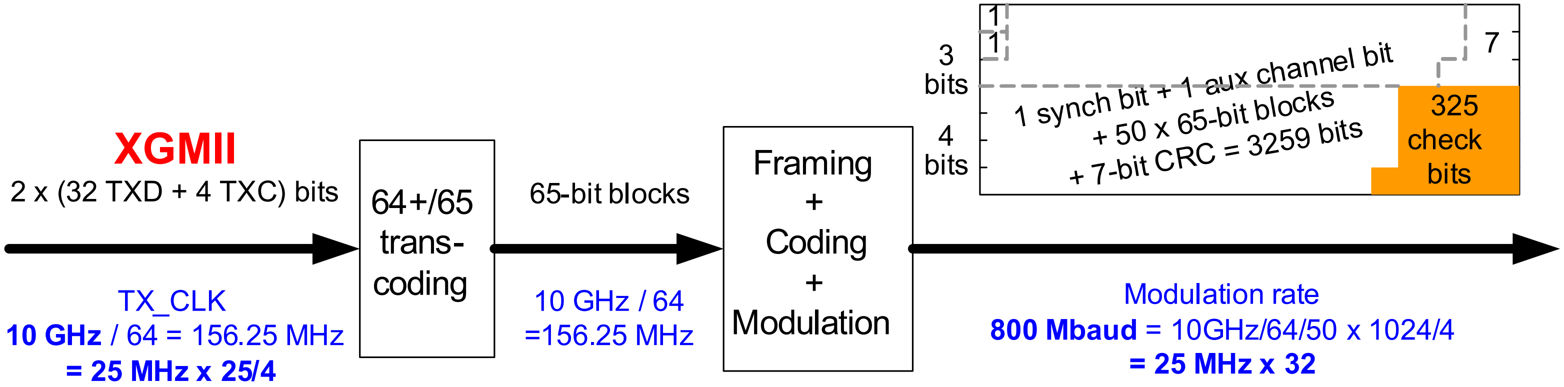
128-DSQ modulation with LDPC (2048,1723) code



Code Block: 1723 + 1536 = 3259 info bits
(3.1826 bit/dim)

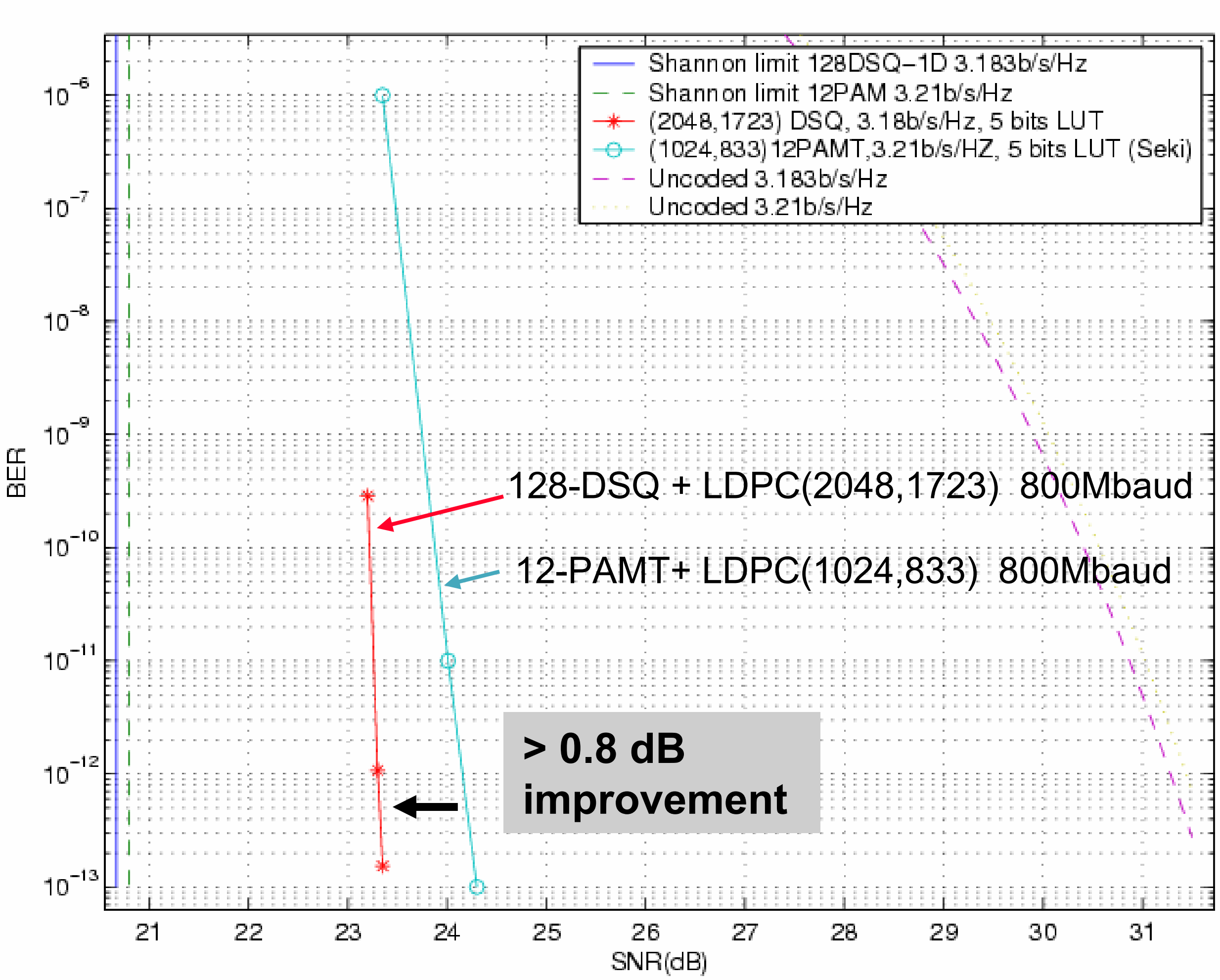
Framing and Clocks

PCS Frame = one code block



Error performance

Simulation results



128-DSQ + LDPC(2048,1723) 800Mbaud

12-PAMT+ LDPC(1024,833) 800Mbaud

> 0.8 dB improvement

128-DSQ + LDPC(2048,1723) advantages

Advantages over 12-PAMT + LDPC(1024,833)

- **> 0.8 dB performance improvement**
- **LDPC(2048,1723) decoding requires fewer operations per time unit than LDPC(1024,833) decoding***
- **Simple mapping and precoding based on power-of-two arithmetic**
- **Avoidance of binary ↔ ternary conversions, hence no multiplication of uncoded-only errors.**

* LDPC(2048,833): 140 messages / PAM symbol (10240 edges x 7 iter / 512 PAM symbols)

LDPC(2048,1723): 84 messages / PAM symbol (12288 edges x 7 iter / 1024 PAM symbols)

False packet acceptance with 128-DSQ+LDPC(2048,1723)

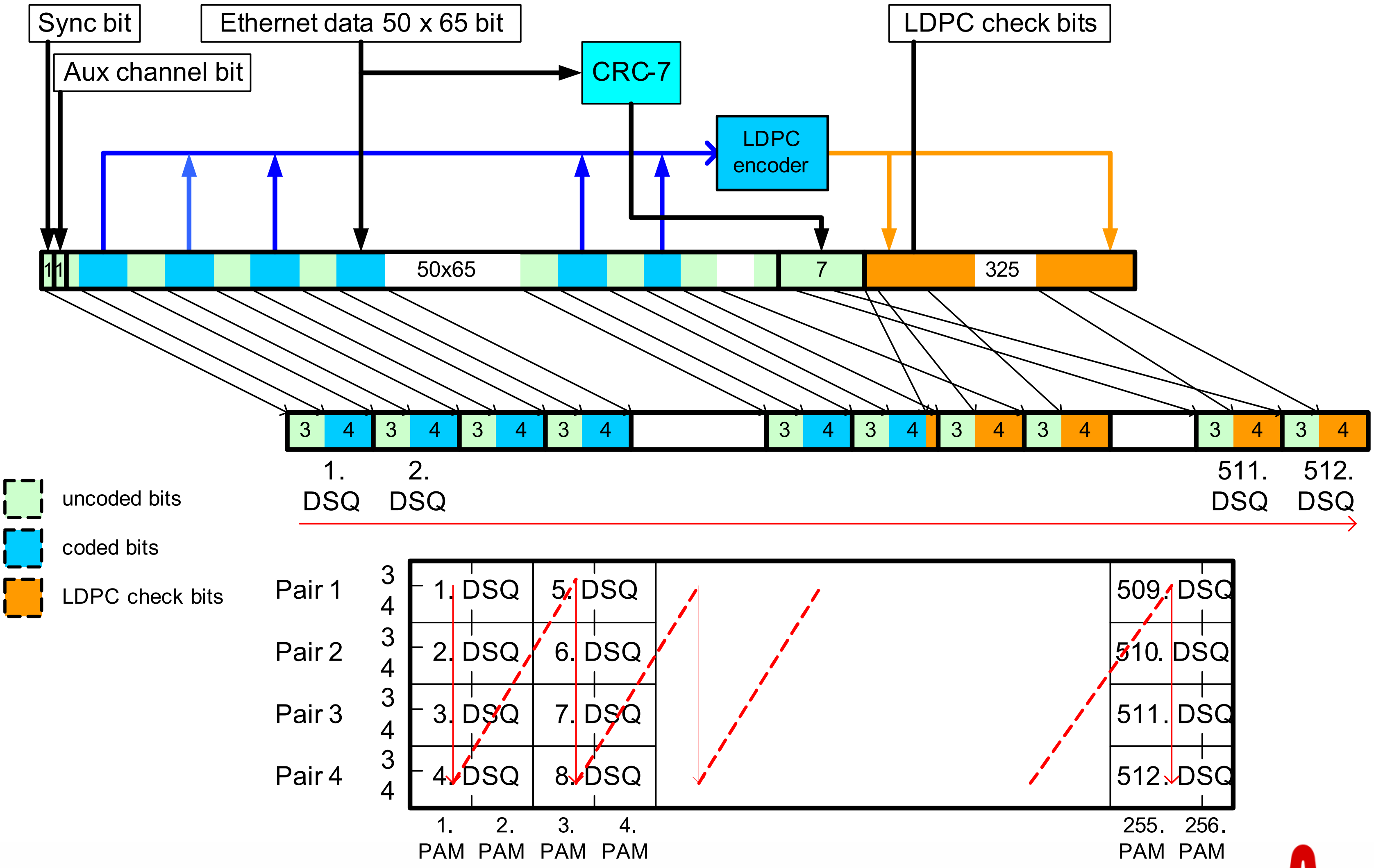
Conjecture: mean time to false packet acceptance (MTTFPA) > 10^4 years

- **Miss-correction to a false valid codeword (FVCW) has never been observed in simulation, neither in low-SNR (<20 dB) nor higher-SNR (>20 dB) region. Assume Prob(FVCW) < 10^{-7}*. Then: MTTFPA(FVCW) > 10^7 PCS frames x 320 ns (PCS frame duration) x 2^7 (CRC-7) x 2^{32} (CRC-32) = 4.4 10^{11} sec = 14’000 years.**
- **LDPC decoding to invalid codewords is easily detected.**
- **Uncoded-bit-errors-only (UBEO) events may occur in higher-SNR region, especially in the presence of AWGN + short impulsive noise events. No error multiplication effect, as with ternary/binary conversions.**
- **The CRC-7 provided in the 128-DSQ+LDPC(2048,1723) PCS frames in conjunction with the Ethernet frame check CRC-32 should provide sufficient detection capability for UBEO events. Assume Prob(UBEO) < 10^{-8}. Then MTTFPA(UBEO) > 140’000 years.**

***Simulation of 10^7 blocks, SNR=20dB with no undetected errors**

Framing Details, Synch & Auxiliary Channel Bits, and Scrambling

128 DSQ + LDPC(2048,1723): framing details



🟩 uncoded bits

🟦 coded bits

🟧 LDPC check bits

(Alternatively, use symbol interleavings of various kinds)

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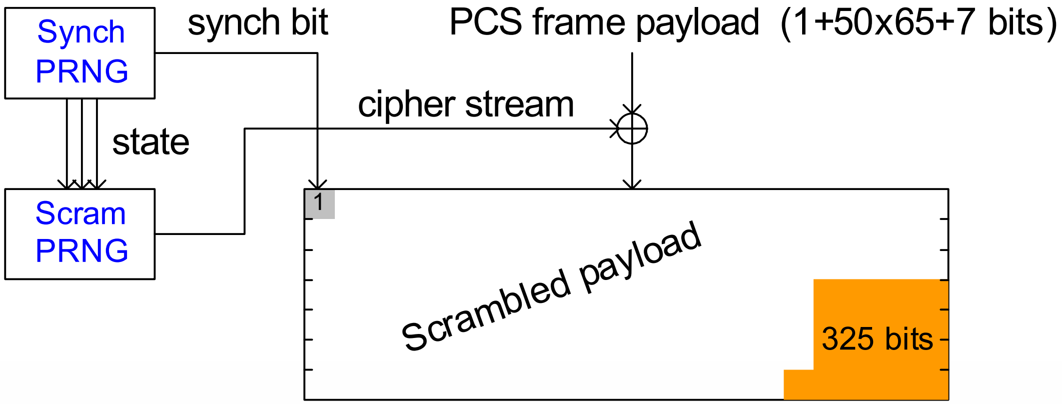
128 DSQ + LDPC(2048,1723): synch and scrambling

- **Synch PRNG generates and inserts one Synch Bit per PCS frame:** permits in receiver verification of PCS frame synchronization and fly-wheel (re-)synchronization
- **At beginning of each PCS frame Scram PRNG is initialized with state of Synch PRNG**
- **Scram PRNG generates cipher-scrambling sequence for use within PCS frame:** cipher-scrambling sequence is mod-2 added to PCS payload.

Generic: could be applied to other framing schemes

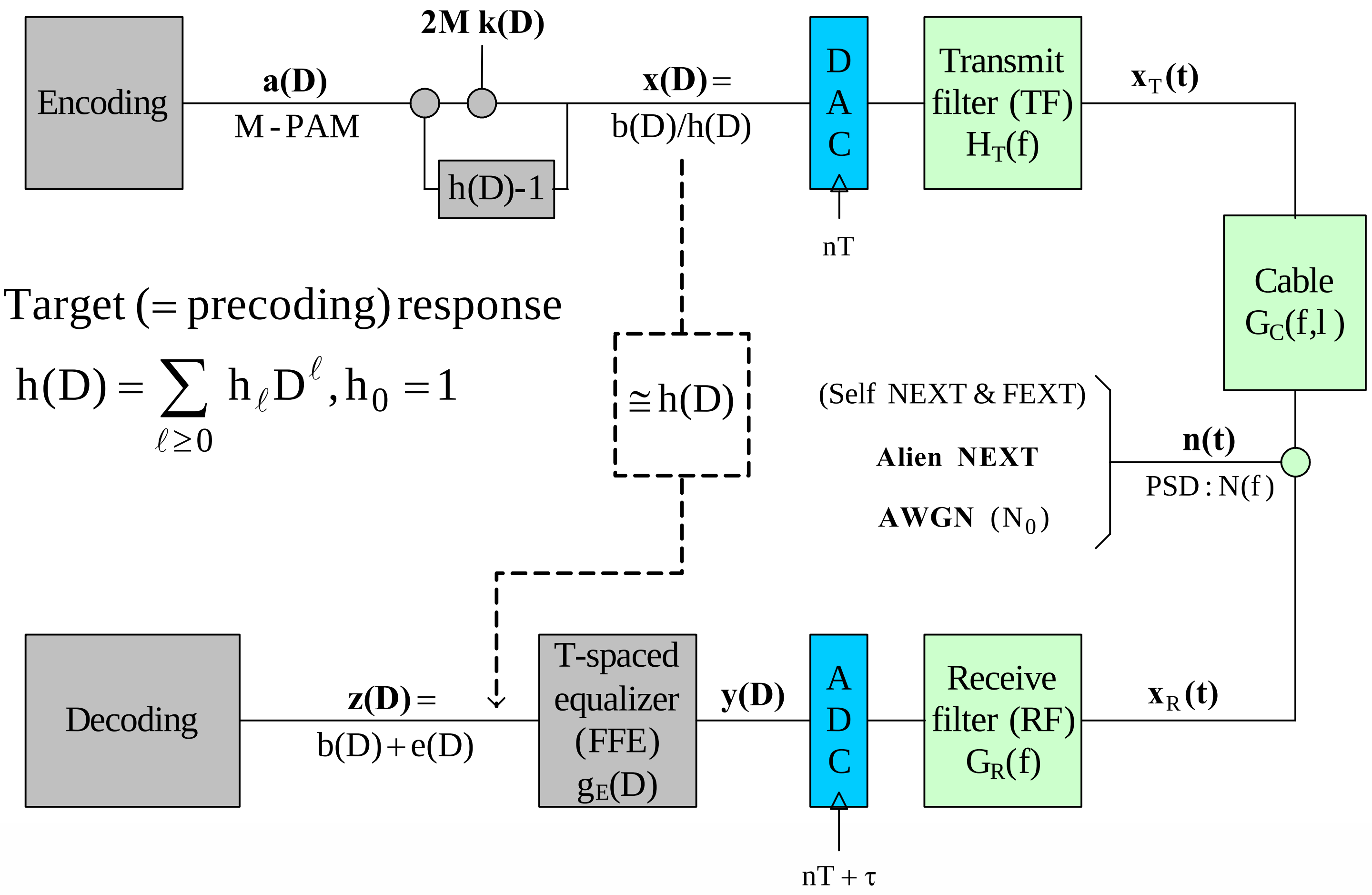


Set of Fixed Precoders and Power Back-off

10GBASE-T PAM transmission model (one pair)

$a(D) + 2M\,k(D) = b(D)$ ... modulation symbols in expanded constellation

$k_n \in Z$ s.t. $-M \le x_n < M$



Target (= precoding) response

$$h(D) = \sum_{\ell \ge 0} h_\ell D^\ell, \; h_0 = 1$$

Variable-length 10GBASE-T cable models (ungerboeck_1_0704.pdf)

Complex-valued cable-transfer function

skin effect

$$G_C(f_{[Hz]},\ell_{[m]}) = e^{-\underset{\uparrow}{\ell\gamma(f)}} \times 10^{-4\times 0.02\times\sqrt{f/10^6}/20}\ ; \quad \gamma(f)=\sqrt{\frac{R_s\sqrt{jf/f_s}+j2\pi fL}{R_d+1/j2\pi fC}}$$

4 connectors

propagation constant

dielectric loss

$$f_s = 200\mathrm{MHz};\ L=0.5\mathrm{mH/m}, C=50\mathrm{pF/m}:\ Z_0 \cong \sqrt{L/C}=100\Omega,\ v=1/\sqrt{LC}=200\times 10^6\,\mathrm{m/s}$$

Expected alien-NEXT squared magnitude function

$$\left|G_A(f_{[Hz]},\ell_{[m]})\right|^2 = 10^{-\left(X1+2.5-S\times\log_{10}\sqrt{f/10^8}\right)/10} \times \left(1-\left|G_C(f,\ell)\right|^4\right);\ S=\begin{cases}10\,, & f\le 10^8\\ 15\,, & f\ge 10^8\end{cases}$$

NEXT attenuation [dB]

dependence on length

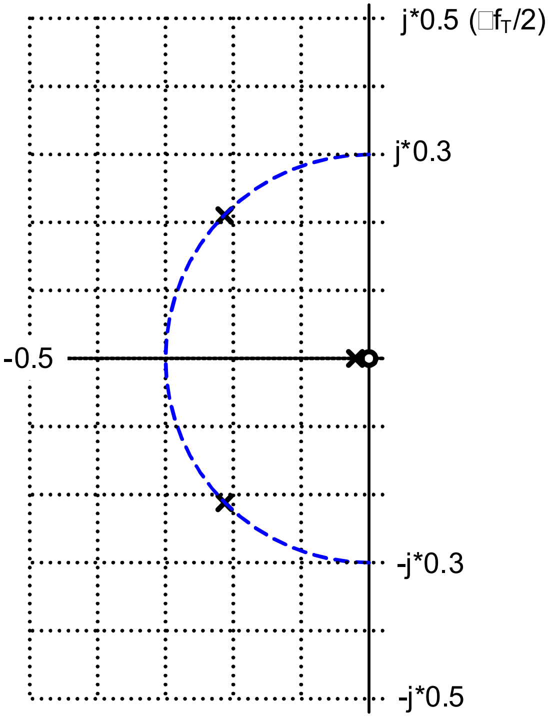
Model #1 (Cat 7, shielded) , 100 m → cabtyp **“ClassF”** : R_s=9.48 Ω/m, R_d=1.7 mΩ/m, X1=60 dB

Model #2 (Cat 6, unshielded) , 55 m → cabtyp **“ClassEu”** : R_s=9.85 Ω/m, R_d=3.5 mΩ/m, X1=47 dB

Model #3 (Cat 6, shielded) , 100 m → cabtyp **“ClassEs”** : R_s=9.85 Ω/m, R_d=3.5 mΩ/m, X1=62 dB

Transmit filter (TF) and TX PSD $S_T(f)$

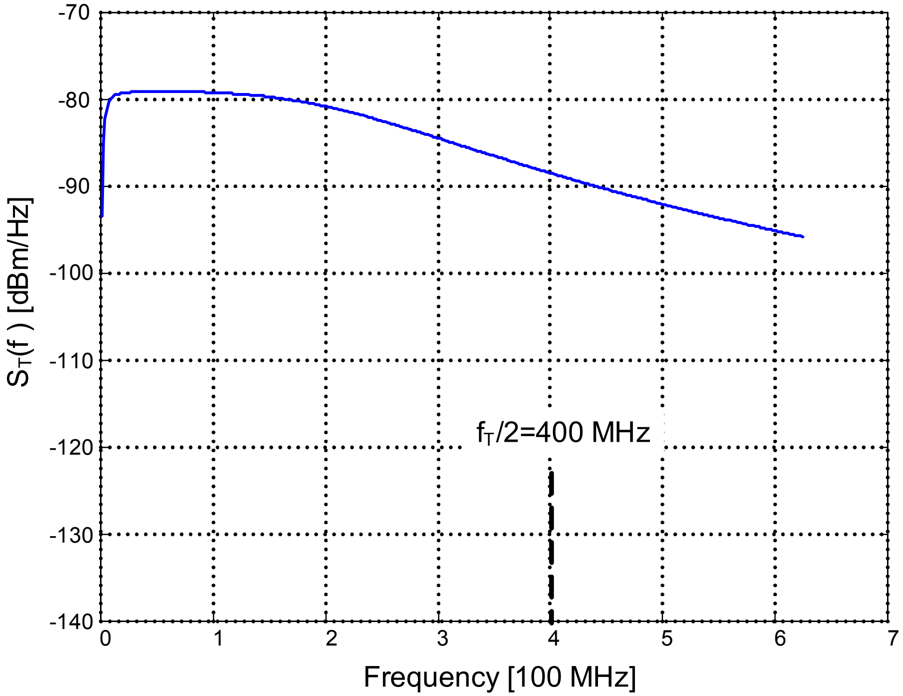
Modulation rate f_T = 800 Mbaud, P_T = 5 dBm,
TF = 2nd-order Butterworth filter with spectral null at dc (“BWF2dcn”)



f_N-plane

Zeroes in f_N-plane:
b1= 0.00000+j 0.00000

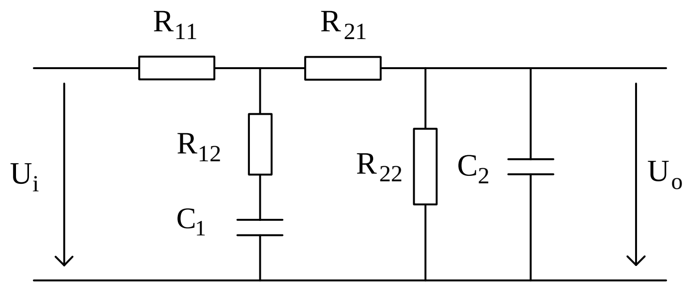
Poles in f_N-plane:
a1=-0.00500+j*0.00000
a2=-0.21213+j*0.21213
a3=-0.21213-j*0.21213



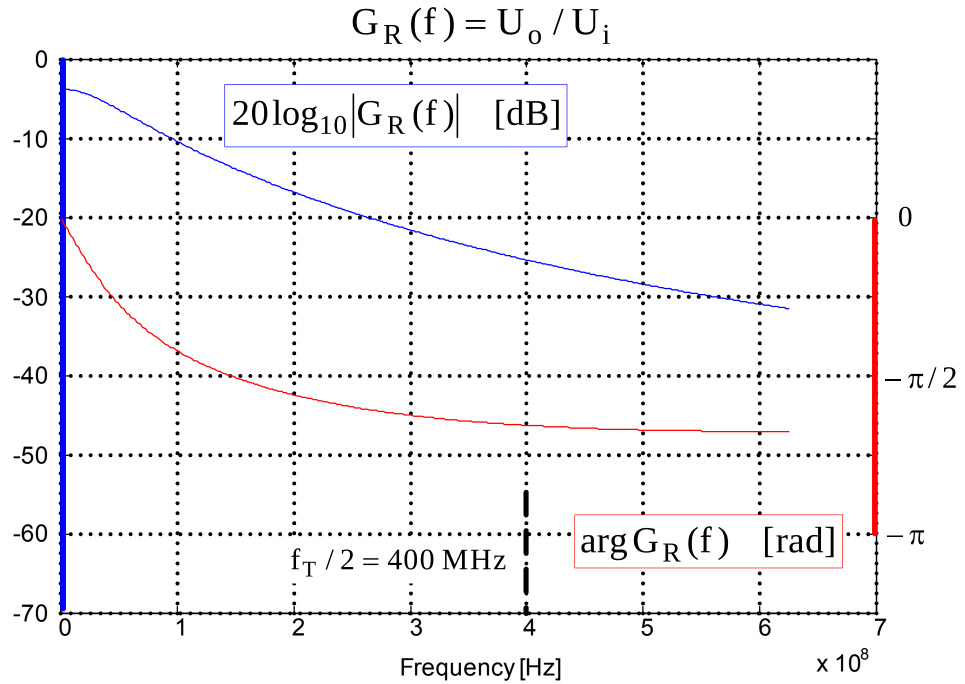
Achievable SNR vs. cable length does not critically depend on exact shape of S_T(f)

Receive filter (RF)

RF = “4R2C”: $G_R(f) \approx G_C(f, \ell = 50\text{m})$ of “ClassEs” cable

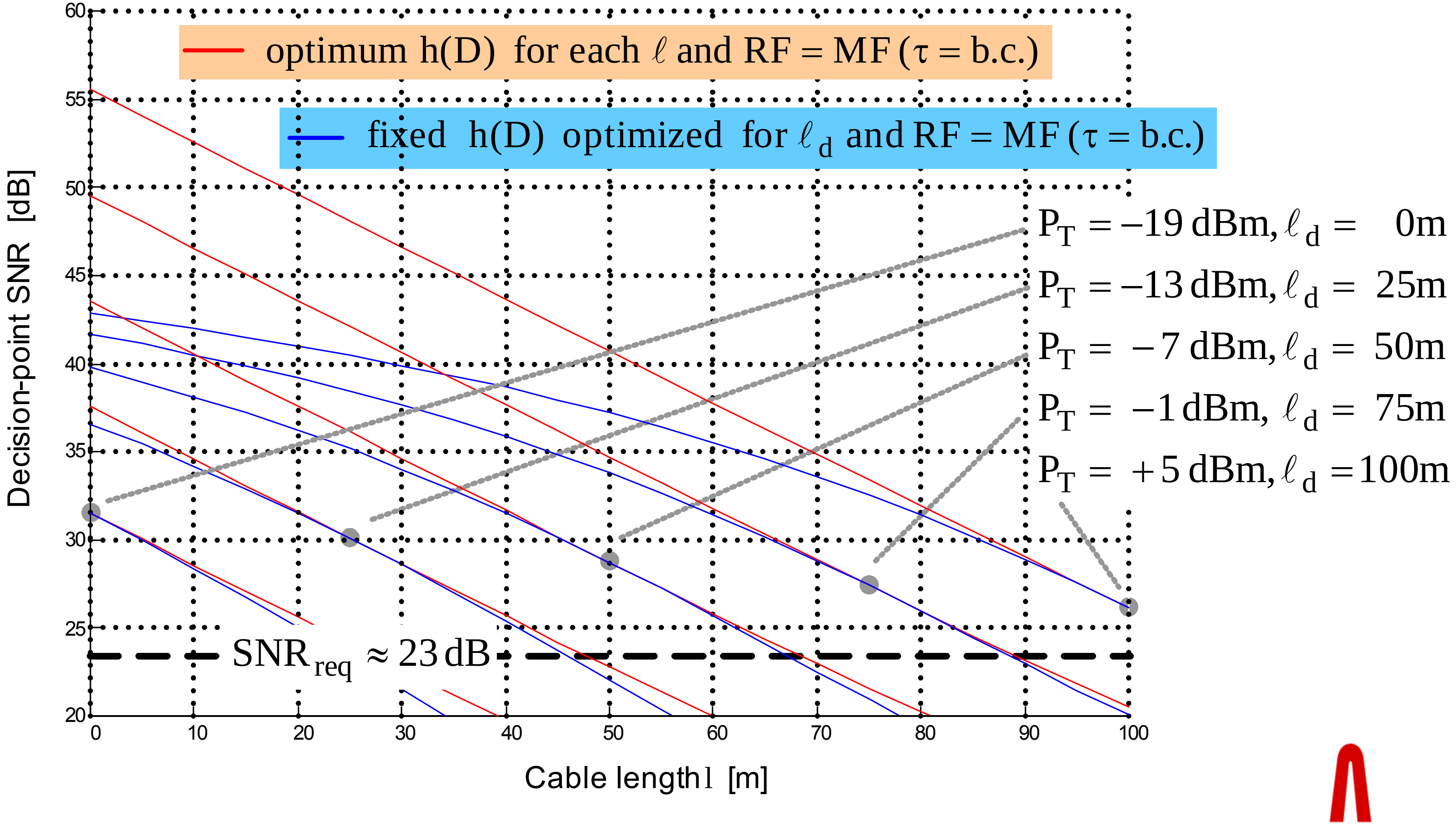


$R_{11} = 80\Omega,\ R_{12} = 8\Omega$
$C_1 = 30\text{pF}$
$R_{21} = 80\Omega,\ R_{22} = 300\Omega$
$C_2 = 12\text{pF}$



SNR vs. cable length

Cable type = "ClassEs" [Model #3(ℓ)]; f_T = 800 Mbaud; TF = "BWF2dcn"; AWGN = -140 dBm/Hz; worst-case ANEXT (P_T=5 dB ,ℓ=100m); inf. mmse FFE



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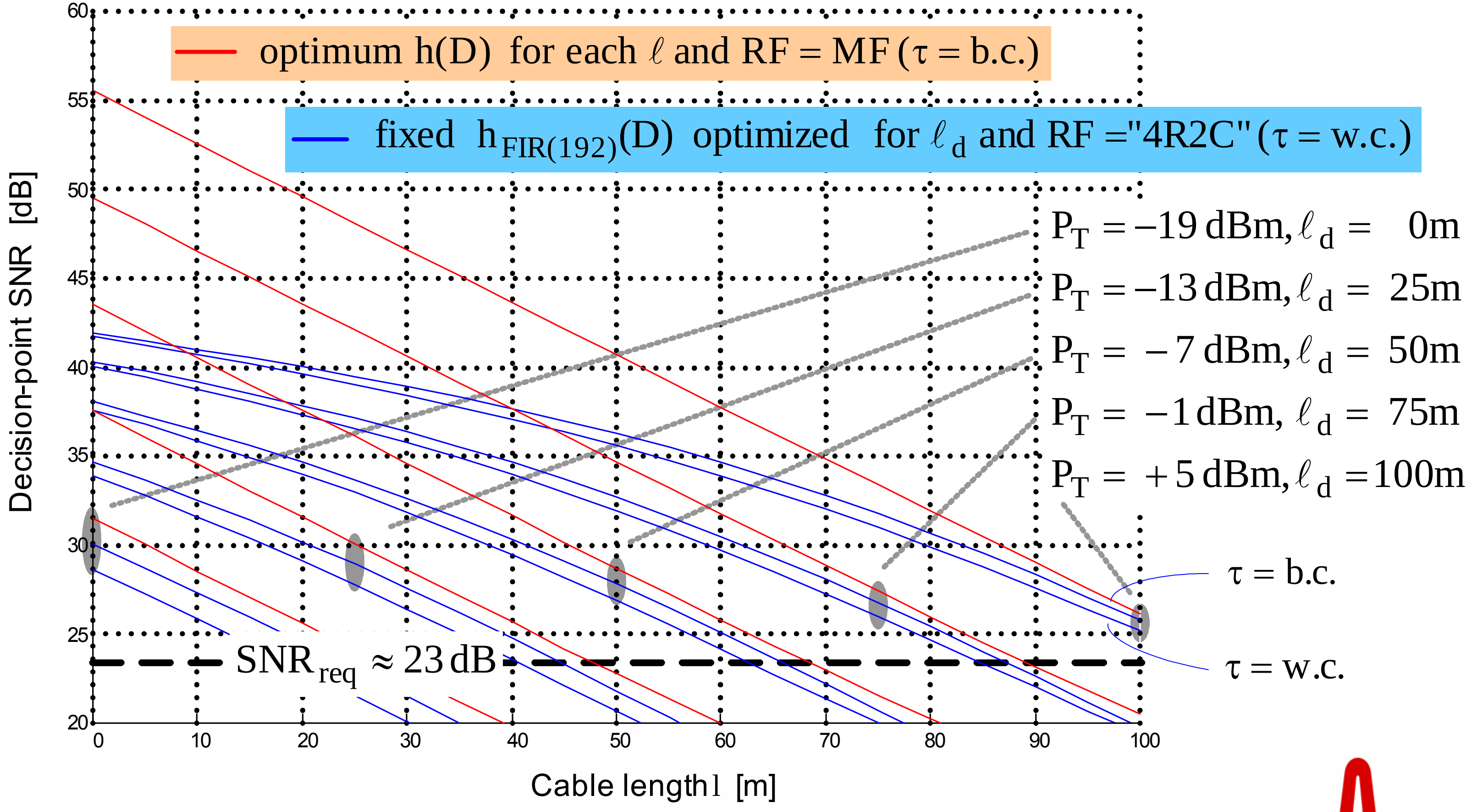

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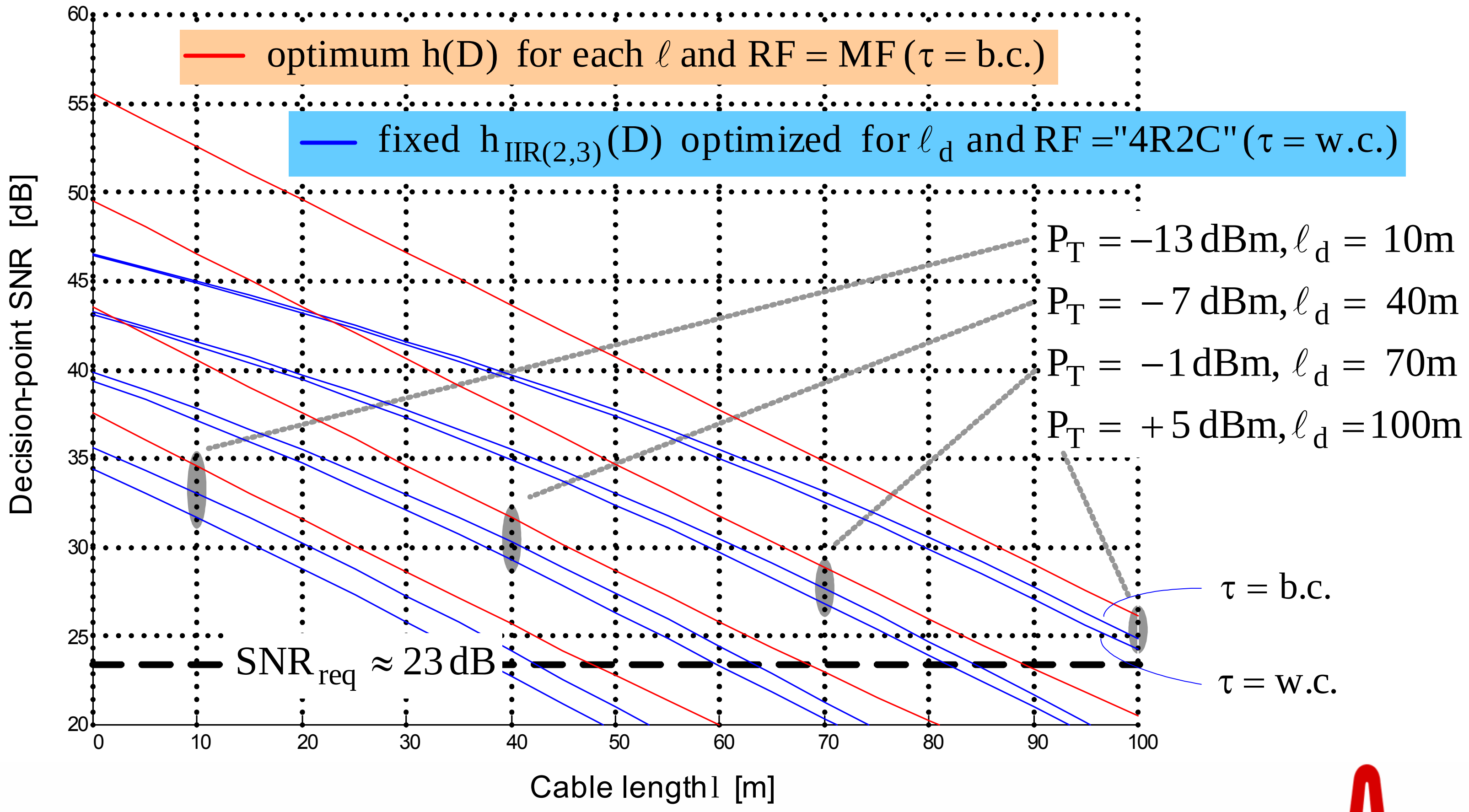


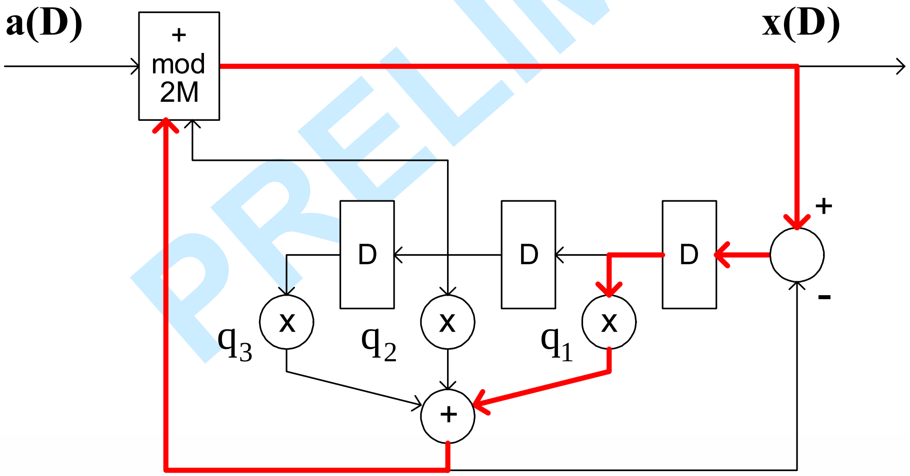
IIR precoding responses $h_{IIR}(D)$

$$h_{IIR(2,3)}(D) = \frac{1-D^2}{1+q_1D+q_2D^2+q_3D^3} = 1 - \frac{q_1D+(q_2+1)D^2+q_3D^3}{1+q_1D+q_2D^2+q_3D^3}$$

	Coeffs			Poles		
	q_1	q_2	q_3	β_1	β_2	β_3
THPF 1 (100m)	$-141/64$	$104/64$	$-26/64$	0.8916	$0.6558+0.1600i$	$0.6558-0.1600i$
THPF 2 (70m)	$-122/64$	$71/64$	$-12/64$	0.9309	0.6785	0.2969
THPF 3 (40m)	$-98/64$	$36/64$	0	0.9195	0.6117	0
THPF 4 (10m)	$-73/64$	$8/64$	$4/64$	0.9356	0.3805	-0.1755

Zeroes

$\alpha_1 = 1, \alpha_2 = -1$



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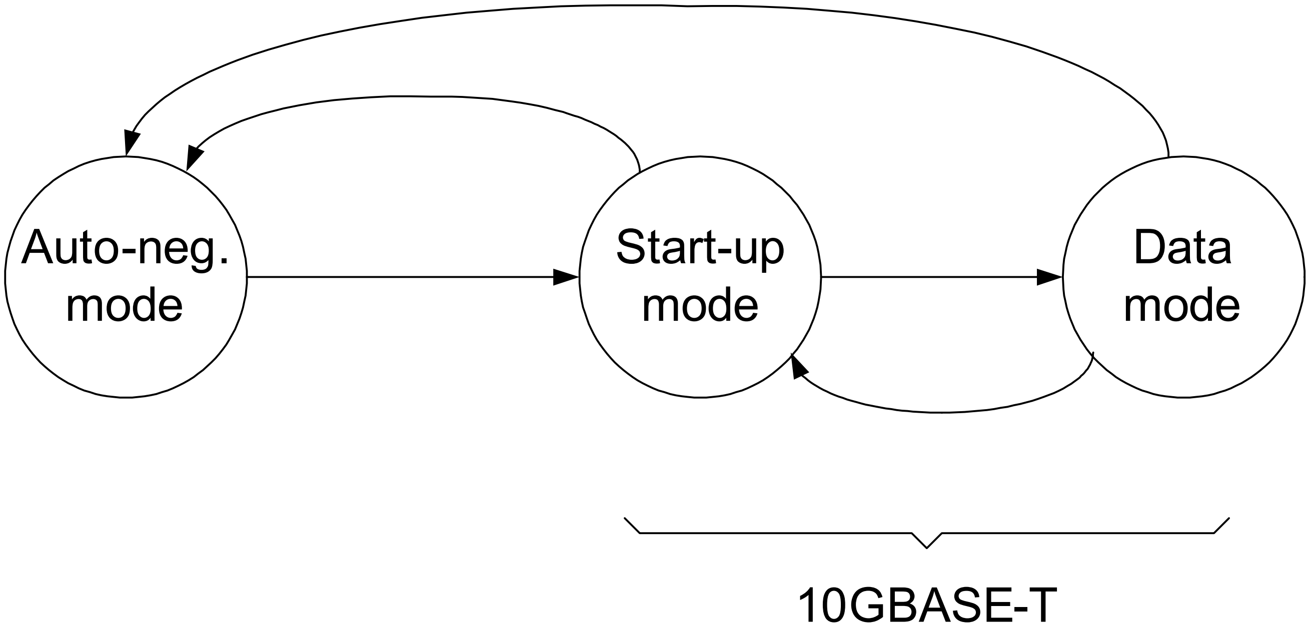
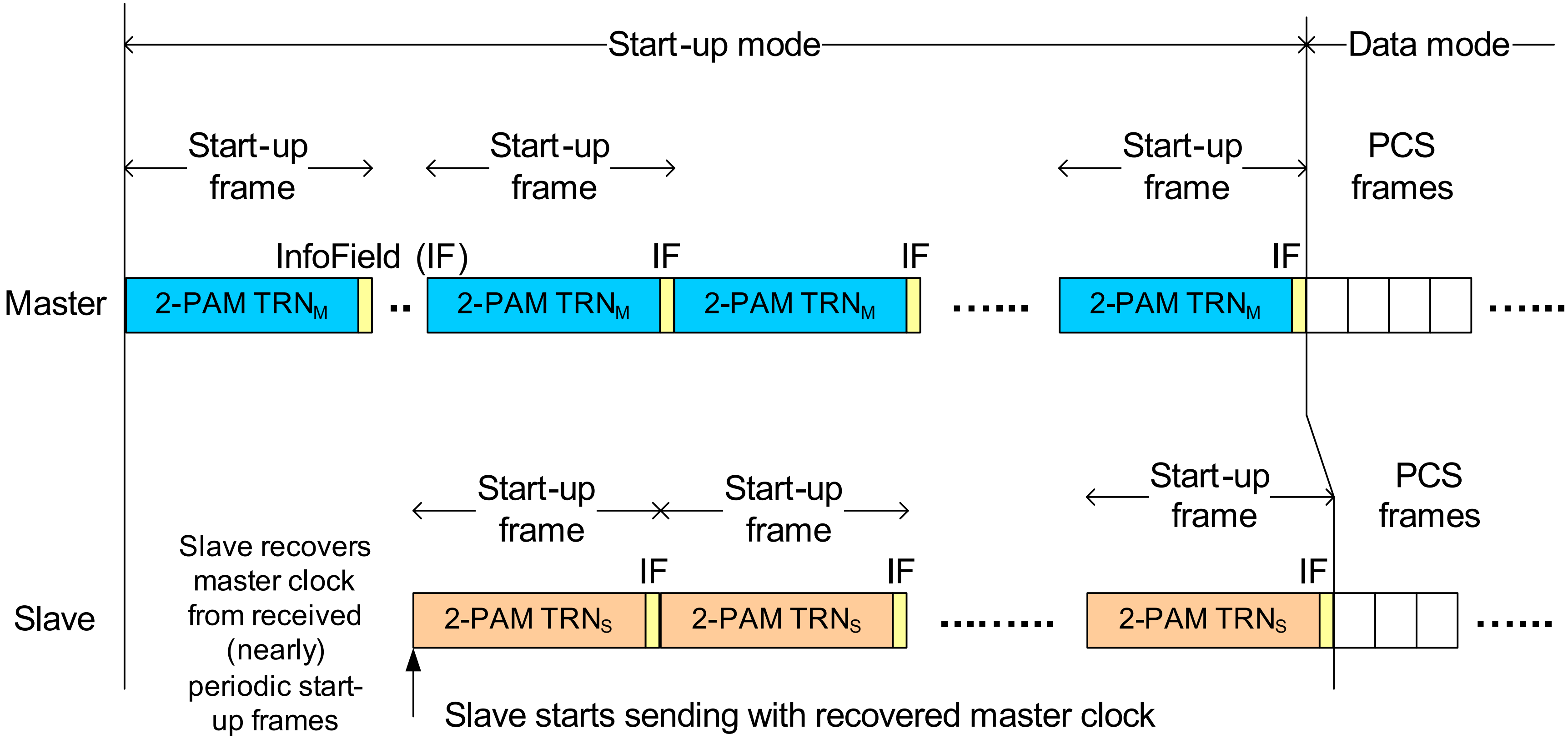
Start-up procedure

Main state diagram



Start-up procedure



<u>Start-up frames:</u> long (e.g., 16K) 2-PAM pseudo random sequences, which are known except for a short InfoField (e.g., 48 bits) at the end. Periodically transmitted during the entire start-up mode. Master and Slave use different sequences.

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Start-up procedure

Contents of the InfoField (IF) in start-up frames

Current transmit gain	4 bit
Current THP filter number	3 bit
Current decision-point SNR	6 bit
Announced transmit gain	4 bit
Announced THP filter number	3 bit
Announced transition to data mode	1 bit
Number of start-up frames until announced values become effective	6 bit
Requested transmit gain	4 bit
Requested THP filter number	3 bit
CRC-14	14 bit
	48 bit

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Concluding remarks

Concluding remarks

- 128-DSQ + LDPC(2048,1723) appears to be best coding & modulation option for 800 Mbaud: offers highest coding gain, lowest LDPC decoding complexity, power-of-2 based mapping and precoding.

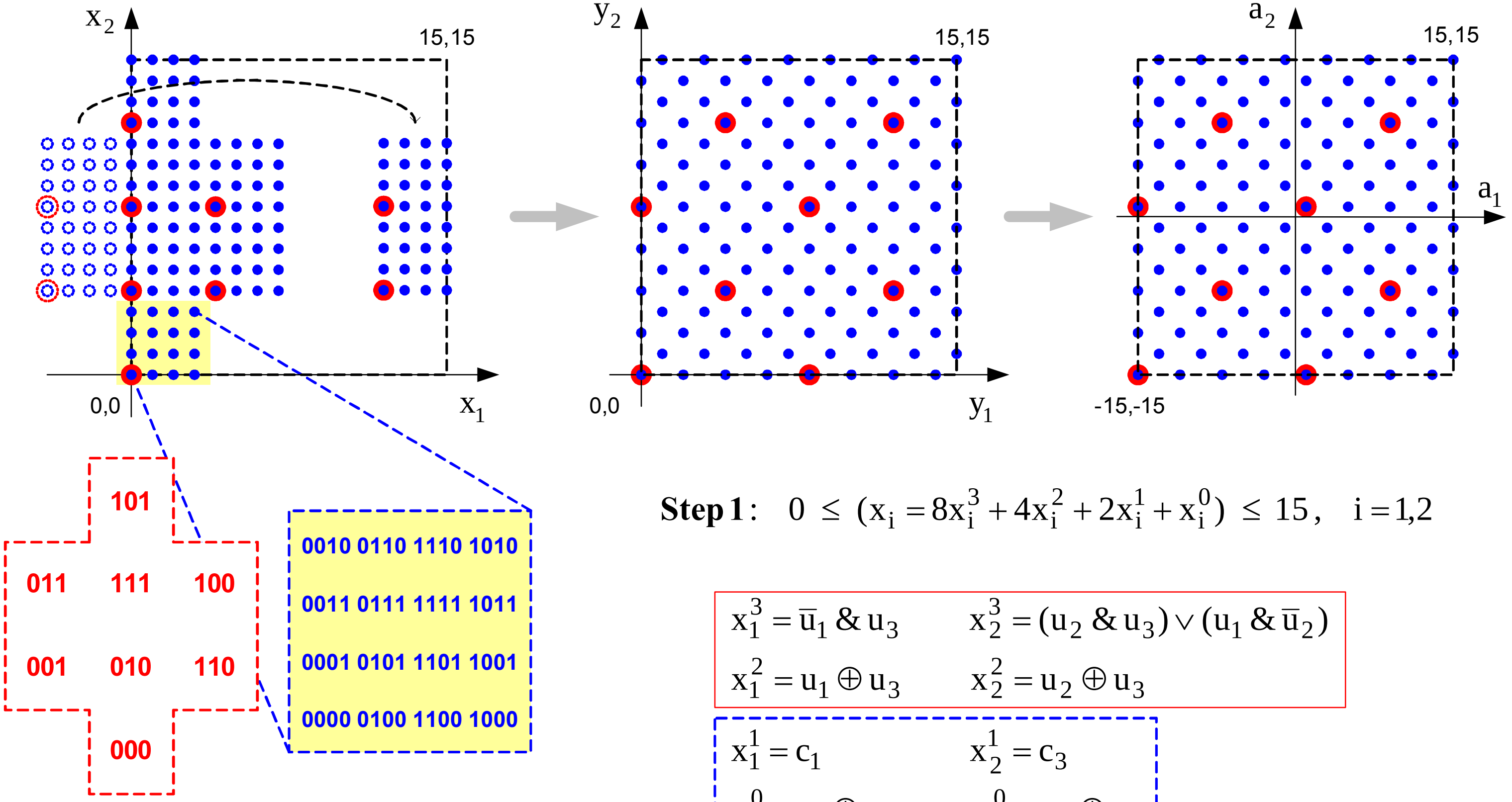
- MTTFPA > 10^4 years seems to be more than adequate. (Ethernet PHYs up to 1 Gbit/s had no enhanced MTTFPA capabilities).

- Small number of fixed THP filters (<8) more than sufficient. Preliminary set of 4 THP filters proposed.

- New start-up concept presented. Emphasis is on simplicity and allowance of long processing delays.

Back-up Slides

128-DSQ bit mapping (ungerboeck_2_0904.pdf)



	101	
011	111	100
001	010	110
	000	

0010	0110	1110	1010
0011	0111	1111	1011
0001	0101	1101	1001
0000	0100	1100	1000

$u_1\ u_2\ u_3$
3 uncoded bits
pseudo-Gray
mapped
(d_H = 1 or 2)

$c_1\ c_2\ c_3\ c_4$
4 coded bits
Gray mapped
(d_H = 1)

Step 1: $0 \le (x_i = 8x_i^3 + 4x_i^2 + 2x_i^1 + x_i^0) \le 15, \quad i = 1,2$

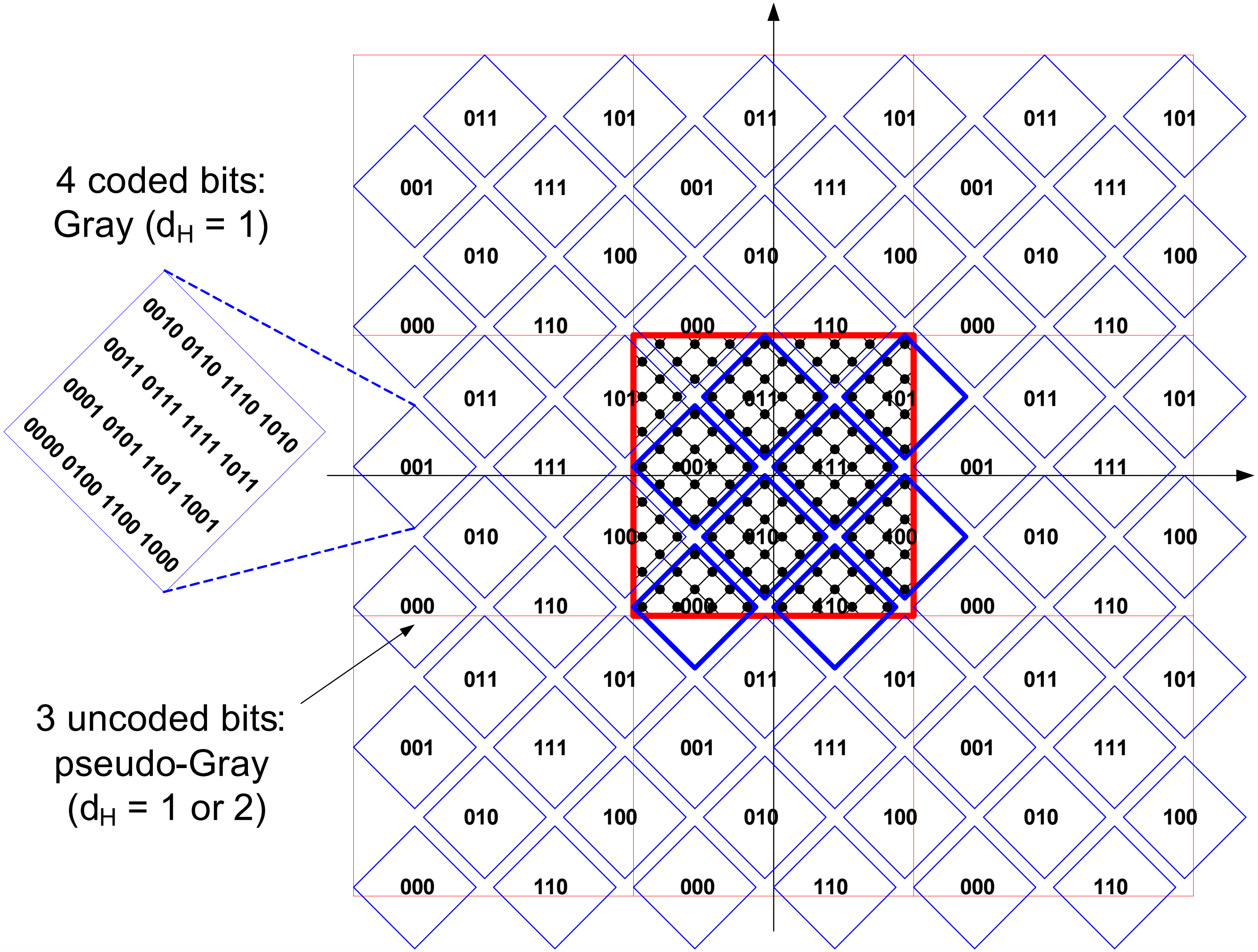
$$x_1^3 = \bar{u}_1 \,\&\, u_3 \qquad x_2^3 = (u_2 \,\&\, u_3) \vee (u_1 \,\&\, \bar{u}_2)$$
$$x_1^2 = u_1 \oplus u_3 \qquad x_2^2 = u_2 \oplus u_3$$

$$x_1^1 = c_1 \qquad x_2^1 = c_3$$
$$x_1^0 = c_1 \oplus c_2 \qquad x_2^0 = c_3 \oplus c_4$$

Step 2: $\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \overbrace{\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}}^{\mathbf{R}} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \bmod 16$

Step 3: $\begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = 2 \begin{bmatrix} y_1 \\ y_2 \end{bmatrix} - \begin{bmatrix} 15 \\ 15 \end{bmatrix}$

Modulo-extended 128-DSQ bit mapping (ungerboeck_2_0904.pdf)



4 coded bits:
Gray ($d_H = 1$)

3 uncoded bits:
pseudo-Gray
($d_H = 1$ or 2)

Basic 128-DSQ with cyclic precoding extensions