In Response to Motion to Remove Loop Timing Option

IEEE 802.3an
October 2005 Interim Meeting

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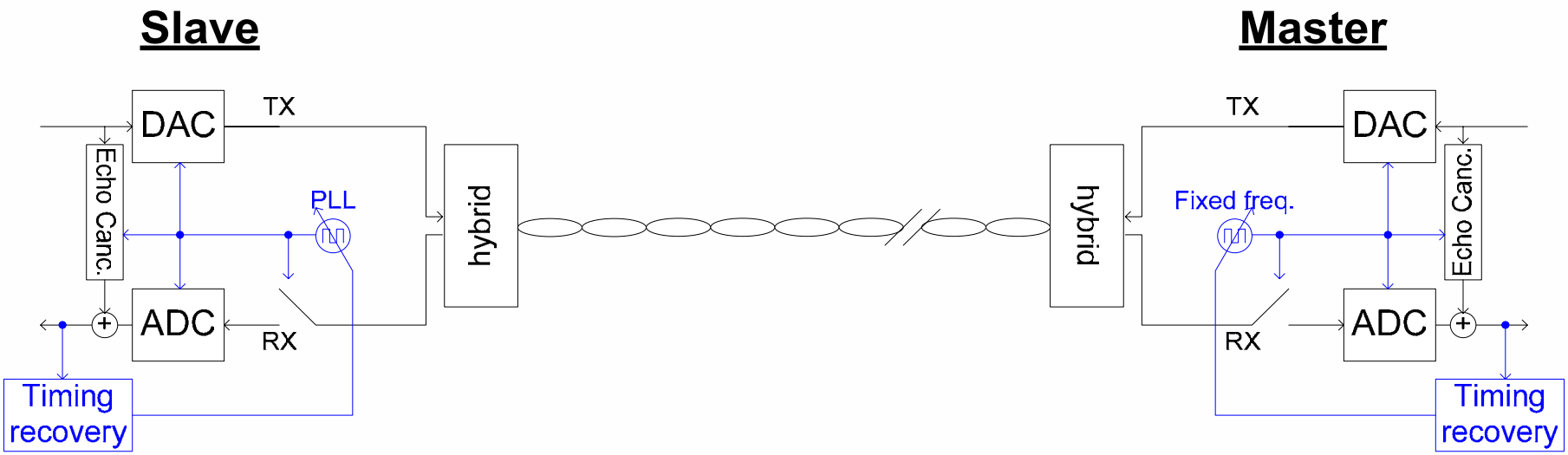
Background: Duplex Transmission

- Duplex = one wire carries transmission in both directions
  - Requires echo cancellation



- Echo (and NEXT) cancellation require the transmitter and receiver to be clocked from the same source

Synchronization Options

- Loop timing: Sampling controlled in analog domain
  - Master Tx and Rx clocked from single free-running source
  - Slave recovers clock and transmits with recovered clock

- Non-loop timing: Sampling controlled in analog or digital domain
  - Oversampled: Receiver samples at a higher rate than symbol rate
  - Baud Sampled: Zero at Fs/2 = 400MHz
    - Can be implemented at receiver

- Standard should avoid specifying the receiver where possible
  - Enforcing loop timing constrains receiver implementations
    - Potentially innovative receiver designs unnecessarily excluded

Non-Loop Timing (NLT) Myths

- NLT does not require zero excess bandwidth transmit spectrum
  - Zero can be implemented at the receiver (pointed out in Nov'04 meeting)
  - Oversampling can be implemented at the receiver
- NLT support is not required. NLT PHYs interoperate with LT PHYs
  - Simple algorithm: LT end is force slave, NLT end is force master
  - If both ends are of the same type: use standard m/s resolution
- NLT requires only negligible overhead on loop timed PHYs
  - One bit in auto-neg
- Nothing has changed in the standard which makes NLT a non-viable receiver option

History

- Two presentations on optional loop timing made to task force
  - powell_1_0904.pdf: Describes implementation challenges with loop timed links and potential benefits with non-loop timed alternatives
  - powell_1_1104.pdf: Describes interoperability between loop timed and non-loop timed PHYs
- Option for non-loop timed links has existed in standard for almost a year
  - Plenty of time for task force members to point out potential faults
  - Motion to make loop timing optional passed unanimously Nov 16,2004
    - Moved by: George Zimmerman Seconded by: Sailesh Rao
    - Y: 35 N:0 A:11

Summary

- Advertise loop timing ability as part of autonegotiation
  - Utilize traditional master/slave resolution if abilities match
  - Force assignment of master and slave if abilities differ
- Permits PHY vendors flexibility in timing recovery implementation
  - Traditional loop timing approach works without modification
  - All-digital approaches can be implemented
  - Avoid specifying receiver implementations in the standard
- Detailed discussion on benefits of non-loop timed links presented over a year ago
  - Changes to the standard do not change relevance of this option