LDPC Evaluation for 10GBT

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1024 Code Family

- RS-Based In Galois Field (2^5)
- 3 Potential Candidates Are (1024,833),(1024,827) And (1024,821) Codes
- All 3 Codes Fit In 800Mhz 4D-12PAM Mapping
- Independent Work Has Been Done By Several Vendors

Column Weight	Row Weight	Codes	Rates	BER Slope Change (Estimated)	BER Slope Change (Simulated)	Complexity
8	32	(1024,845)	0.8252	No Data	~ 1E-9	0.8X
10	**32**	**(1024,833)**	**0.8134**	**1E-12**	**Not seen till 1E-12**	**1X**
11	**32**	**(1024,827)**	**0.8076**	**Should be Below 1E-12**	**Not seen till 1E-8**	**1.1X**
12	**32**	**(1024,821)**	**0.8017**	**< 1E-13**	**Not seen till 3E-11**	**1.2X**
14	32	(1024,809)	0.7900	No Data	No Data	1.4X
30	32	(1024,783)	0.7646	No Data	No Data	3X
32	32	(1024,781)	0.7626	1E^-23	No Data	3.2X

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BER Requirement

- Neighboring Codes In The Same Family Offer Similar Performance
- As Column Weight Increases:
  - BER Performance Improves
  - **Error Floor Also Gets Pushed Down**
  - Complexity Increases, Too
- BER Requirement Is The Key Factor To Select The Optimal Code, But Simulations In The Low BER Region (Below 1E-12) Take Very Long Time
- Error Floor Estimates Provide A Good Indicator To Where The BER Curve May Start To Bend
- Reference:
  - "Error Floors of LDPC Codes", by Tom Richardson

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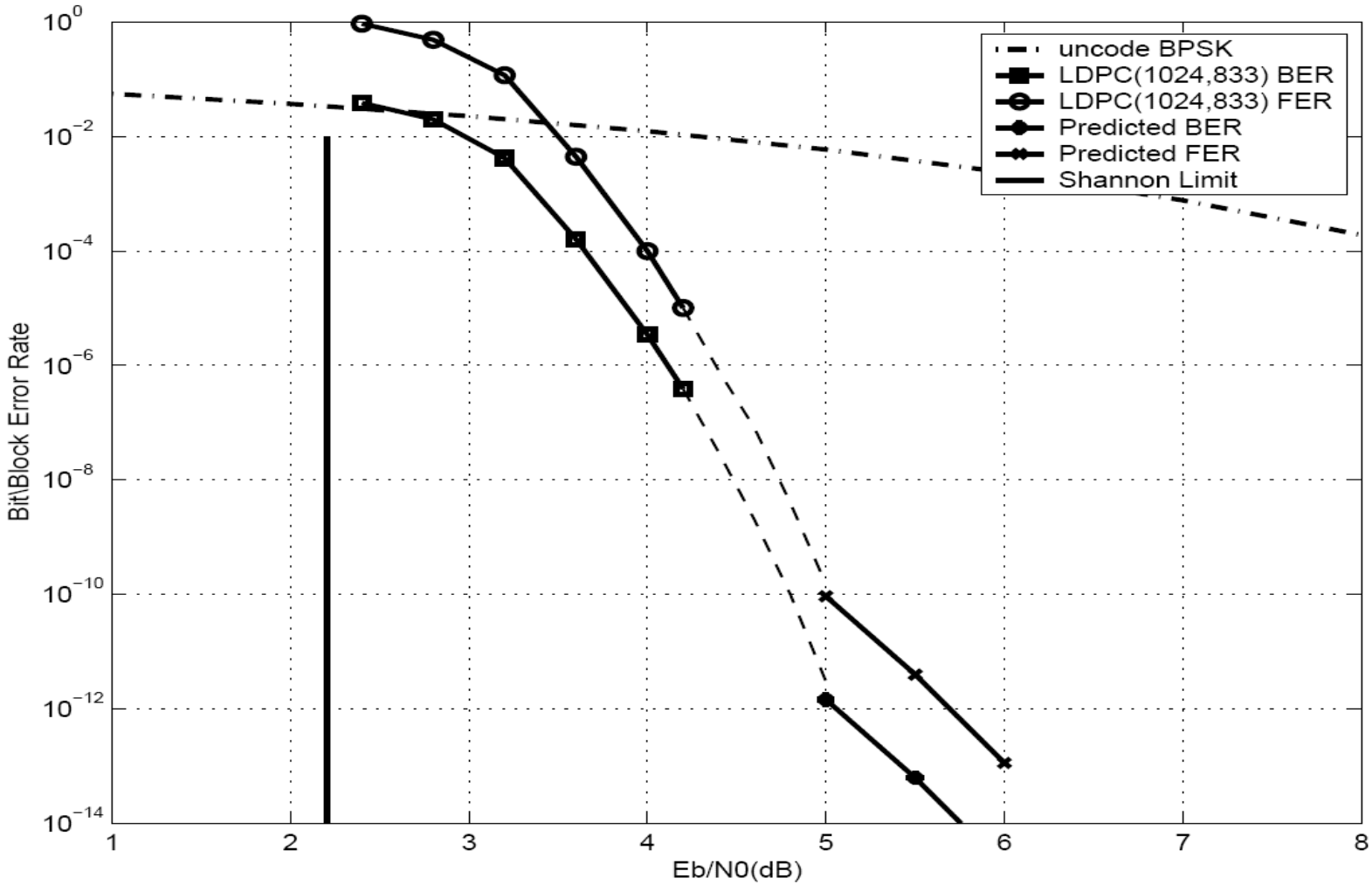
1024,833 Error Floor Estimate



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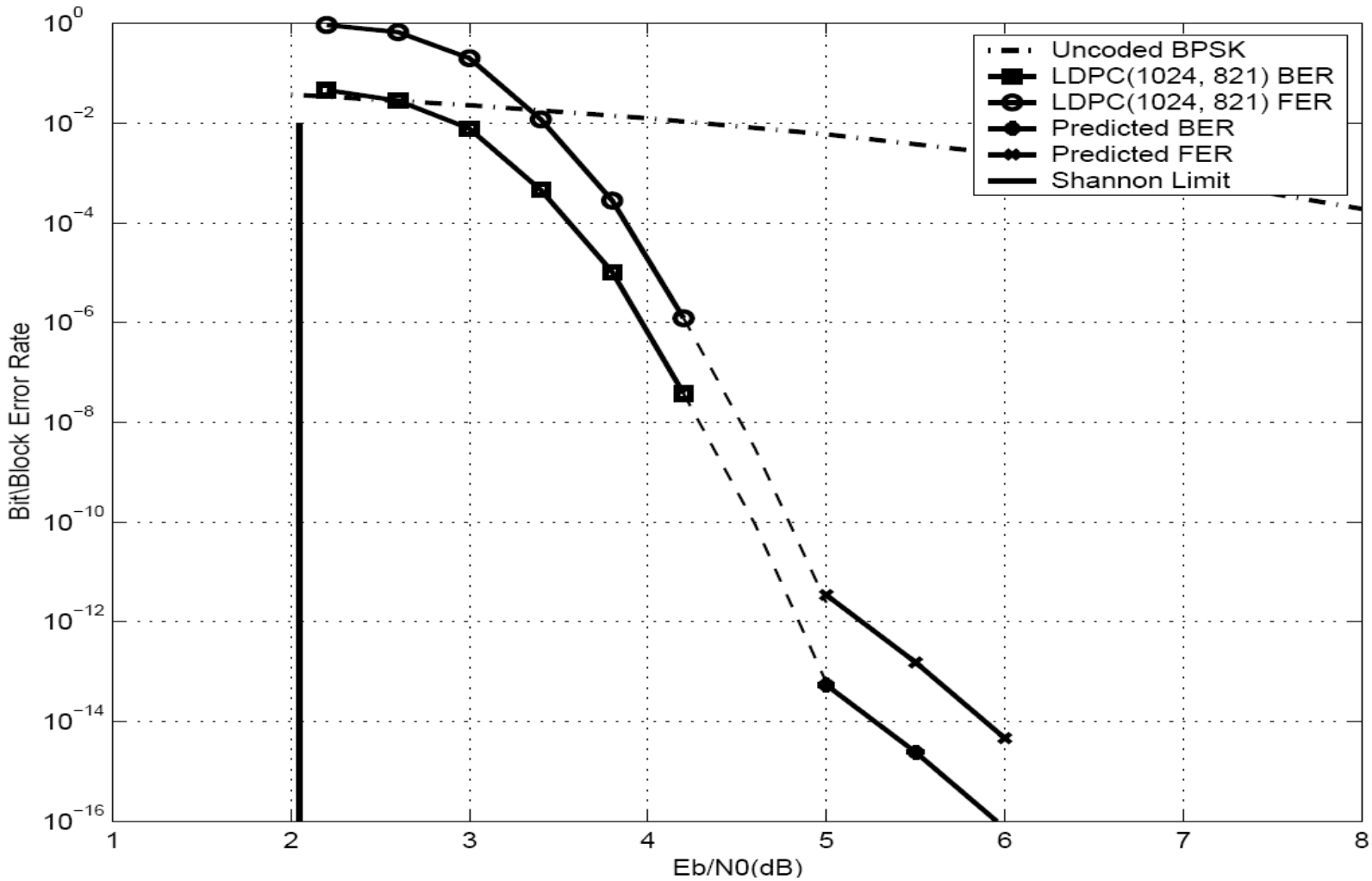
1024,821 Error Floor Estimate



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Fixed Point Simulation for (1024,821)

- Extrapolated Required SNR
  - 24.2dB at 1E-12 For Fixed Point
  - 23.7dB at 1E-12 For Floating Point
- 0.5-0.6 dB Loss From Fixed Point Simulation To Floating Simulation
  - Fixed Point Simulation Using 5 Bits Precision And 4 Bit Look Up Table
  - Complexity Penalty Compared To (1024,833) Code May Not Be Less Than 20% If It Needs More Than 5 Bits Of Precision Or 4 Bits Of Look Up Table

Note : Floating Point Simulation Is Provide By NEC

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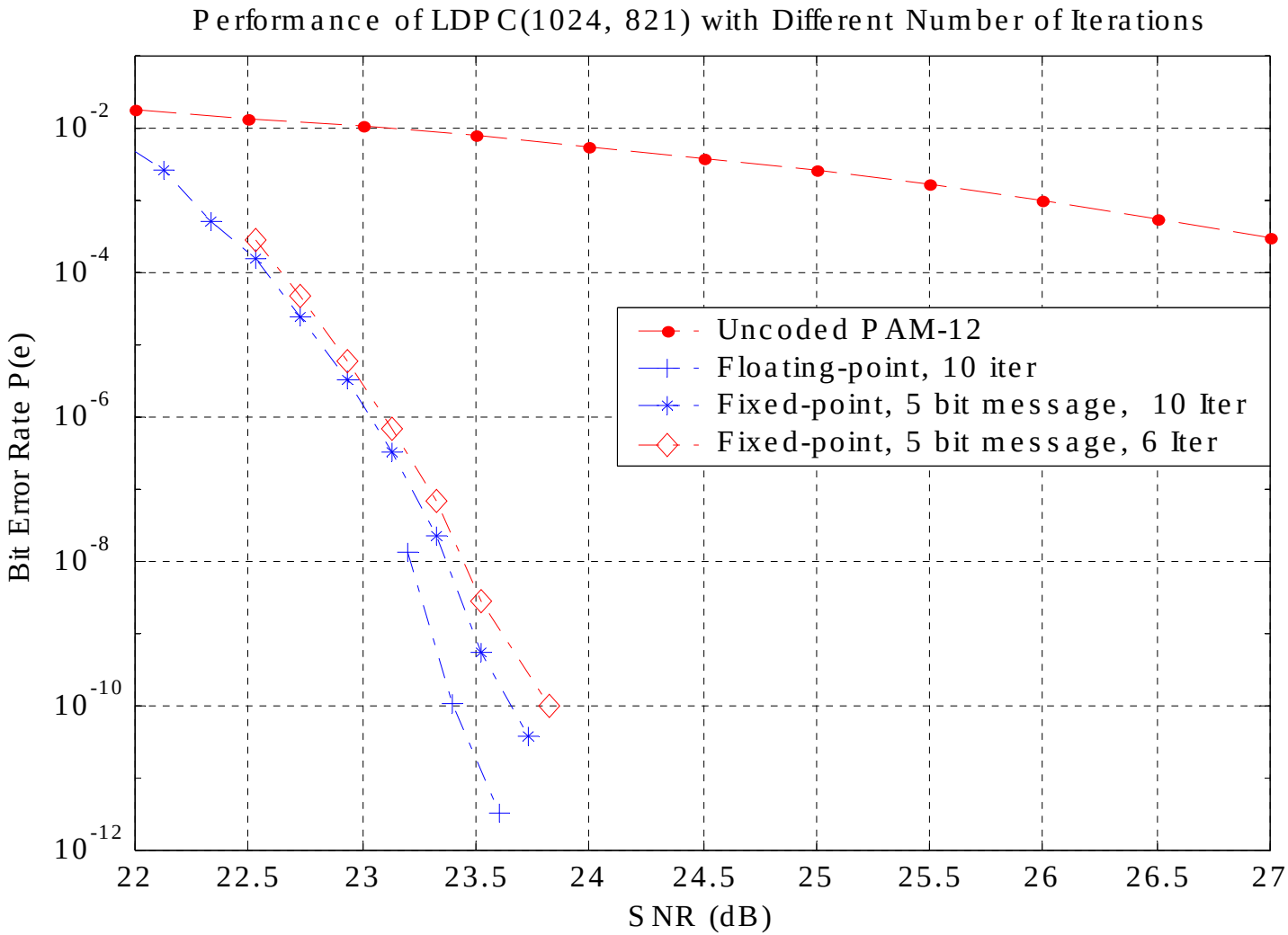
LDPC(1024, 821) W/PAM12 Modulation



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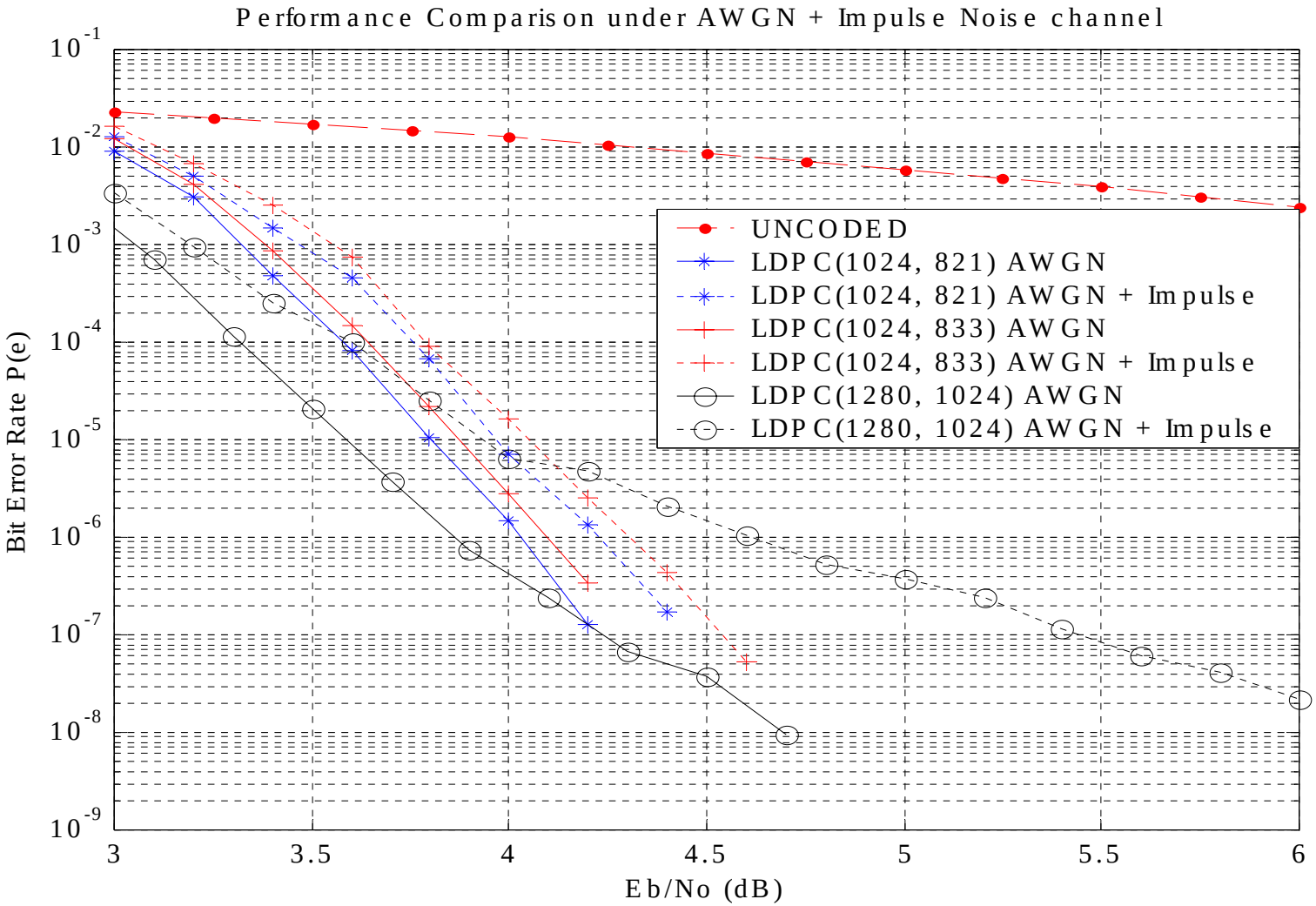
Impulse Noise Simulation

- RS-based LDPC Is Less Sensitive To Impulse Noise Than IrLDPC
- Simple Impulse Noise Is Generated With Burst Length Of 4 And Periodically Applied To AWGN Channel (Every 511 Bits)

Performance Under AWGN + Impulse Noise



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Performance Matrix

	(1024,821)	(1024,827)	(1024,833)
BER Slope Change Est.	5E-14	4E-13	1E-12
FER Slope Change Est.	5E-12	4E-11	1E-10
Intrinsic Latency	160n sec	160n sec	160n sec
Number Of Edges	12288	11264	10240
Frame Rate	800 Mhz	800 Mhz	800 Mhz
Hamming Dist. Lower Bound	14	12	12

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Summary

- (1024,821), (1024,827) And (1024, 833) Are All Good Candidates For Meeting The 10GBASE-T Requirement In Terms Of:
  - Good Coding Gain
  - Small Decoder Latency
- (1024, 821) Has A Lower Error Floor With 20% Higher complexity Then (1024,833) Code
- (1024, 833) Code Is 20% Less In Hardware But Marginal Performance In Our Floor Estimate
- (1024, 827) Could Be A Good Compromise
  - Floor Slope Change Should Be Below 1E-12
  - Only 10% Overhead Compared To (1024,833) Code
  - Performance Should Be Between (1024,833) And (1024,821) Code

Conclusion

All In All,

- We Should Work Together And Focus On 1024 Code Family To Speed Up Standard Development
- We Need More Simulation Data Of The BER Slope Below 1E-12 Before We Can Choose One Of The Three Codes As The Standard
- Standard Must Offer Us Good Performance And Less Complexity, In Which Performance should The First Priority

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BACK UP

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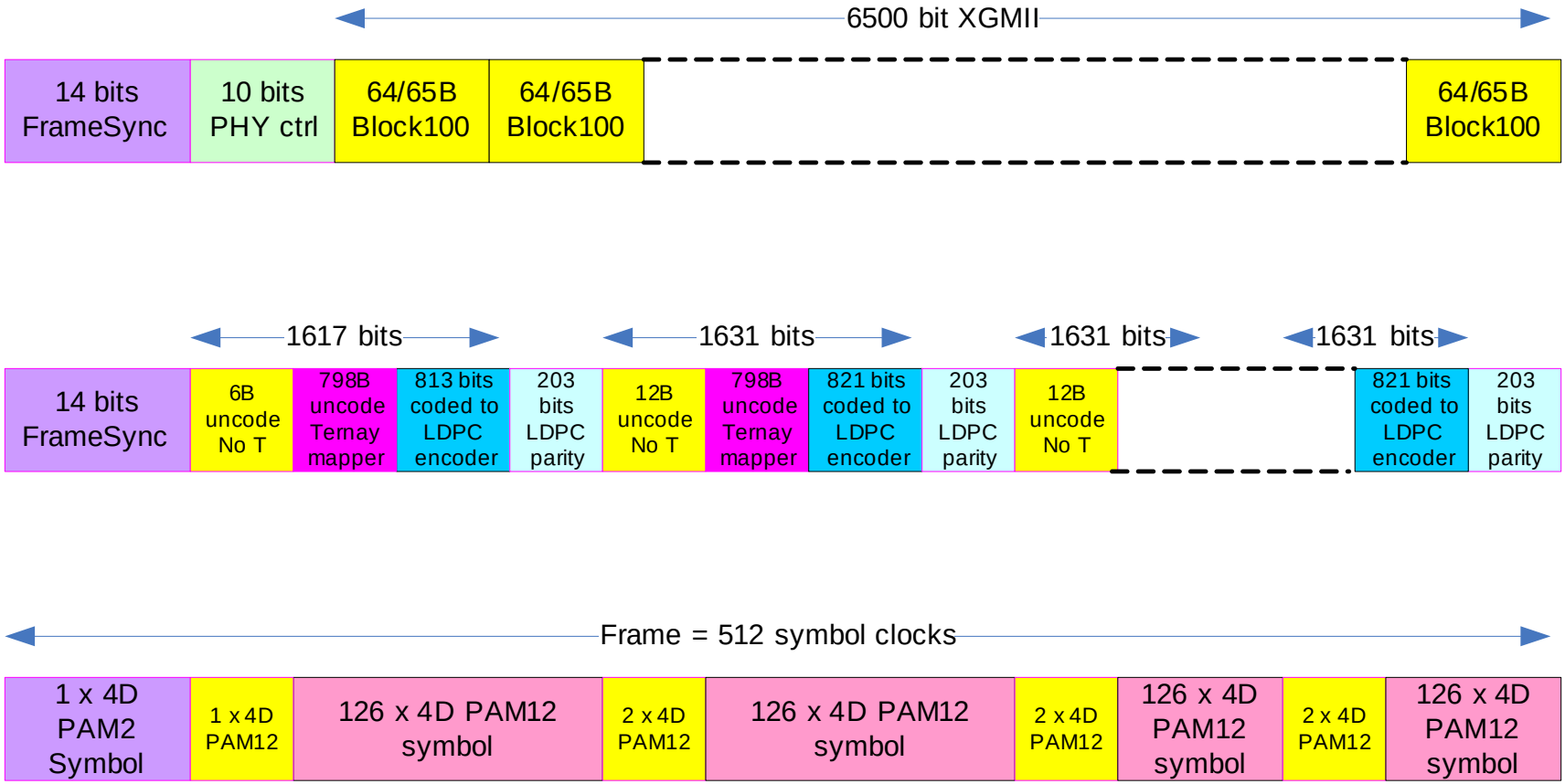
Framing Format



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