4-Channel Sampling Considerations for 10GBASE-T

IEEE 802.3an Interim Meeting

September 2004

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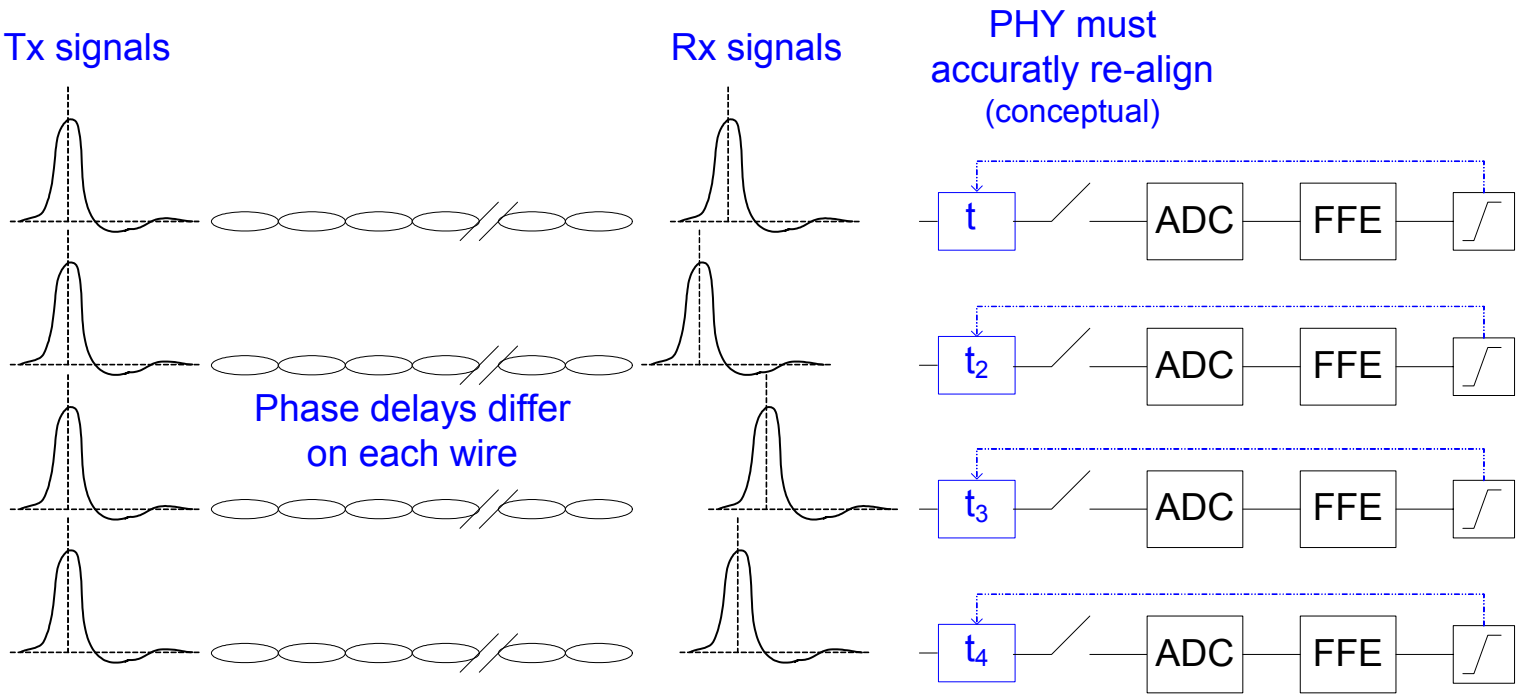
Agenda

- **4 Channel Sampling**
  - Challenges & alternatives
- **Phase Insensitive Sampling**
  - Zero excess bandwidth channel
- **4 Channel Sampling with Single Free Running Clock**
  - Modified master/slave
- **Summary/Conclusions**

4 Channel Sampling

Traditional Analog/Digital Phase Compensation



- **Optimal baud spaced samples are ≈ at pulse peak**
- **Independently adjusted phase for each channel**

— Same frequency

Connecting everything™

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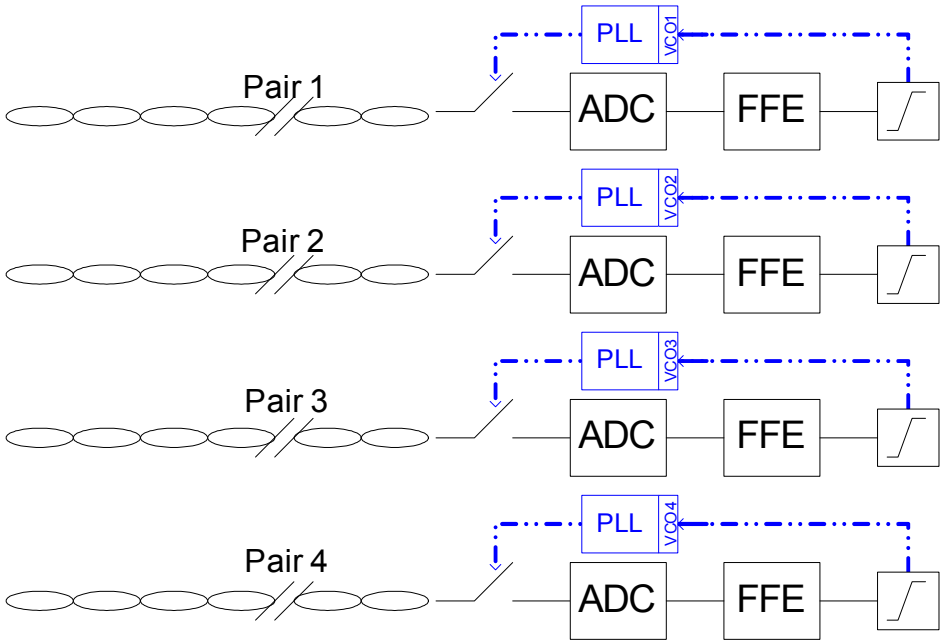
Implementation Challenges

- **Approach 1: independent PLL per channel**

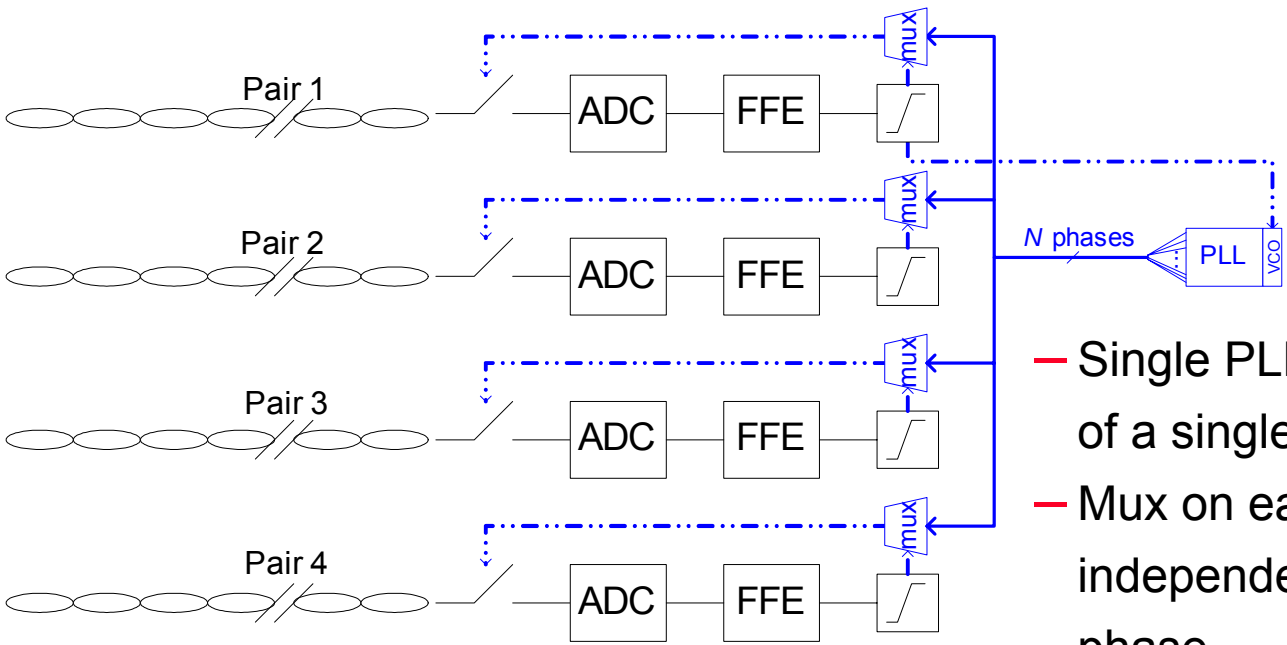


– Each PLL independently adapts to optimal frequency/phase

- **Theoretically possible but has implementation challenges**
  - Difficulties with multiple VCOs on same die – interactions almost inevitable
  - Injection locking has been shown to be the root cause failure mechanism in previous products

Implementation Challenges

- **Approach 2: Single VCO with phase selector**

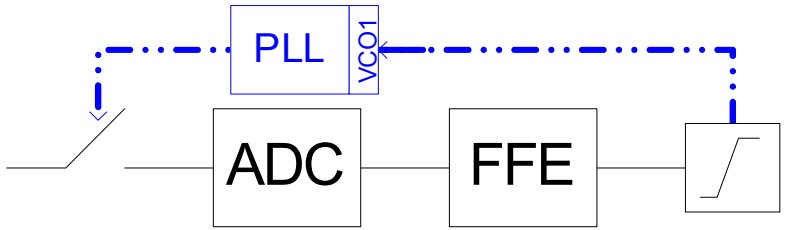


- Single PLL generates *N* phases of a single recovered clock
- Mux on each channel independently selects optimal phase

- **50~60dB Echo suppression requires very large number of phases: $N_{10G} >> N_{1G}$**
  - Phase steps cause transient echo cancellation errors

Implementation Challenges

- **Decision directed timing recovery has ADC+FFE latency in PLL loop**

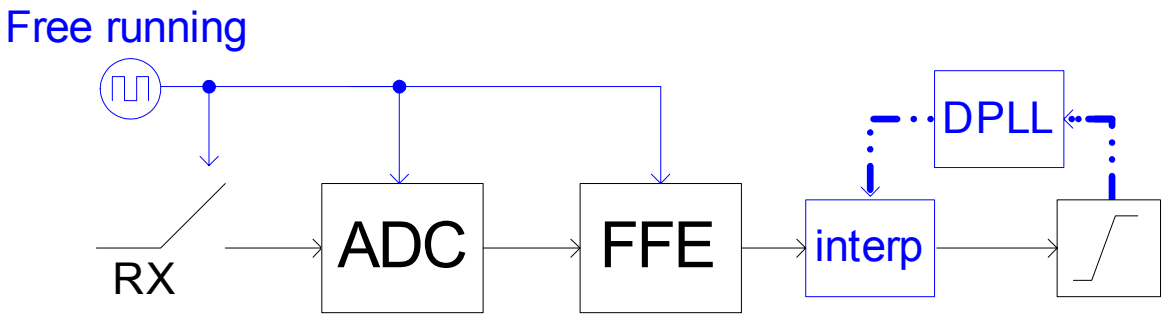


- **Jitter tolerance and latency are opposing goals**
  - Latency requires PLL bandwidth to be reduced
  - Jitter tolerance requires PLL bandwidth to be increased

- **Low jitter requirement may constrain design options for ADC, FFE, slicer**
  - Eg: FFT based filters offer lower complexity but higher latency

System Solution to Implementation Challenges

- **Approach 3: Move timing recovery after FFE:**
  - Digital interpolator instead of analog VCO or phase selector



- **Removes latency restriction on ADC and FFE** **Advantage #1**
  - Opens opportunity for design innovation
- **Free running clock removes requirement for high precision phase selector** **Advantage #2**

System Solution to Implementation Challenges

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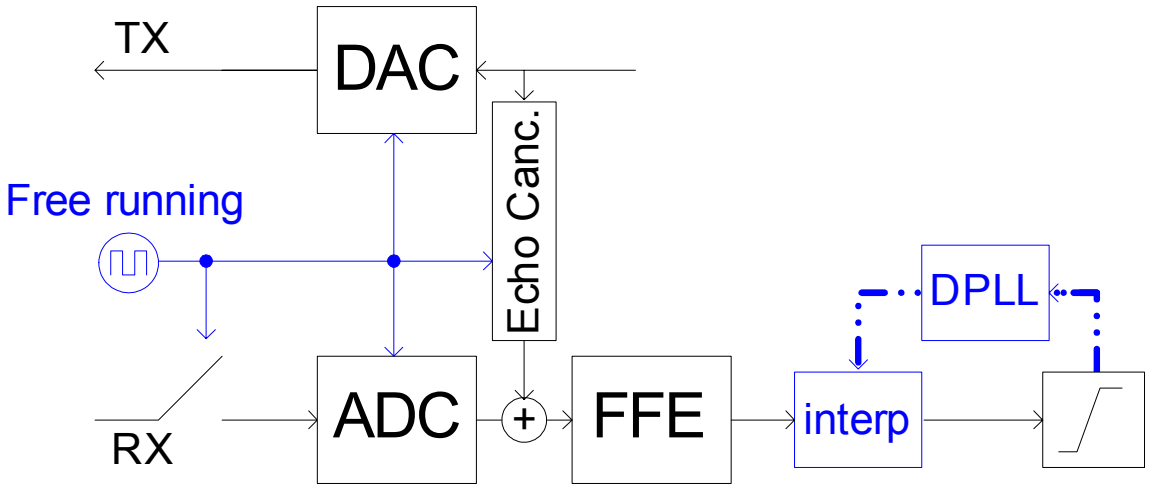
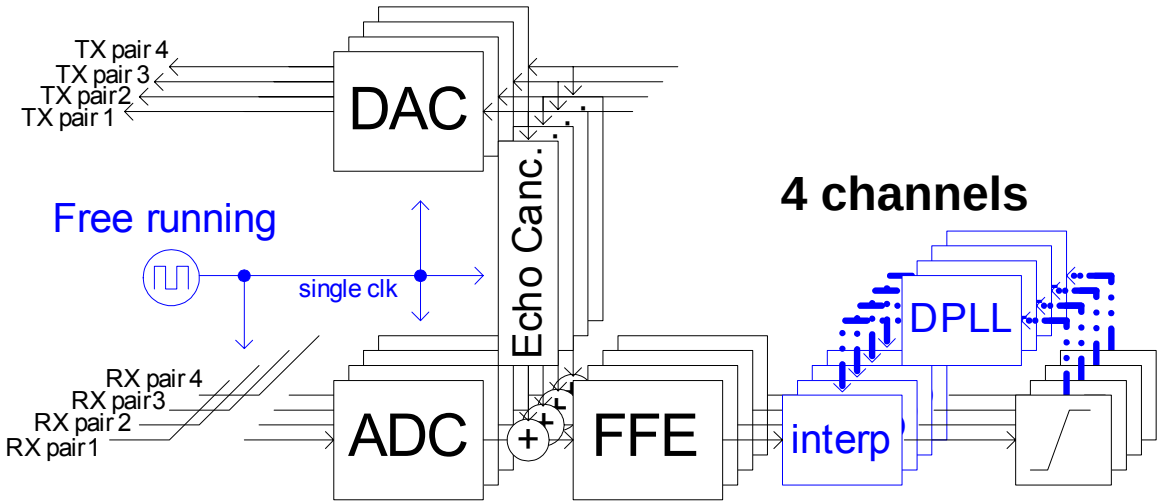


- **ADC, DAC, echo canceller, FFE all on same clock**
  - Removes need for FIFOs

Advantage #3

System Solution to Implementation Challenges

- **Approach 3: Move timing recovery after FFE:**
  - Digital interpolator instead of analog VCO or phase selector



- **FFE in each channel performs independent phase adjustment**

Advantage #4

  - Analog PLL per channel not required
  - Removes requirement for large phase selecter
  - Single clock for all 4 channels (may want intentional fixed offset)

Transmitter Requirements

- **Standard does not need to specify receiver implementation**
  - All three options can be permitted with appropriate transmitter
- **Two main transmitter features must be adopted by task force to permit option 3:**
  1. **Zero excess bandwidth channel**
     - Permits (but does not require) digital timing recovery after equalizer
  2. **Slave *optionally* transmits with recovered clock**
     - Permits (but does not require) single free running clock at both ends of link
- **Neither of these features precludes implementation options 1 or 2**

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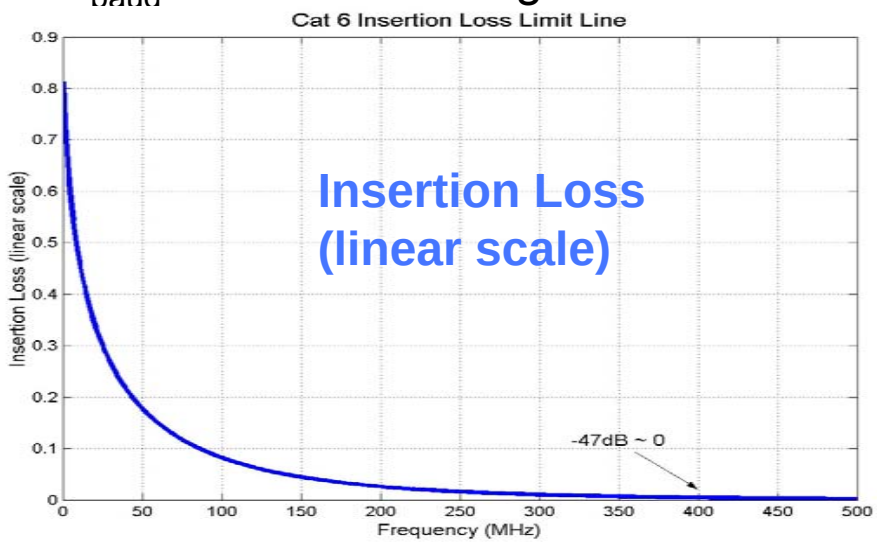
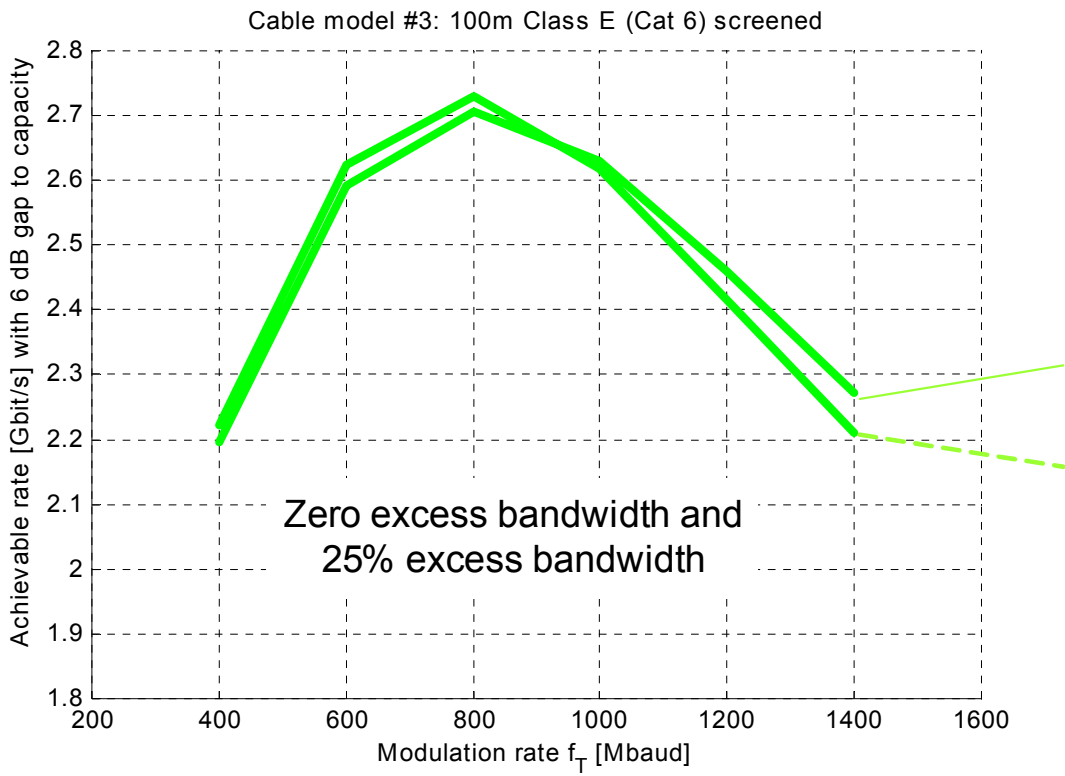
Zero Excess Bandwidth

- **Well known technique for phase insensitive sampling**
  - Signal bandwidth constrained to < $F_{baud}/2$
  - Permits sampling phase to be adjusted digitally (through interpolation)
- **Severe insertion loss channel is already close to a zero excess bandwidth channel**
  - Additional zero at $F_{baud}/2$ does not change much



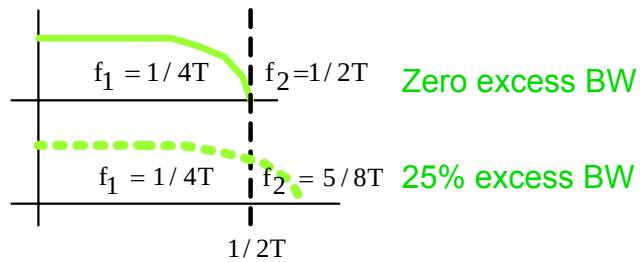
Tx Filtering for Phase Insensitivity: *Minimal Rate Loss*

- **Cable Model #3: 100m Class E (Cat 6) screened**
- **TX PSD with cosine roll-offs: zero excess bandwidth and 25% excess bandwidth**
- **Modulation rates f_T=1/T = 400 to 1400 Mbaud; P_T=10dBm, N_0=-135 dBm/Hz, Γ = 4 (6 dB).**



Negligible rate loss with zero excess bandwidth filter

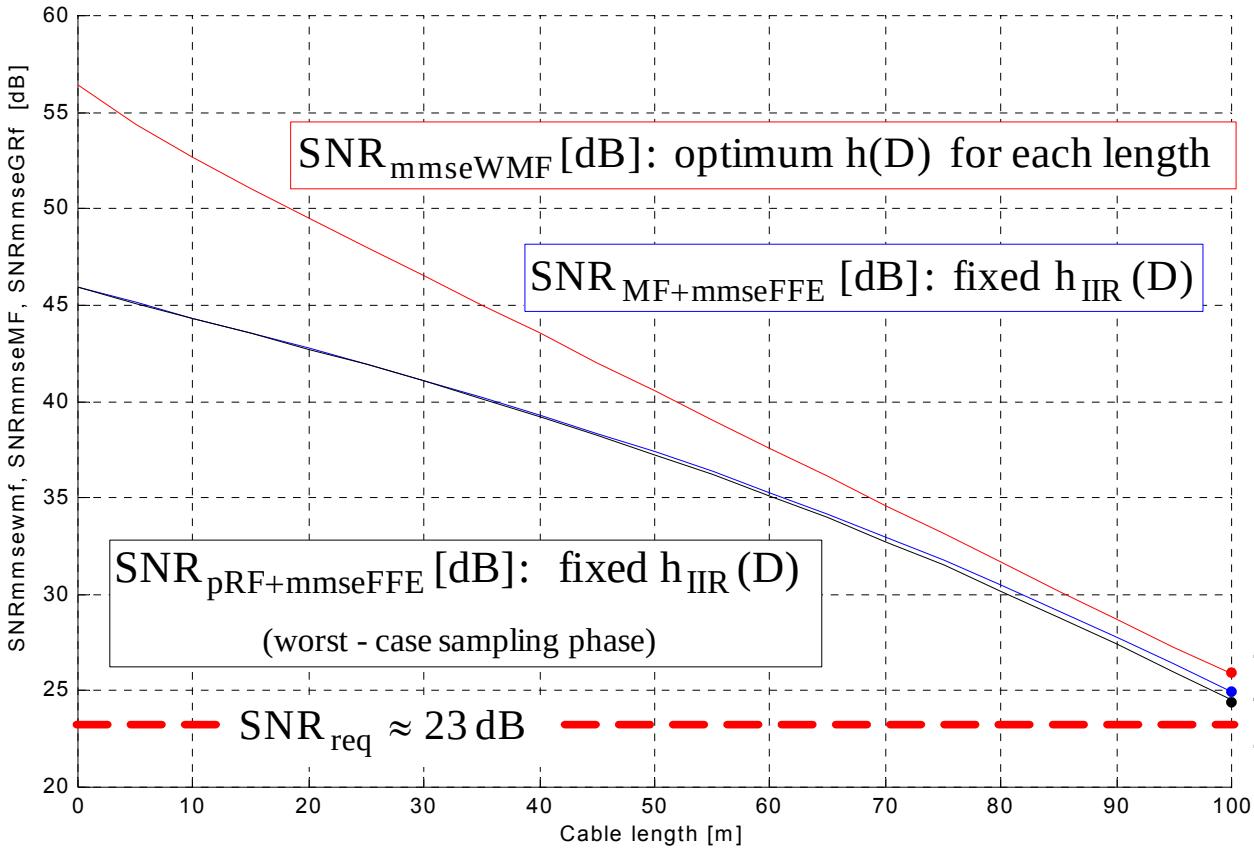
Shapes of $S_T(f)$



Tx Filtering for Phase Insensitivity: *Minimal SNR loss*

Cable type = "ClassEs"; f_T = 820.72 MBaud (12-PAM); practical TX filter;

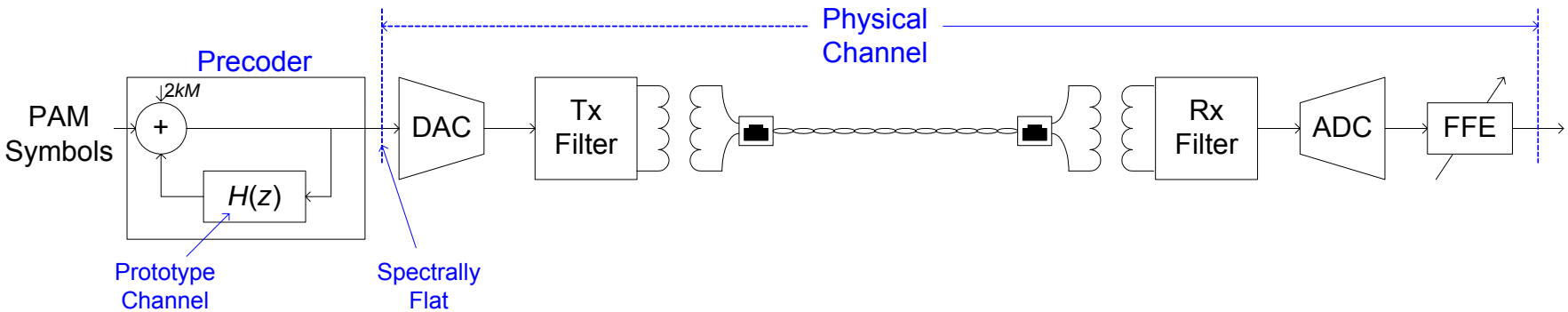
P_T = 5 dBm; alien NEXT + AWGN (-140 dBm/Hz); opt. FFE



Negligible SNR loss with zero excess bandwidth filter

Implementation: Background

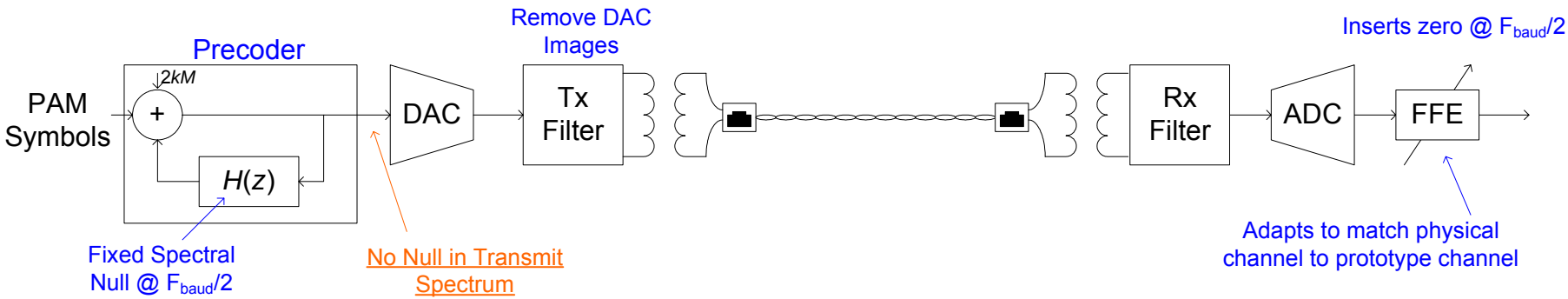
- **Phase insensitive sampling**
  - Single free-running PLL for all four channels
- **Define:**
  - "Physical Channel" ≡ Tx filter + cable/connectors + FFE
  - "Prototype Channel" ≡ precoder feedback filter



- **Fixed prototype channel, adaptive physical channel**
  - FFE will adapt to make physical channel = prototype channel

Implementation of Zero Excess Bandwidth Channel

- **A combination of *THP*, *Tx filter*, *cable*, *Rx FFE***
  - THP (fixed, digital): places null in prototype channel $H(z)$ at $F_{baud}/2$
  - Tx Filter (fixed, analog): gradual roll-off eliminates images
    - Does not need to implement spectral null (see ungerboeck_1_0704.pdf slide 19)
  - Cable (fixed, analog): approx inverse of THP response
  - Rx FFE (adaptive, digital): adapts to make channel = prototype channel
    - Implements spectral null



Conceptual "equivalent" channel: actual implementation may differ

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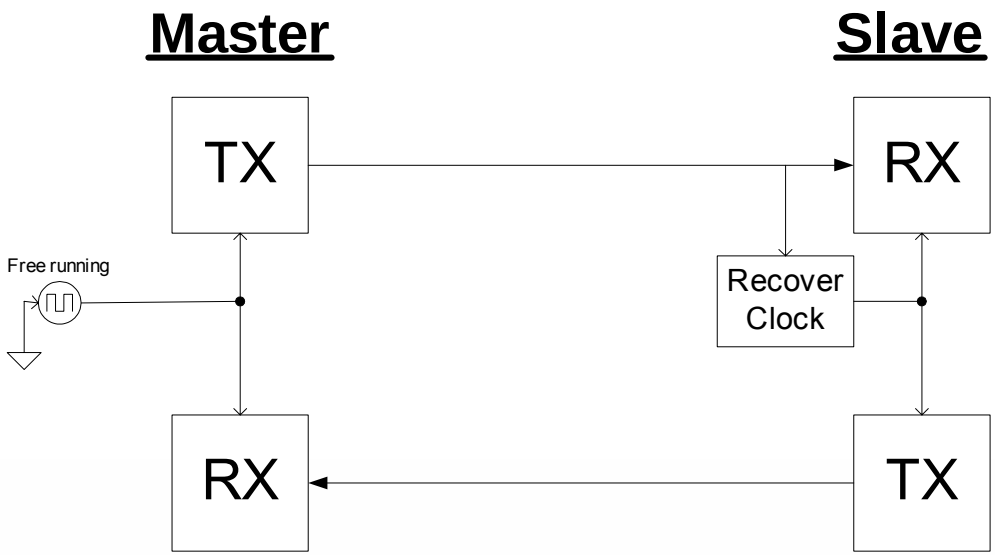
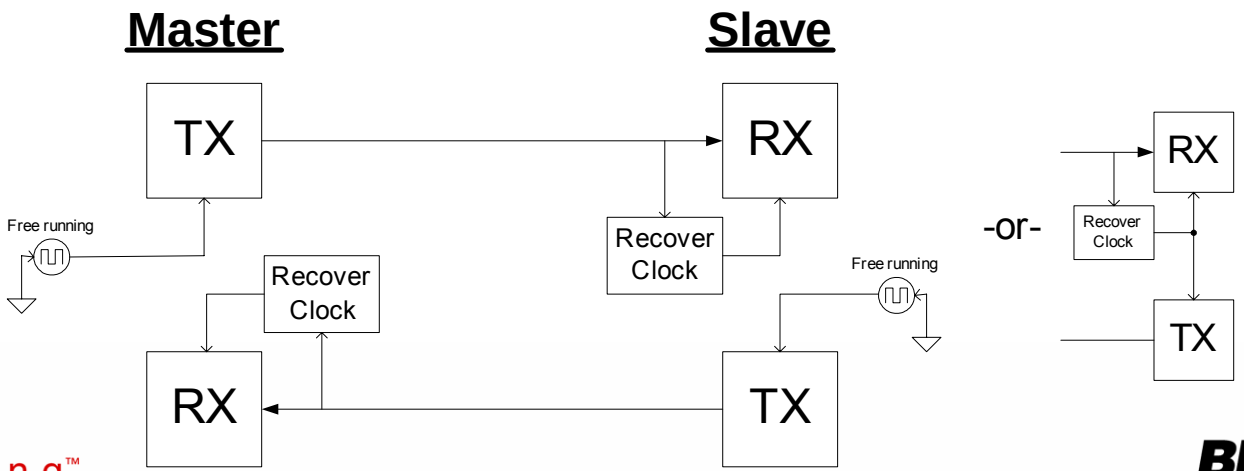
Master/Slave Full Duplex Communications

- **Only used in 1000BT**
  - 10BT, 100TX, 1000X do not have master/slave concept
- **Asymmetric PHYs**
  - Slave transmits with recovered clock
  - Each PHY must support both master and slave modes



Modified Master/Slave Configuration

- **Modified and traditional master/slave sides interoperate**
  - modified master ↔ traditional slave traditional master ↔ modified slave
- **Symmetric configuration**
  - Both PHYs can have identical configurations, if desired
  - Permits phase insensitive timing recovery
  - Permits single free running clock for all 4 channels



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Summary

Challenges of Traditional 4-Channel Sampling

1. Independently controlled phase for each channel
2. Multiple VCO's have interaction difficulties (injection locking, jitter coupling)
3. Phase selectors require large number of phases due to large echo
4. Analog PLL loop delay restricts ADC & FFE implementation options

Advantages of Phase Insensitive Sampling

1. No restrictions on ADC/FFE implementation
2. Single VCO, no high precision phase selector
3. Single free running clock for all 4 channels
4. ADC, DAC, echo canceller, FFE for all 4 channels in same clock domain
5. Transmitter requirements do not preclude traditional 4-channel sampling

Conclusions

- **Common 4-channel sampling approaches used in gigabit phys have implementation challenges for 10GBASE-T**
- **Simple transmitter modifications will permit alternate 4-channel sampling approaches to be considered**
  - Modifications do not preclude traditional approaches
- **Phase insensitive sampling offers implementation advantages and opportunities for innovation for 10GBASE-T PHYs**
  - Disadvantages need to be independently quantified and weighed against advantages … goal for next meeting ?