



Update on the LDPC 4D-PAM8 Proposal for 10GBASE-T

IEEE 802.3an Task Force
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Agenda



- Summary of Refinements
- Environmental Variations of Cable Insertion Loss
- Reduced Symbol Rate
- Framing Refinement
- Transmit Filtering Refinement
- Updated LDPC Decoder Simulation Results
- Conclusions

Summary of Refinements



- ☰ These refinements to the LDPC 4D-PAM8 proposal described in rao_1_0704.pdf have been presented through the reflector to ensure timely discussion:
- Eliminate in-band adaptation of THP coefficients during normal operation.
 - Use bandwidth freed above to reduce symbol rate from 1Gs/s (1.0ns symbol period) to 952.381Ms/s (1.05ns symbol period).
 - Use 64B/65B encoding from powell_1_0704.pdf and tellado_1_0704.pdf to reduce control overhead
 - use (60,44,5) Reed-Solomon inner code to additionally protect header and back-channel bits in each block.
 - Use 1st order IIR transmit filter section instead of 1st order FIR transmit filter section to reduce EMI PSD peak by an additional 2.0dB.

Temperature Variations of Cable Insertion Loss



- ☰ Temperature coefficient of cable insertion loss (ISO/IEC-11801)
 - 0.4% per deg C from 20C to 40C for UTP
 - 0.6% per deg C from 40C to 60C for UTP
 - 0.2% per deg C from 20C to 60C for STP
 - Temperature variation of Insertion loss is <14% from 20C to 60C at 500MHz for 100m Cat-6 UTP*.
 - Temperature variation of Insertion loss is <6% from 20C to 60C at 500MHz for 100m Cat-6 STP*.

*ref: Alan Flatman, private communication

Eliminating in-band adaptation of THP Coefficients



- ☞ Temperature variation of cable insertion loss is less than 14m for a 100m Cat-6 cable.
- ☞ A single TH Precoder was shown to be reasonably effective over 100m variation of insertion loss in ungerboeck_1_0704.pdf.
 - Therefore, non-adaptive THP is clearly effective for dealing with 14m cable insertion loss variation due to temperature changes.
- ☞ In-band adaptation of THP Coefficients is not fast enough to deal with transient narrow band interferers.
 - Requires the use of an adaptive FFE at the receiver to notch out such interferers anyways.

Symbol Rate reduction



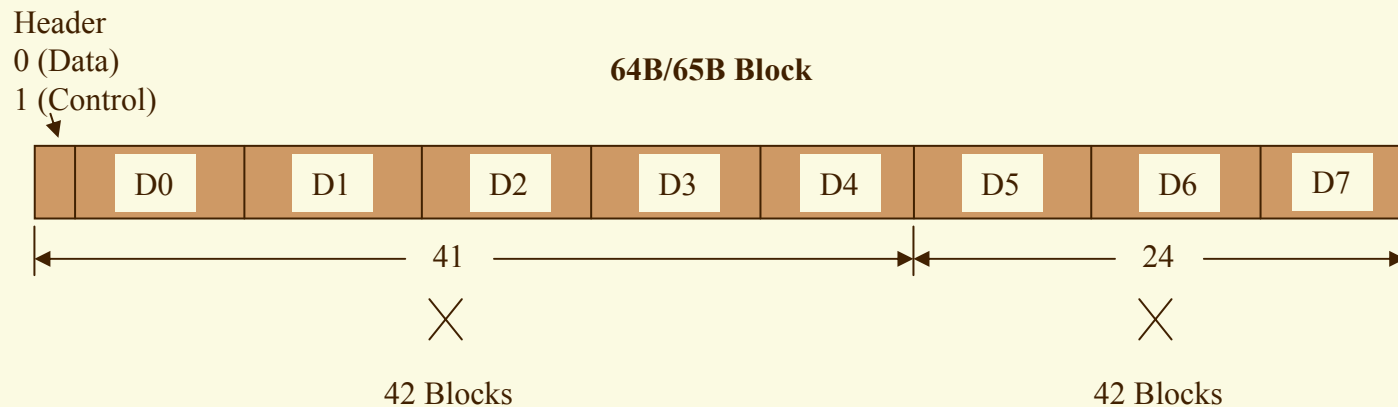
2747-bit Frame composition in rao_1_0704.pdf:

- 2560 Data bits over 256 symbols
- 80 64B/66B Header bits
- 10 pad bits
- 65 THP update bits
- 32 CRC bits
- Symbol rate = $10\text{Gb/s} * 256\text{symbols} / 2560 = 1\text{Gs/s}$
- Symbol period = $1 / 1\text{Gs/s} = 1.0\text{ns}$

Refined 2747-bit Frame composition:

- 2688 Data bits over 256 symbols
- 42 64B/65B Header bits
- 16 Parity Bits for an RS(60,44,5) Double Error Correcting Reed-Solomon inner code.
- 1 Back-channel information bit
- Symbol rate = $10\text{Gb/s} * 256\text{symbols} / 2688 = 952.381\text{Ms/s}$
- Symbol period = $1 / 952.381\text{Ms/s} = 1.05\text{ns}$

Proposed Framing

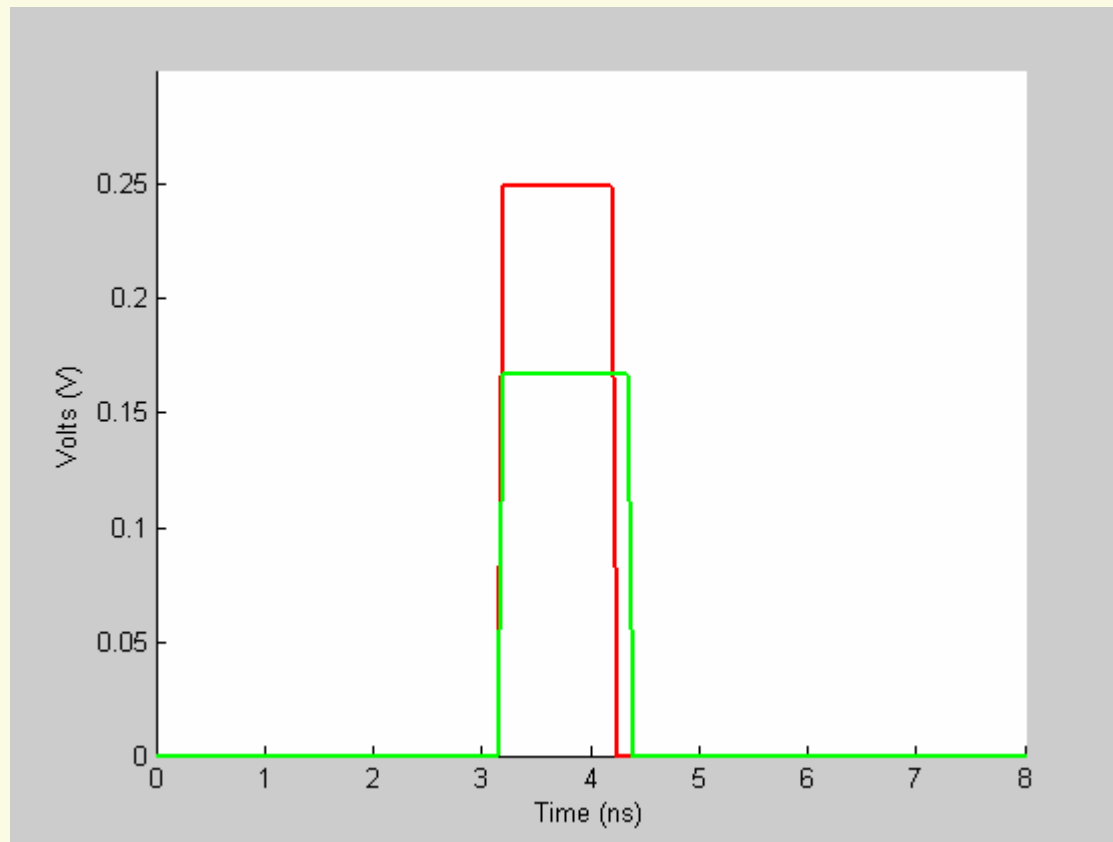


+1 Back Channel Bit = 1723
Information bits for (2048,1723)
RS-LDPC Code

+16 Parity bits for RS(60,44,5)
Code = 1024 Uncoded
Information bits for 1024 PAM8
symbols

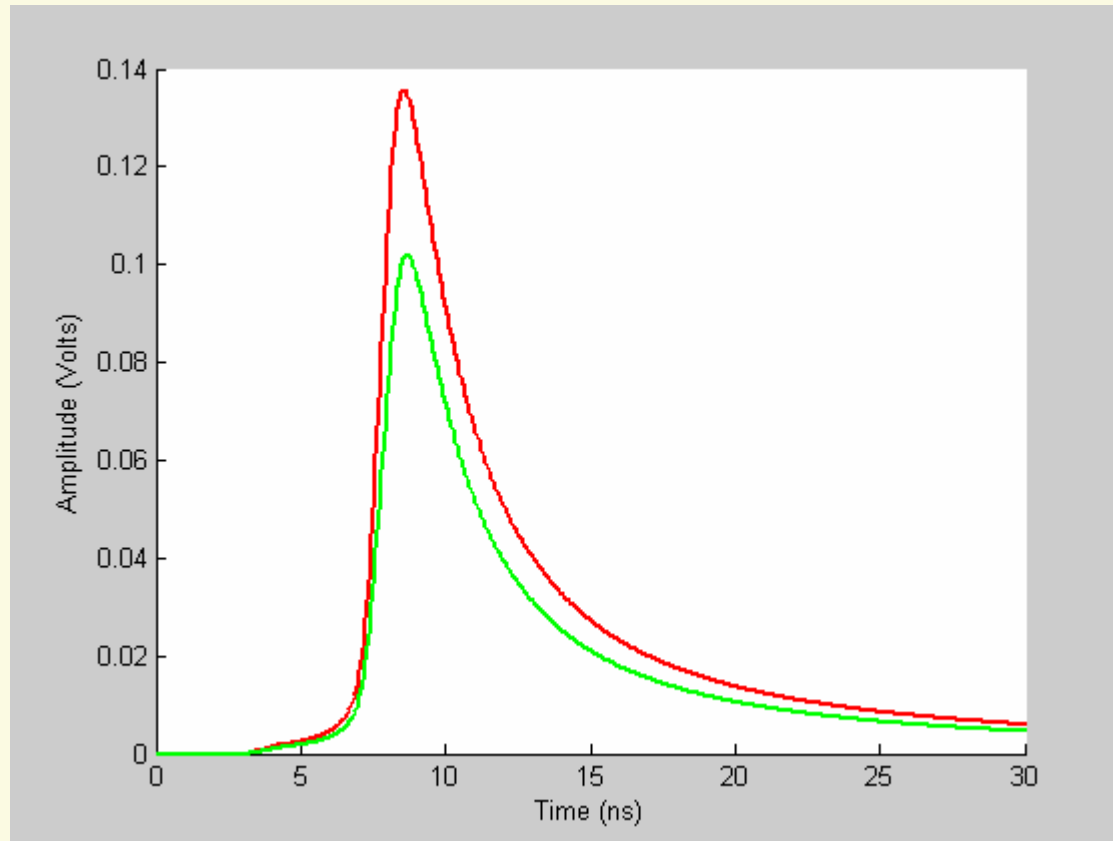
Unit Pulse Analysis

At input, after TH-Precoding – Difference in Amplitude is **3.5dB**



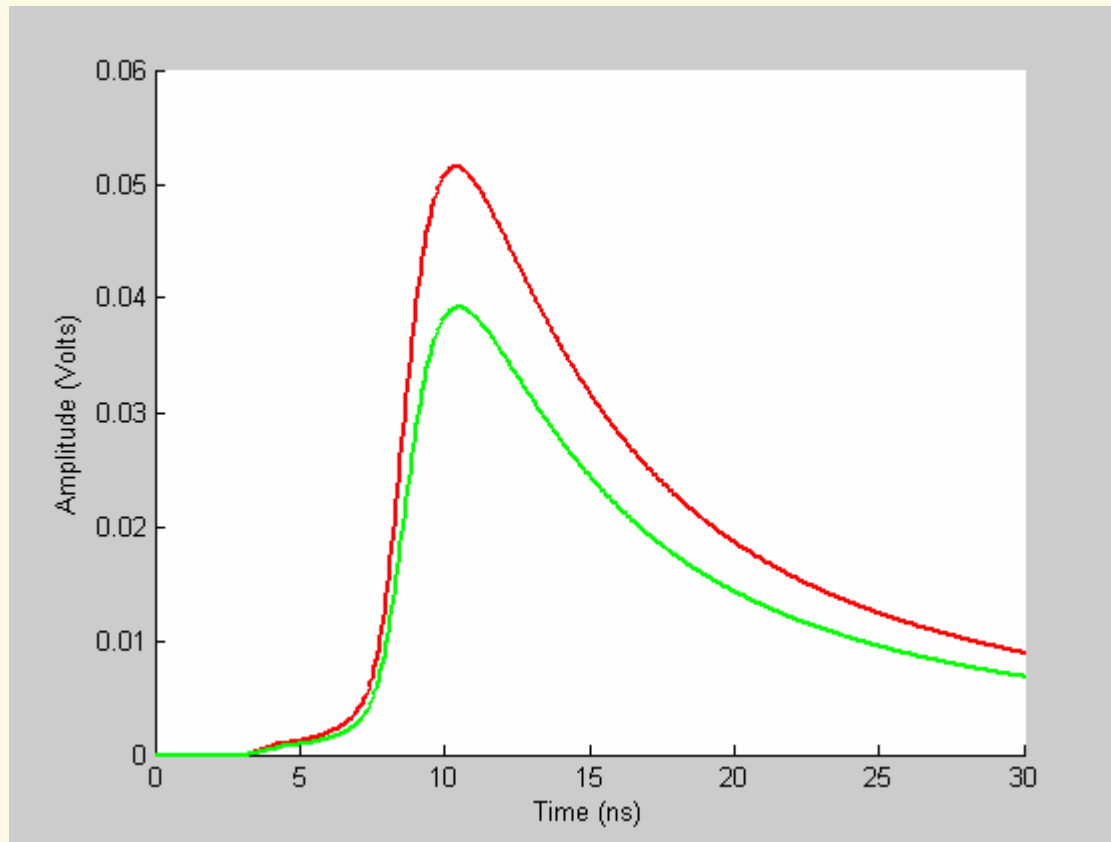
Unit Pulse Analysis

After 55m Cat-6 – Difference in Amplitude is **2.6dB**



Unit Pulse Analysis

After 100m Cat6 – Difference in Amplitude is **2.4dB**



Performance Comparisons



Model 1: 100m Cat7 4Conn IL, 62.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters

Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	AWGN for 1E-12 BER	Total EMI Penalty
LDPC 4D-PAM8	952.4Ms/s	19.9dB	26.5dB	6.6dB	-133.8dBm/Hz	0dB
LDPC 4D-PAM12	825Ms/s	23.8dB	29.5dB	5.7dB	-135.6dBm/Hz	2.4dB

Model 2: 55m Cat6e 4Conn IL, 49.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters

Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	AWGN for 1E-12 BER	Total EMI Penalty
LDPC 4D-PAM8	952.4Ms/s	19.9dB	26.8dB	6.9dB	-121.7dBm	0dB
LDPC 4D-PAM12	825Ms/s	23.8dB	29.1dB	5.3dB	-124.5dBm/Hz	3.4dB

Performance Comparisons (Contd.)



Model 3: 100m Cat6e 4Conn IL, 64.5dB ANEXT at 100MHz, split slope, Default Cancellation Parameters

Proposal	Symbol Rate	SNR for 1E-12 BER	SNR at -150dBm WGN	Margin at -150dBm WGN	AWGN for 1E-12 BER	Total EMI Penalty
LDPC 4D-PAM8	952.4Ms/s	19.9dB	26.1dB	6.2dB	-135.6dBm/Hz	0dB
LDPC 4D-PAM12	825Ms/s	23.8dB	29.2dB	5.4dB	-137.3dBm/Hz	2.3dB

Note: With AWGN analysis using Salz DFE SNR margins, assuming NO transmit filtering except for the transformer poles at 500MHz, the Total EMI penalty for PAM12 reasonably matches that derived from simple Unit Pulse Analysis

Refinement of Transmit Filtering

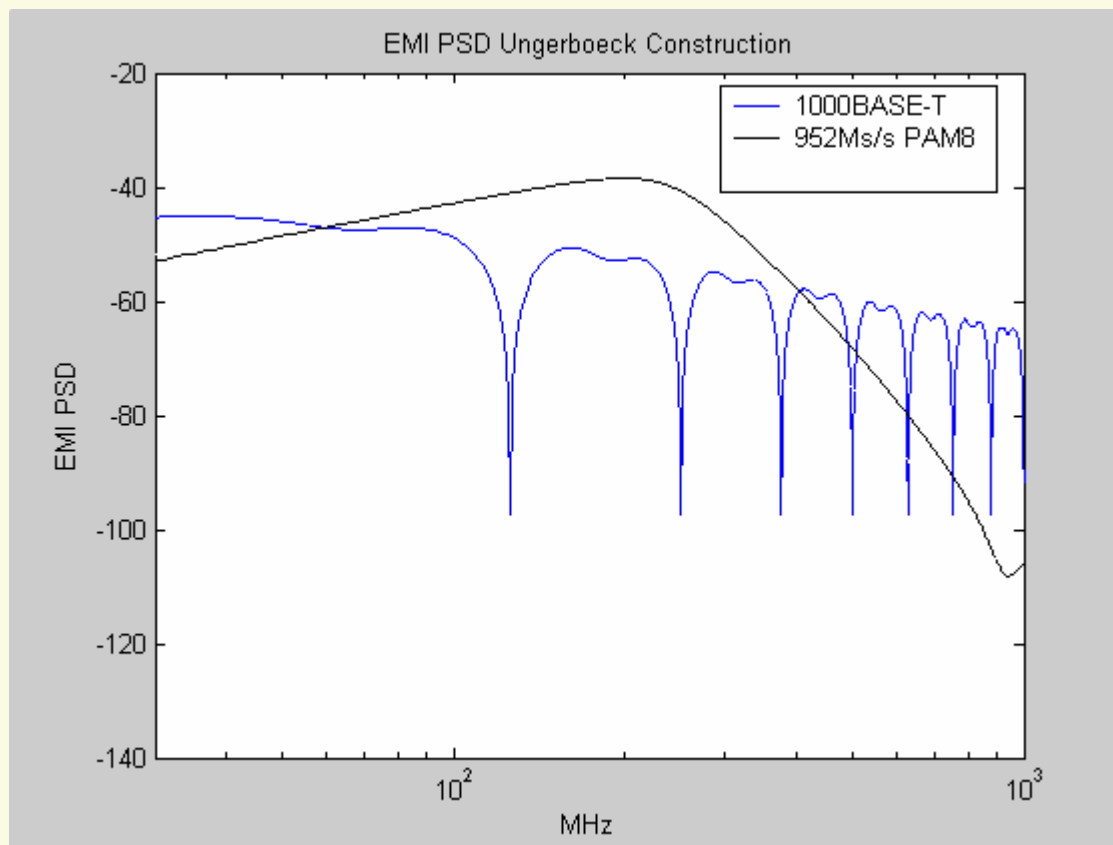
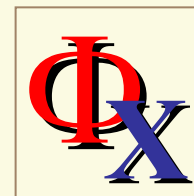


- ☞ Studied 3 different transmit filtering methods for SNR margin loss vs. EMI PSD peak relative to 1000BASE-T
 - EMI PSD peak computed using 20dB/decade slope applied to transmit PSD for $f > 30\text{MHz}$
 - SNR Margin loss computed by modifying transmit PSD with transformer loss and transmit filter response in solarsep_varlen7a code

- ☞ Transmit filtering methods:
 - (0.75+0.25D) First order FIR filter as in rao_1_0704.pdf
 - 5th order Butterworth filter with 3dB point at $f_s/4$ (238MHz) as in powell_1_0704.pdf
 - First order IIR filter with 3dB point at $f_s/5 = 190\text{MHz}$.

Filter Type	Order	3dB point	SNR Loss	EMI PSD peak vs 1G	Peak Frequency
(0.75+0.25D) FIR	1		1.2dB	+6.3dB	257MHz
Butterworth IIR	5	238MHz	2.4dB	+6.6dB	201MHz
IIR	1	190MHz	0.5dB	+4.2dB	237MHz

EMI PSD with BW5

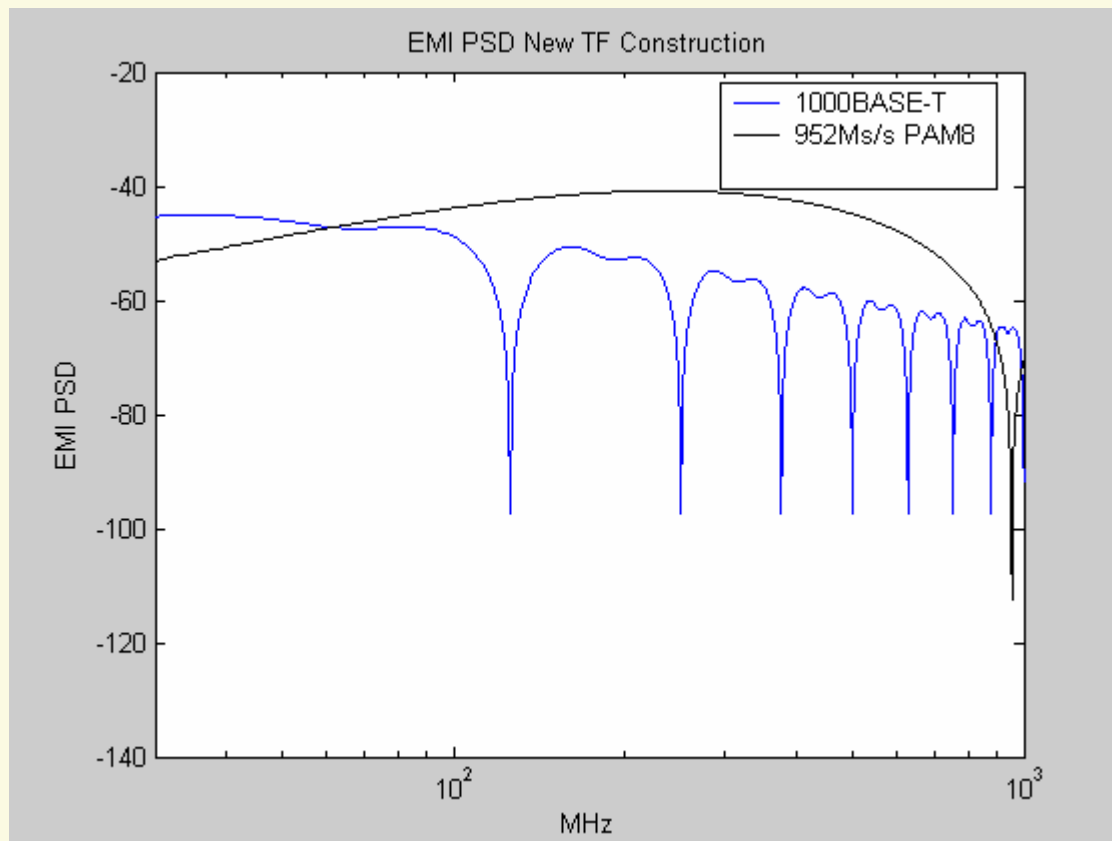
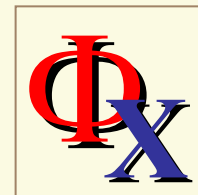


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EMI PSD with IIR-1



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Updated (2048,1723) RS-LDPC Simulations



☰ Gallagher Sum-Product Algorithm with

- 12-bit fixed point arithmetic,
- 4096-word lookup tables
- Max 30 iterations, with Frame Errors monitored as a function of number of iterations
- For each block that was found in error, a floating point simulation was initiated to check if the error was repeated

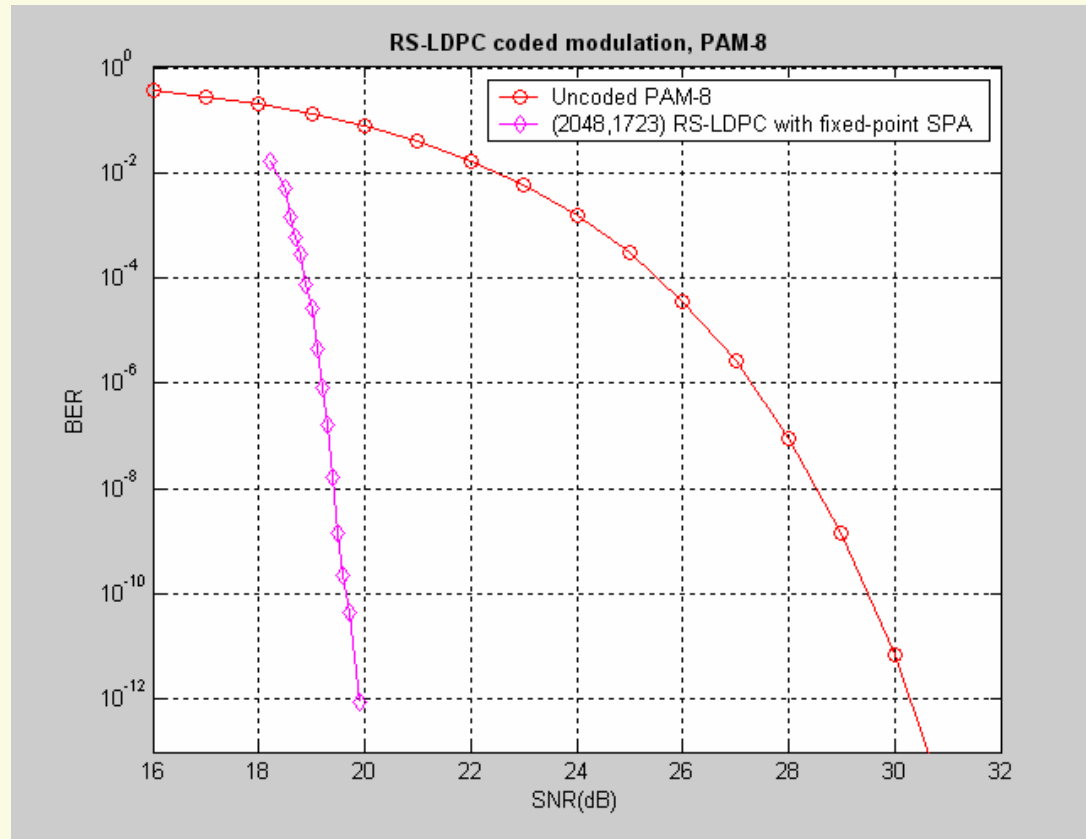
☰ General Observations:

- Max. number of iterations needed for convergence decreased as the SNR was increased
 - No more than 12 iterations were used at an SNR of 19.9dB
- The difference in performance between floating point and fixed point was less than 0.1dB.

☰ At an SNR of 19.9dB,

- there were 2 block errors with fixed-point arithmetic totaling 18 bit errors in 7,302,369,000 blocks for an estimated BER mean of $8.9E-13$
- There were 0 block and bit errors with floating point arithmetic in 7,302,369,000 blocks

Updated Simulation Results



Conclusions



- ☞ Proposed eliminating in-band adaptation of TH-P coefficients to reduce complexity of the 10GBASE-T standard
- ☞ Reduced symbol rate from 1Gs/s to 952.381Ms/s
 - Results in 1dB more SNR margin over all worst-case Models
- ☞ Refined Framing to use 64B/65B encoding and 2-error correcting RS inner code to protect header and back channel information bit
- ☞ Improved transmit filtering scheme to result in 2dB lower EMI PSD and 0.7dB lower SNR margin loss due to the transmit filter
 - Simple first order IIR filter can be implemented either in digital or in analog
- ☞ Presented simulation results of the (2048,1723) RS-LDPC code for better than 1E-12 BER using fixed point arithmetic.