

Performance evaluation of low latency LDPC code

Sept 2004

Katsutoshi Seki, NEC Electronics*

Toshihiko Shimizu, Tokyo Electric Power Company

Tetsuya Higuchi, Yuji Kasai, Eiichi Takahashi, AIST

*presenter

Supporters:

Outline

- Motivation
- 1K RS-based LDPC code family
- Simulation conditions
- Simulation results
- BER slope change estimation of LDPC(1024,833)
- Worst case BER curve of LDPC(1024,833)
- Summary

Motivation

- System vendors pointed out that low latency increases the market potential. *1
- 1K RS-based LDPC code family has low intrinsic latency of 160nsec.
 - $\gamma = 8$ LDPC(845,1024) *2
 - $\gamma = 10$ LDPC(833,1024) *2
 - $\gamma = 32$ LDPC(781,1024) *3
- LDPC(845,1024) has BER slope change at $1E-9$ BER. *2
Increasing bit node degree(γ) pushes down BER slope change point.

Purpose :

Find LDPC code which has BER slope change below $1E-12$ BER.
Estimate BER curve below slope change point.

*1 www.ieee802.org/3/an/public/mar04/muller_1_0304.pdf

*2 www.ieee802.org/3/an/public/july04/seki_1_0704.pdf

*3 www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf

1K RS-based LDPC codes

Code	(821, 1024)	(833,1024)	(845,1024)
Coding rate	0.802	0.813	0.825
Intrinsic Latency @800MHz baud	160nsec	160nsec	160nsec
Check node degree	32	32	32
Bit node degree	12	10	8
Lower bound Hamming distance	14	12	10
The # of Edges of message path	12280	10240	8192

Simulation conditions

Mapping: PAM12-doughnut (*1) and PAM12T (*2)

Decoder design :

1) Floating point design

10 iterations

2) Fixed point design

1D-PAM12 decoder(PAM12T decoder)

6 bit operations,

5 bit address for Gallager function LUTs

7 iterations

Decoding algorithm: SPA

SNR definition

Var : Variance of additive noise

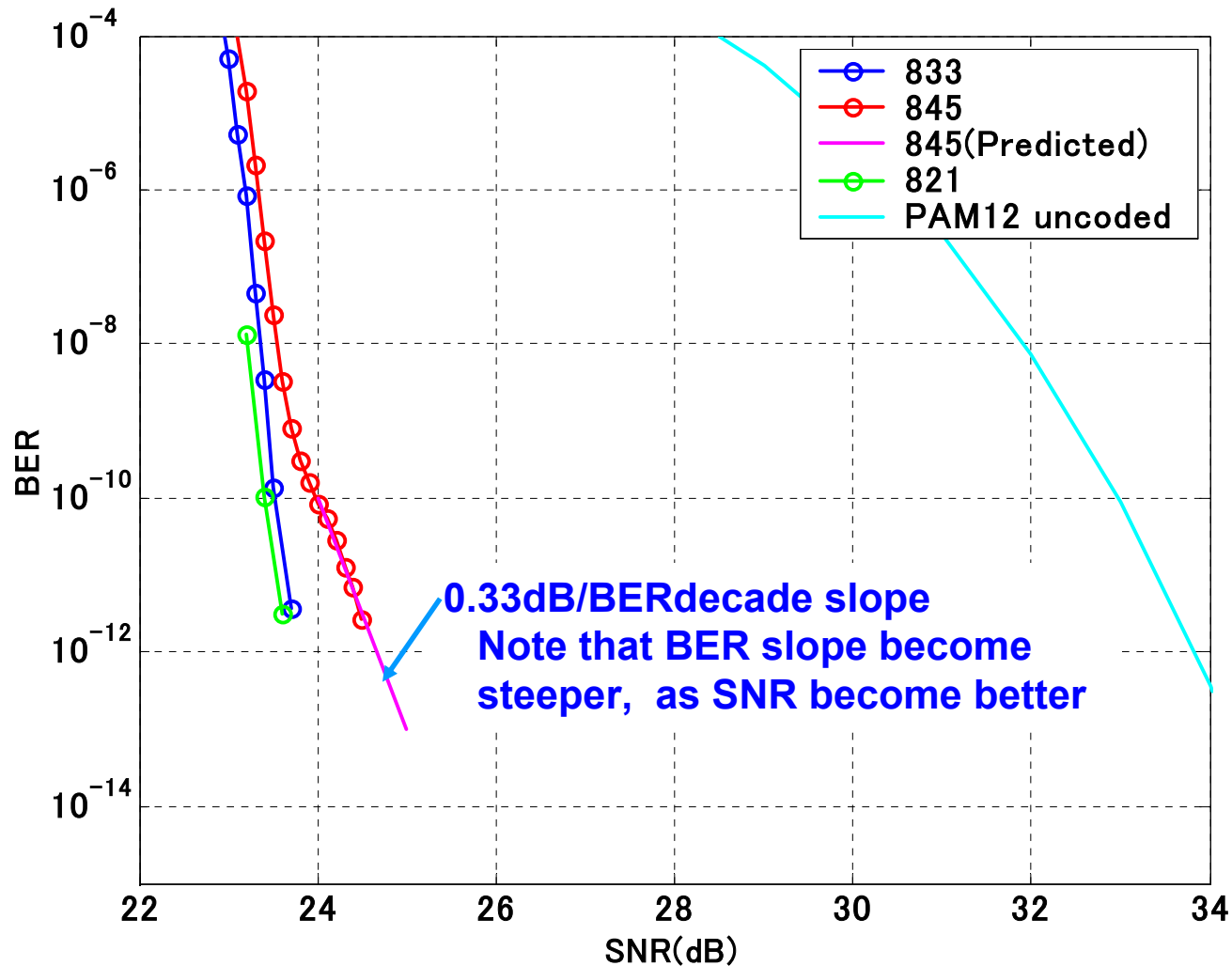
Min. distance between constellations : 2

Var = $\text{pow}(10.0, (-\text{SNR}/10.0)) * 47.67$;

*1 www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf

*2 www.ieee802.org/3/an/public/sep04/tellado_1_0904.pdf

Simulation results

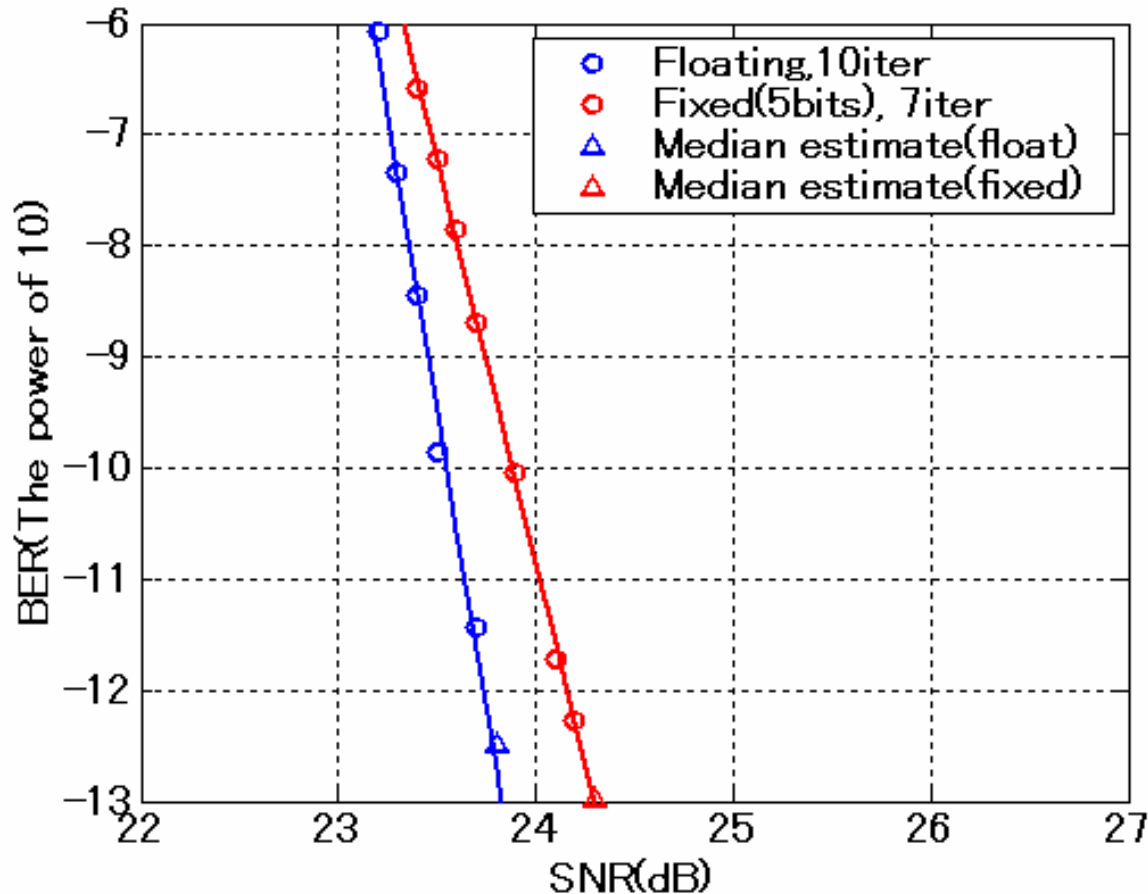


LDPC(833) is recommended 1K code

Code	(821, 1024)	(833,1024)	(845,1024)
Coding rate	0.802	0.813	0.825
Intrinsic Latency @800MHz baud	160nsec	160nsec	160nsec
Check node degree	32	32	32
Bit node degree	12	10	8
Hamming Distance	≥ 14	≥ 12	≥ 10
The # of Edges of message path	12280	10240	8192
Relative complexity	1.2 or more	1	0.8 or less
Required SNR for 1E-12 BER (PAM12 mapping)	23.7dB	23.8dB	24.8dB

- 821 code have 20% larger number of edges than 833 code.
This give us routing and congestion problems on the message network,
witch requires increase in logic size and power consumption by more than 20%.
- 833 code is optimal code in terms of performance complexity tradeoff

BER slope change estimation of 833 code



1) Floating point design
No error seen in 4.0E13 bits
at SNR=23.8dB

2) Fixed point design
No error seen in 1.4E14 bits
at SNR=24.3dB

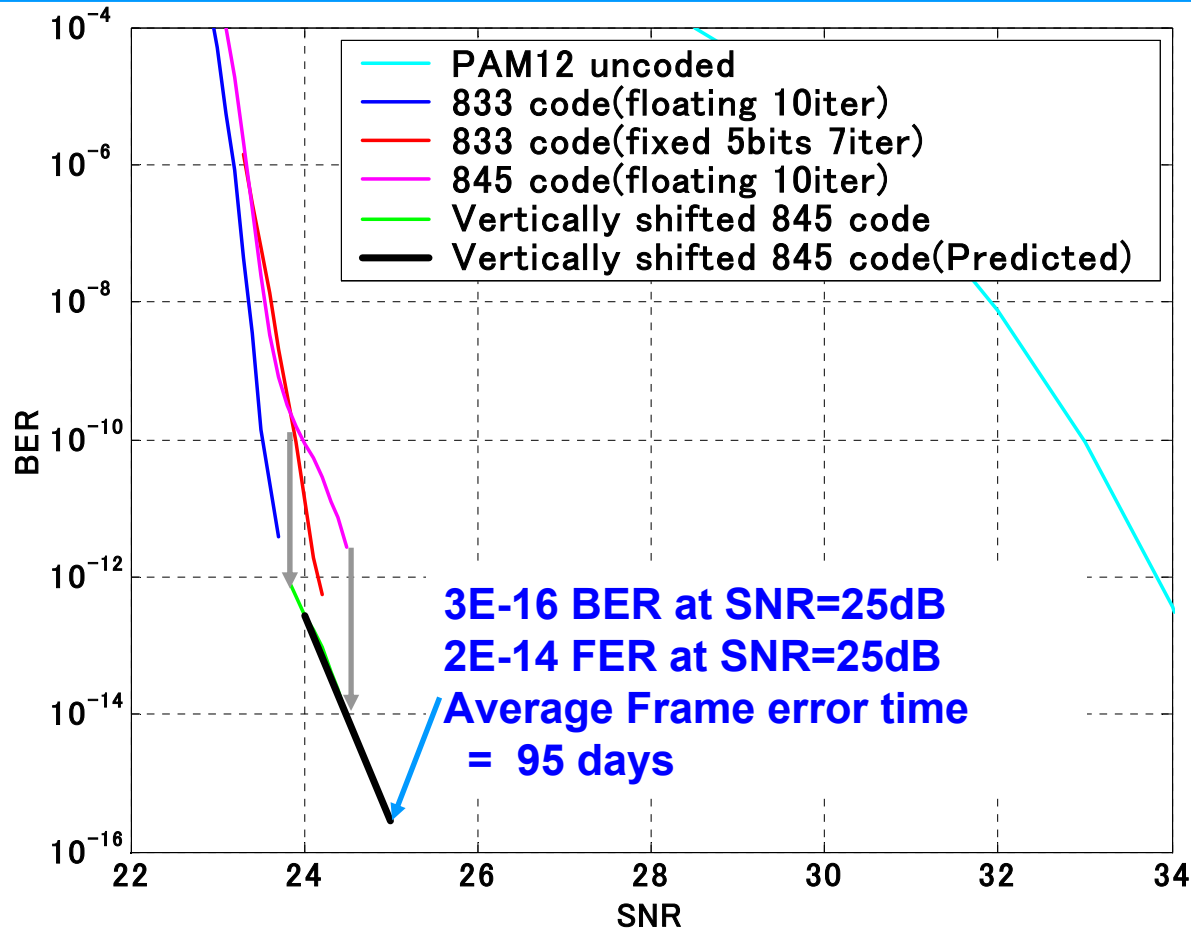
Average number of error bits
per error blocks =25

$$FER = BER / 25 * 1792$$

Confidence interval points	float	fixed
95%	1.77e-12	4.79e-13
80%	9.37e-13	2.60e-13

This results shows BER slope change does NOT occur above 1E-12 BER.

Worst case BER curve of 833 code



-Even if BER slope change happens at $1E-12$ BER, BER curve is below vertically shifted BER curve of 845 code.

Summary

We have evaluated 1K RS-based LDPC code family

LDPC(845,1024) : Poor performance

**LDPC(821,1024) : Only 0.1dB gain to 833 code
with 20% or more higher complexity**

LDPC(833,1024) :

- **Excellent error correction performance**

 - Required SNR=23.8dB for 1E-12 BER**

- **No BER slope change down to 1E-12 BER**

- **Even if BER slope change happens at 1E-12 BER,
BER curve is still acceptable**

LDPC(833,1024) is optimal code in terms of performance complexity tradeoff