



#### IEEE 802.3ap Channel Ad Hoc Status Update - SDD21 & SDD11/22 Model Development

Rich Mellitz, Intel Matt Hendrick, Intel John DAmbrosia, Tyco Electronics







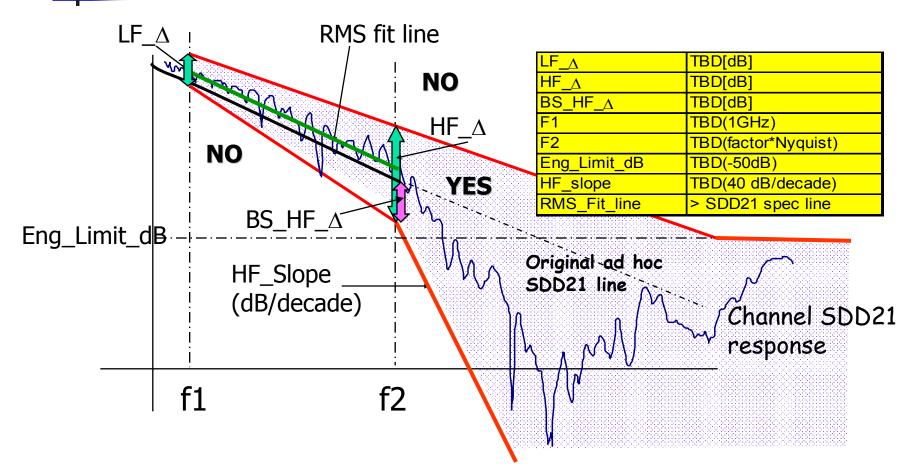
#### Acknowedgements

- Steve Krooswyk
- Mike Altmann



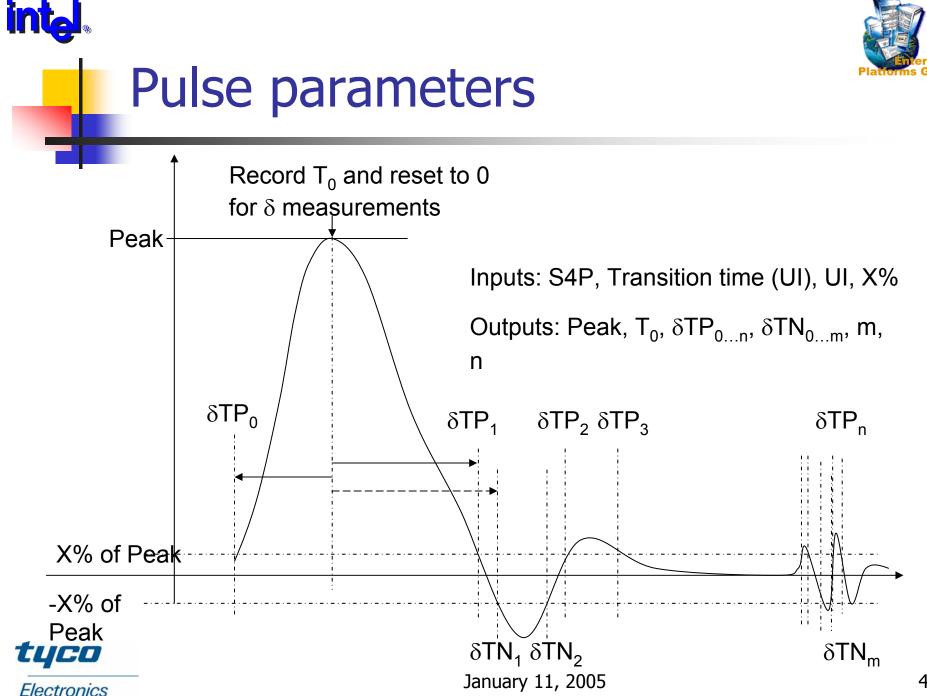
#### Frequency Domain: Modified SDD21







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#### **Course of Action**

Analyze all sorts of channels based on proposed SDD21 model and subsequent pulse response parameters

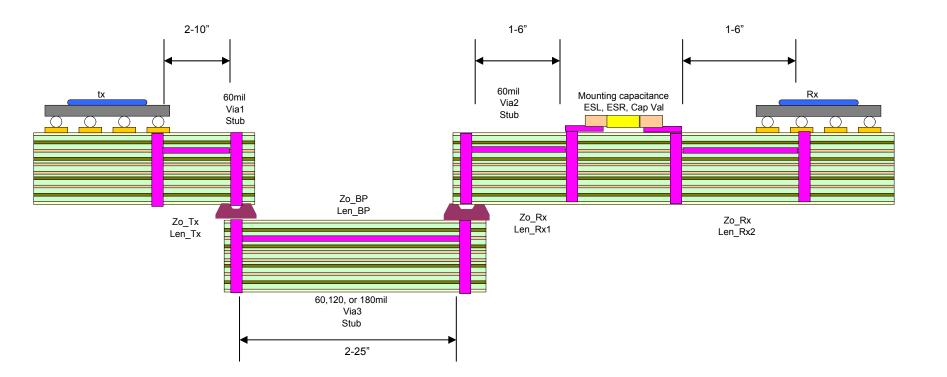
- Description of analysis
  - F1 = 1 GHz
  - F2 6 GHz
  - 10Gb/s Pulse
  - Settling time based on 5% of peak
  - Min, max values calculated over entire range, specified values at F1 / F2 to be determined
- Description of channels
  - Intel 192 different simulations
    - Backplanes Summary Description
      - Lengths
      - Layer connection varied by stub length
      - Generic FR-4
    - Line Cards
      - To TP4 Length 1" 6"
      - TP4 TP5 Length (no cap, but vias and stubs included) 1' -6"
      - Packaging Effects (different 10 dB packages)
      - Layer Connections varied by stub lengths
      - Generic FR-4
    - Board materials
  - Tyco 60 different channel measurments
    - Backplanes QR Designs (0.125" nominal thickness)
      - -13SI, -13, 9000
      - 1" to 30"
      - Top (No Counterboring) and bottom layer connections
    - Line Cards (0.092" nominal thickness)
      - -13, -13SI, -6
      - 6" and 10"
      - No AC Coupling
      - No Packaging effects
      - Top (No Counterboring) and bottom layer connections
- Through correlation analysis between frequency and time data, identify trend behavior of different parameters that impact settling time
- Look at interaction of packaging with placement of decoupling cap and impact on settling time







## Intel Simulation Topology



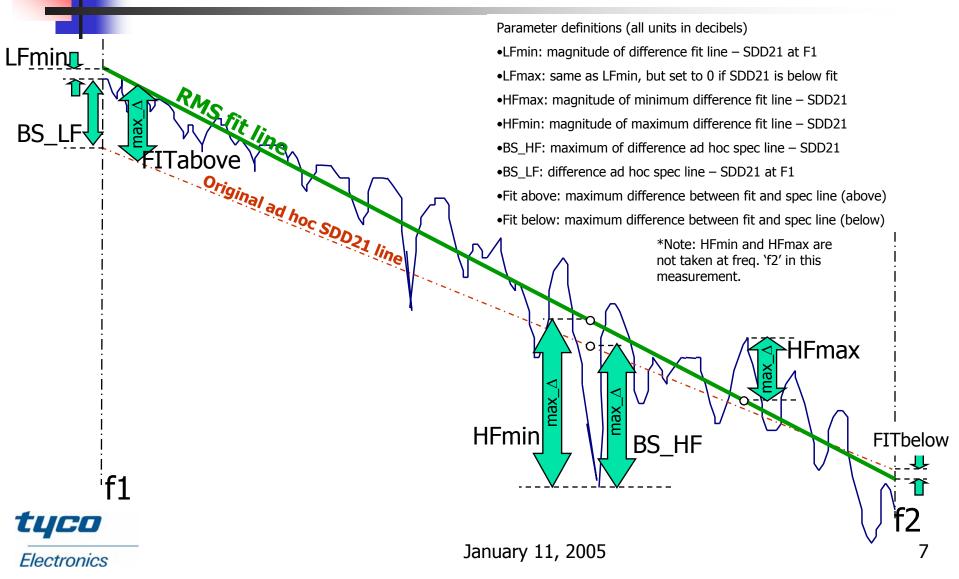
\*Note: capacitor currently shorted. Awaiting accurate HF/LF capacitance models





#### Frequency Domain Calculated Parameters SDD21

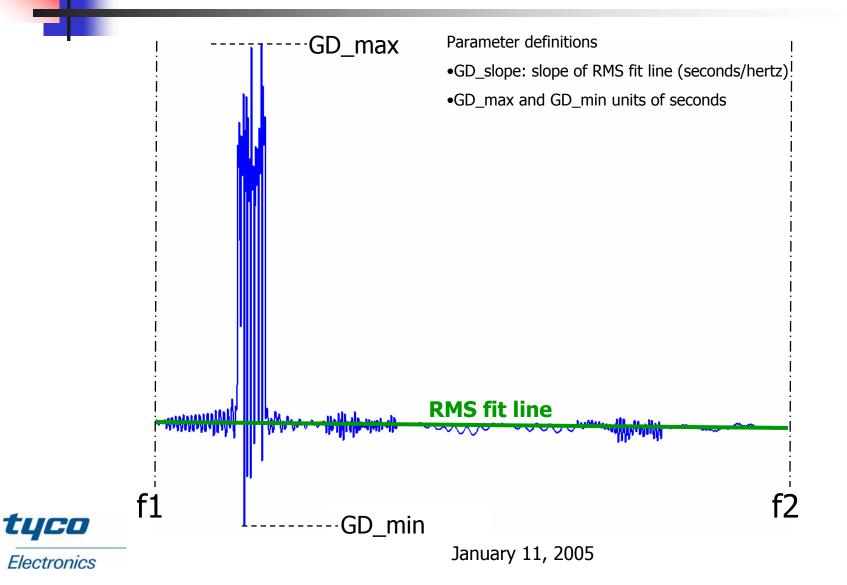
intel.

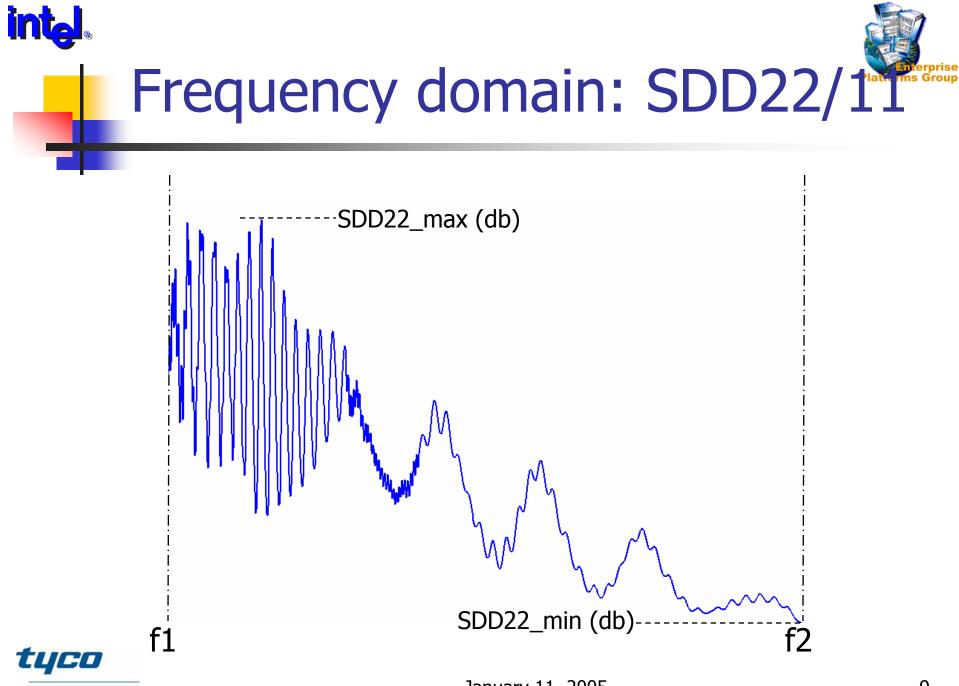






#### Frequency domain: Group Delay





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# Summary

Legend	
Strong	
Medium	
None	
Not Available	



Parameter		Correlation
LFmax	Intel	
	Тусо	
LFmin	Intel	
	Тусо	
HFmax	Intel	
	Тусо	
HEmin	Intel	
	Тусо	
BS_LF	Intel	
	Тусо	
BS HF	Intel	
	Тусо	
FITabove	Intel	
	Тусо	
FITbelow	Intel	
	Тусо	
GD_min	Intel	
	Тусо	

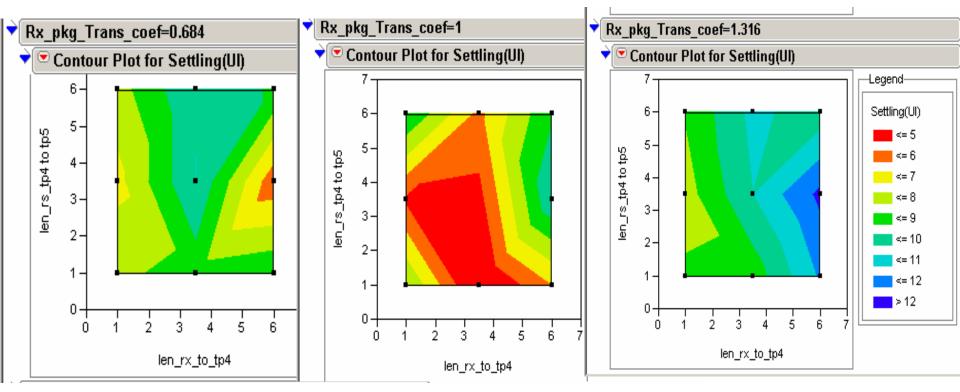
Parameter		Correlation
GD_max	Intel	
	Тусо	
GDslope	Intel	
	Тусо	
SDD11max	Intel	
	Тусо	
SDD22max	Intel	
	Тусо	
SDD11min	Intel	
	Тусо	
SDD22min	Intel	
	Тусо	
peak	Intel	
	Тусо	
n(TP)	Intel	
	Тусо	
m(TN)	Intel	
	Тусо	
TP(-1)	Intel	
	Тусо	
TP(1)	Intel	
	Тусо	
Total Length	Intel	
	Тусо	







### Effect due to 10dB packages



- 10 dB packages have a large impact.
- Reference http://ieee802.org/3/ap/public/channel\_model/mellitz\_m1\_0105.pdf

**tyco** Electronics





#### Conclusions

- Further investigation of simulation results and outliers from both sets of data necessary
- Parameters used in analysis based on proposed SDD21 model are strong indicators of settling time
- SDD11 / SDD22 of TP1 / TP4 lacked correlation to settling time
- Group Delay
  - Looked at in range of F1 / F2
  - Minimum value had greatest correlation to settling time
  - But correlation with actual channel data wasn't as strong as simulated.
- Critical
  - Rx line card and package design causes variability in settling time
  - Packaging design could increase the settling time







### Recommendations

- Adopt proposed TP1/TP4 Informative SDD21 model template
  - To be done specify LF and HF parameter at F2
  - Evaluate need of all parameters in model
  - Specific recommendations for each value needs to be completed upon Signal Ad Hoc analysis
- Eliminate proposed TP1/TP4 Informative SDD11 / 22 mask
  - Leave to normative analysis with inclusion of packaging effects
- Eliminate TP1/TP4 Informative Group Delay template







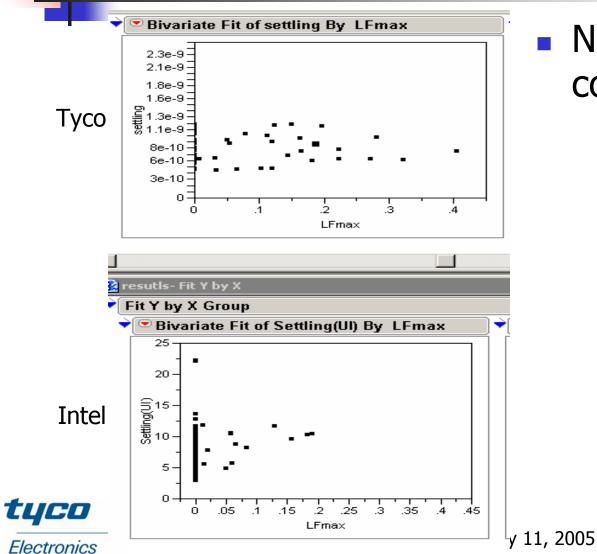
#### **Backup Slides**





#### LF max





#### No apparent correlation



#### LF min



Type Function Bivariate Fit of settling By LFmin 1.8e-9 1.8e-9 1.4e-9 1.2e-9 8e-10 6e-10 4e-10 0.2.6 1 1.41.82.22.6 3 3.43.84.24.6 5 5.45.8 LFmin

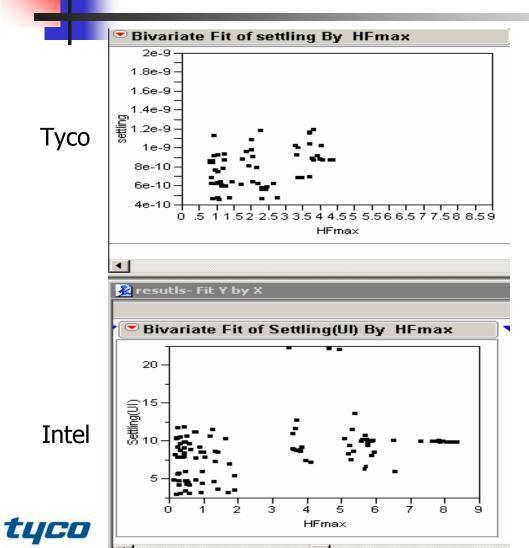
# Intel Intel

#### Simulations show another distribution





#### HF max

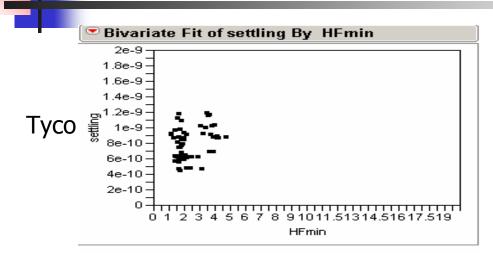


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#### HF min



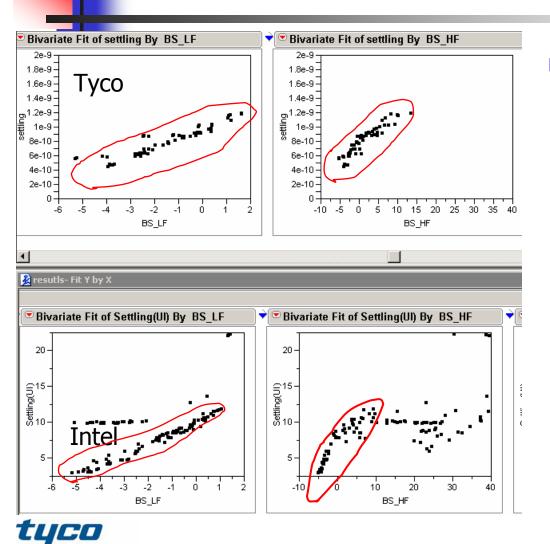


# Intel Fictorics

# No correlation2 sim distritutions



#### BS\_LF / BS\_HF



#### Correlation but Intel data has 2<sup>nd</sup> distribution

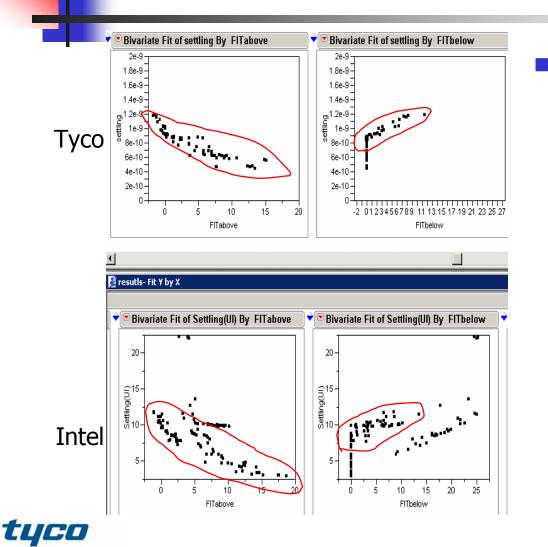








### Fit Above / Fit Below



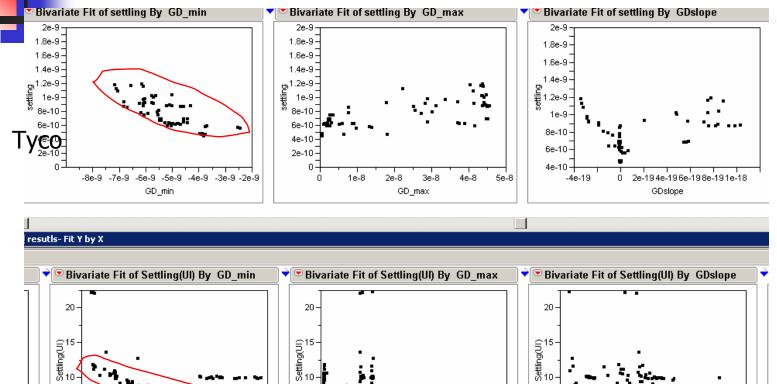
Strong influence but sim data has some outliners.

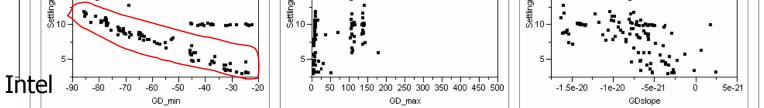
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#### **Group Delay**





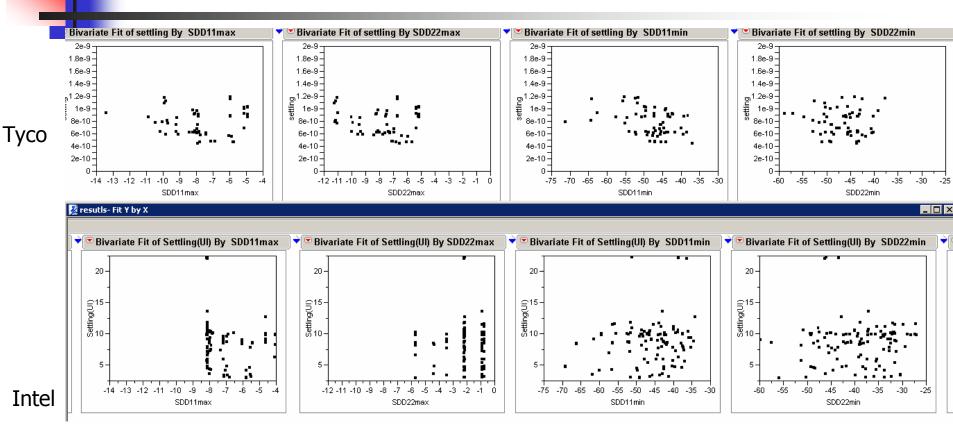


GD\_min ... correlation but simulations had second distribution
GD\_max and GD\_slope ... no correlation





#### SDD11 / SDD22



#### No correlation

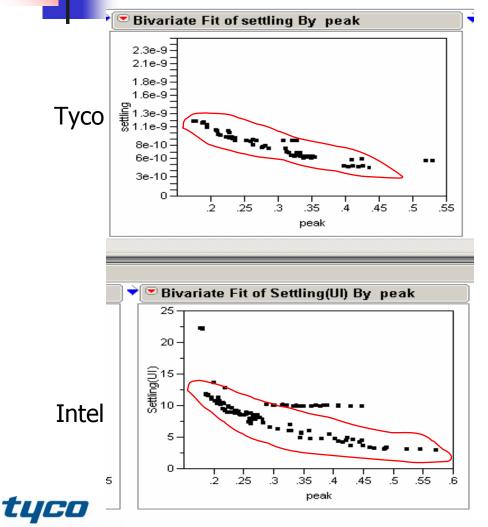




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#### Pulse Response Peak



- Good peak correlation
- Sim data as 2<sup>nd</sup> distribution and outlier
- Settling is % of peak. Should it be absolute?

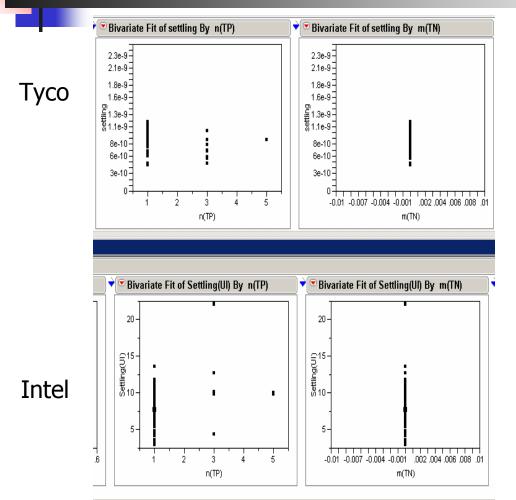
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### Number of Crossings



- No negative crossings
- Max of 5 positive crossings
- But not via > 200 mils stub and based on 5 %

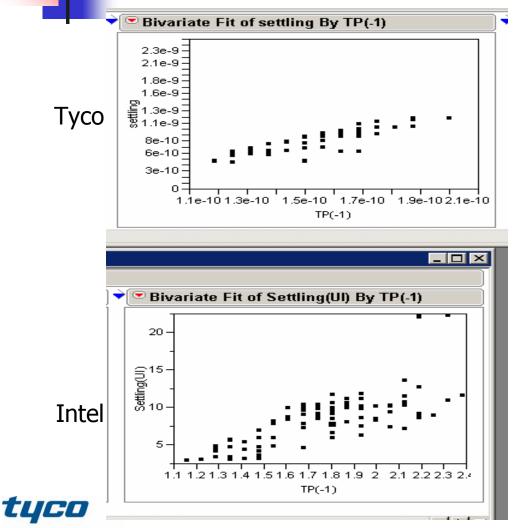




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# First Crossing (TP-1)



- Strong correlation
- Sim has wider distribution and an outlier.

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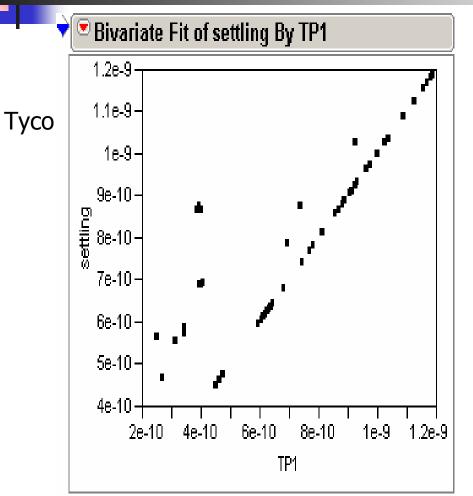


intal

TP1

January 11, 2005



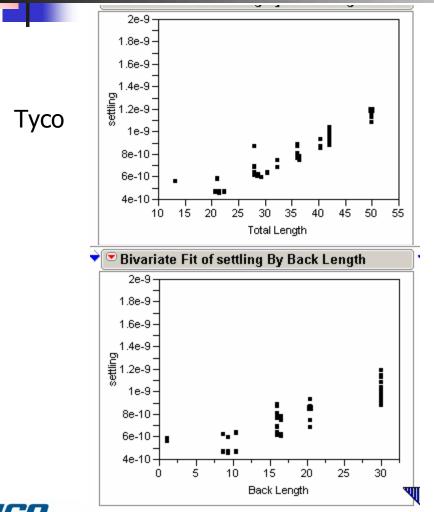


#### Good correlation but outliers









- Overall length has strong correlation
- LC length not strongly correlated

