IEEE802.3ap

Duty Cycle Distortion Penalty

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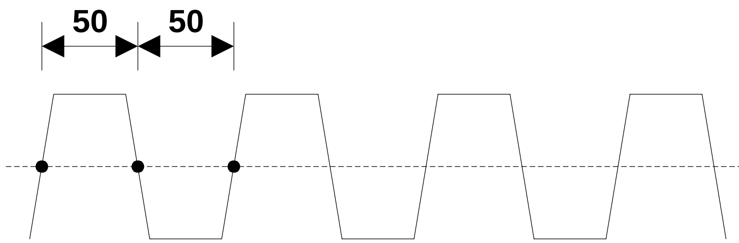
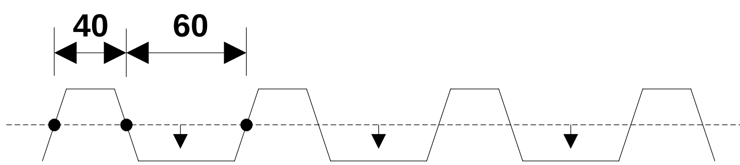
Overview

Duty Cycle is the ratio of the pulse duration to the pulse period. Ideally the duty cycle prior to the backplane is 50%.

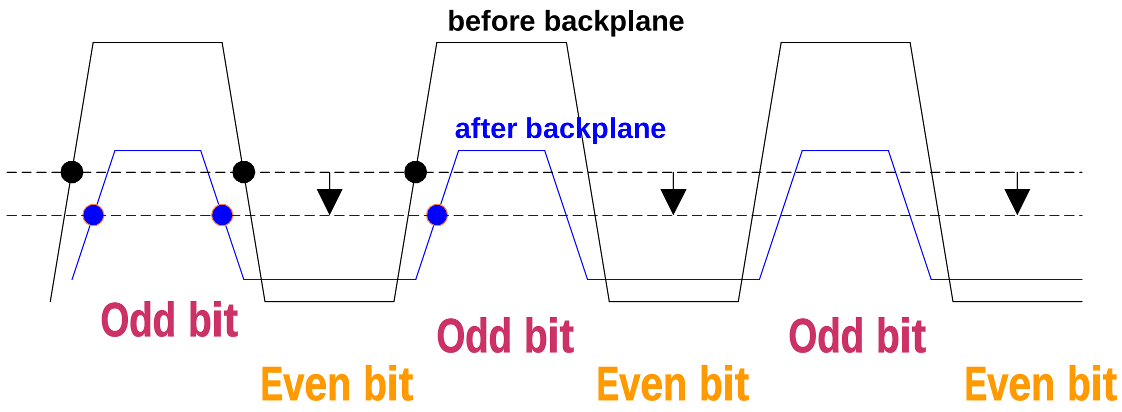


Duty Cycle Distortion (DCD) is both the variance in timing away from 50% duty cycle, and also the variance in average voltage offset.



DCD increases as the low pass filter effects of the backplane channel reduce amplitude and rise / fall times.

Average Voltage Offset

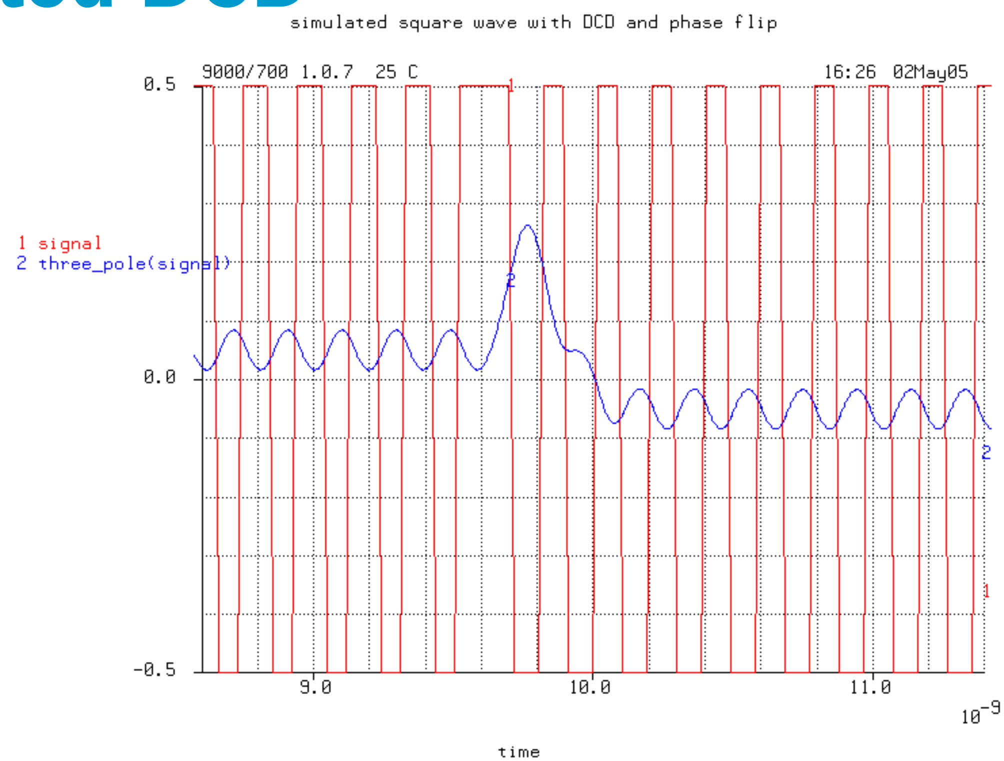


Let's call the wide bits even, and the narrow bits odd.

If, during some period of time, the majority of the even bits are low and the majority of the odd bits are high, the signal will have an overall average offset toward low, even though there are <u>equal number</u> of highs and lows.

The channel will attenuate the high frequency components but generally not the offset, which will be at a much lower frequency

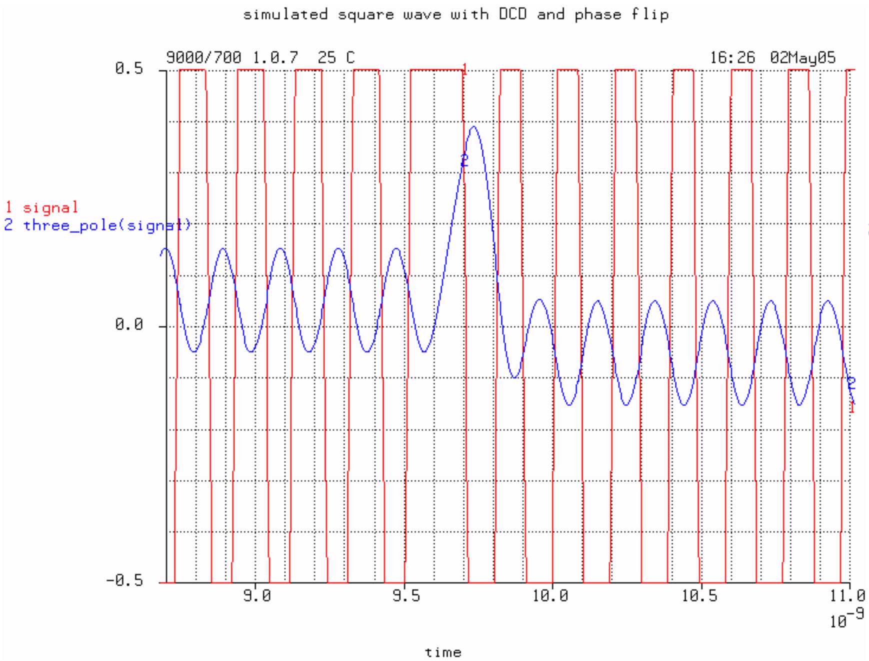
Simulated DCD

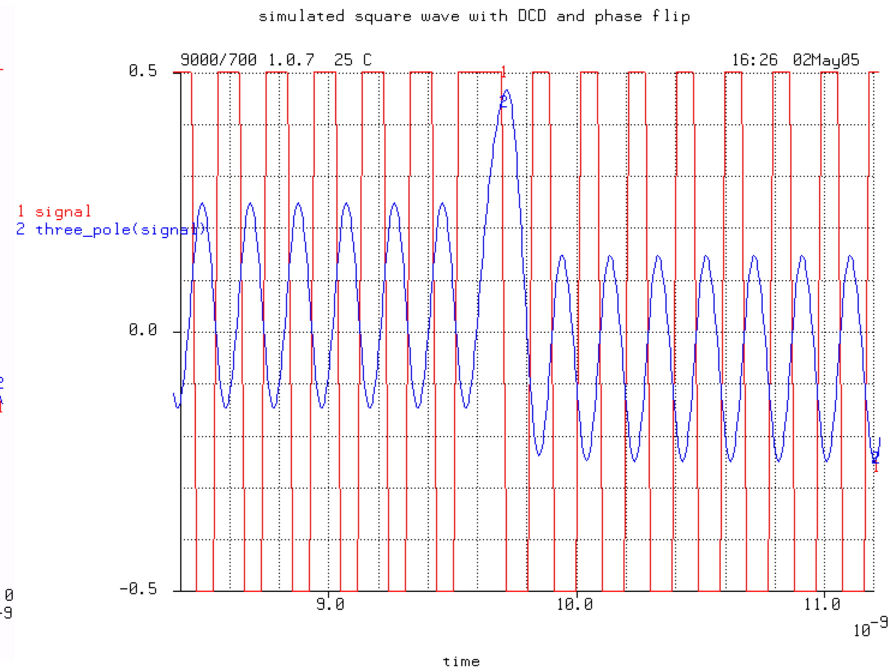


This is an alternating 1010 pattern with 5% DCD before (red) and after (blue) a 10GHz low pass filter with a change in phase so that the even bits are initially 1s, then 0s.

The blue trace shows the offset shift from 50mV above ideal to 50mV below ideal.

Simulated DCD

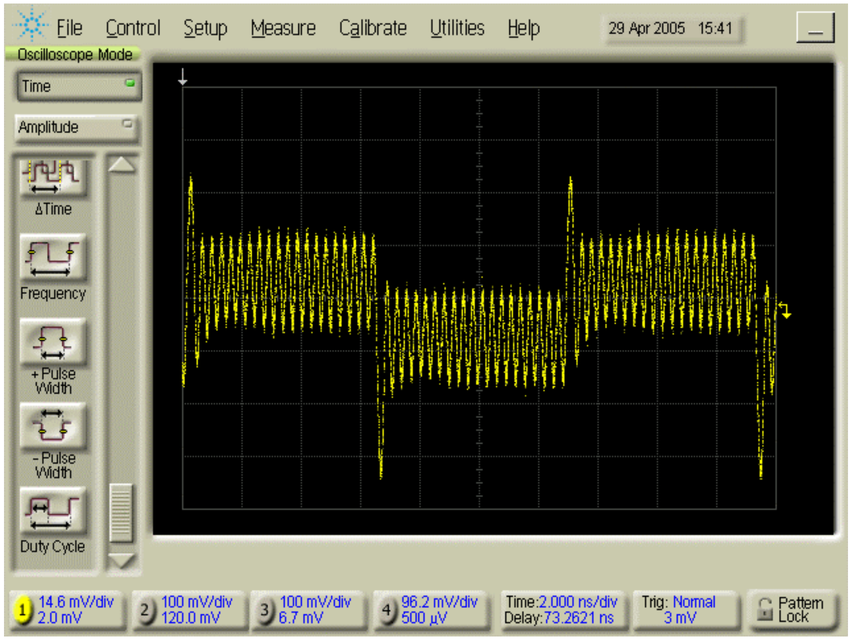




Same simulation with 15GHz and 20GHz low pass filters.

This shows that with better frequency capable backplanes, DCD would be less of an issue, and the offset difference between even and odd weighted duty cycles would allow more open eyes.

Measured DCD

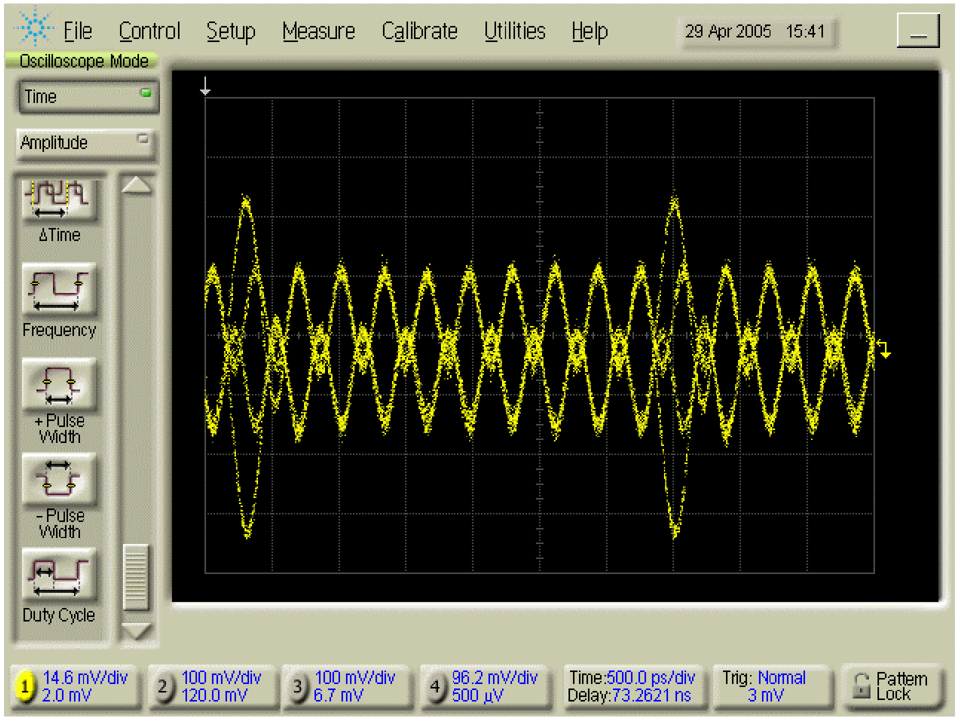


Here is the same thing but measured rather than simulated.

Conditions:

- **6.25Gbps**
- **Legacy backplane**
- **About 1% duty cycle distortion**

Measured EYE with DCD



Here is a zoomed in scope shot of the previous 1010 pattern through a legacy backplane at 6.25Gbps with 1% DCD while maintaining the constant phase

Note: offset doesn't change

How to describe the DCD effect

This EYE can be treated either:

- As an EYE partially closed vertically by changing baseline
- As an EYE partially closed horizontally by amplified jitter, producing even bits which are extra wide and odd bits which are extra narrow

Proposal

I propose that we use the baseline wander description because:

- **Baseline wander is linear with Duty Cycle error and jitter amplification is not.**
- **Baseline wander is easier to add into the link Budget.**