

# **EIT limit for port type KR**

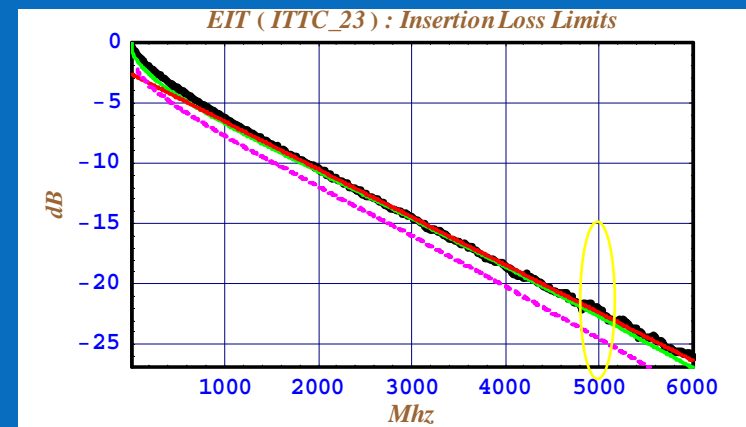
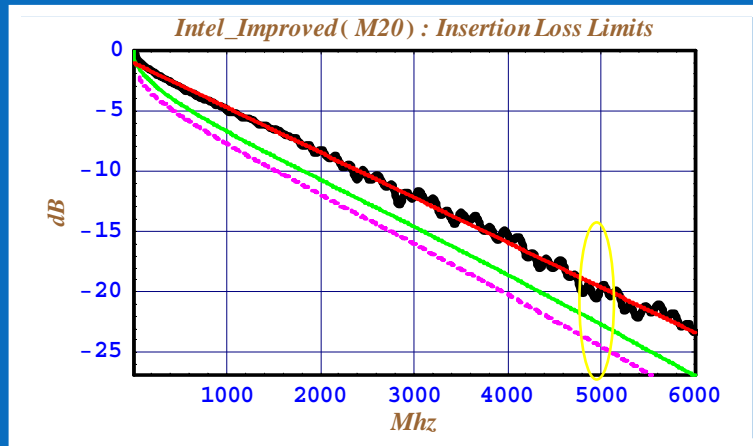
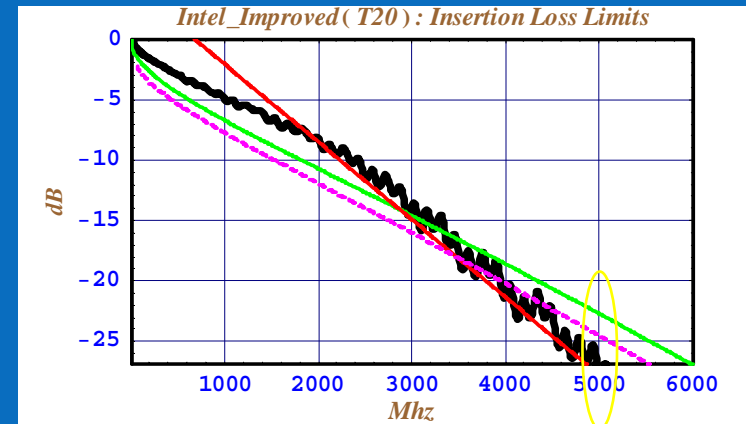
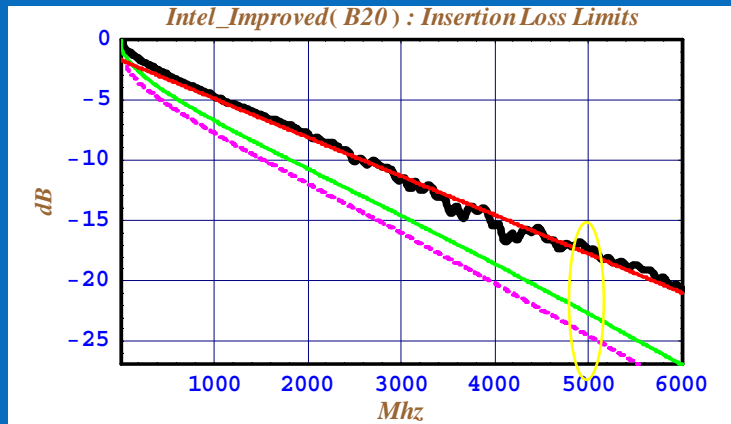
Fulvio Spagna

# Objectives

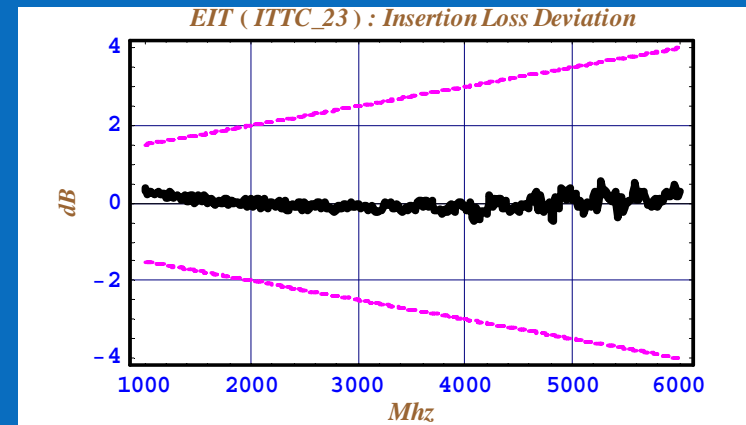
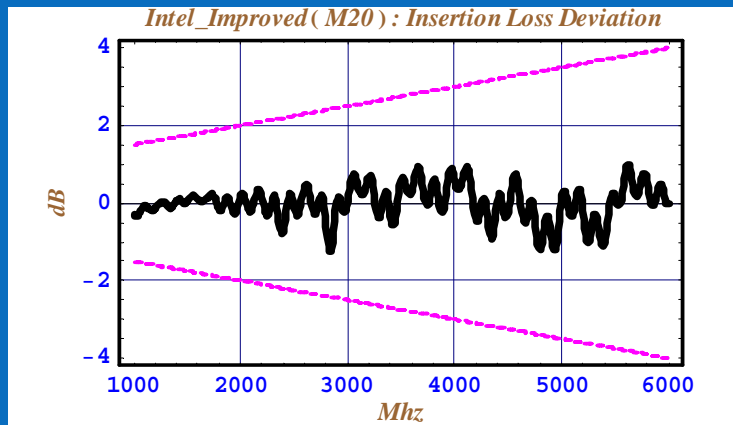
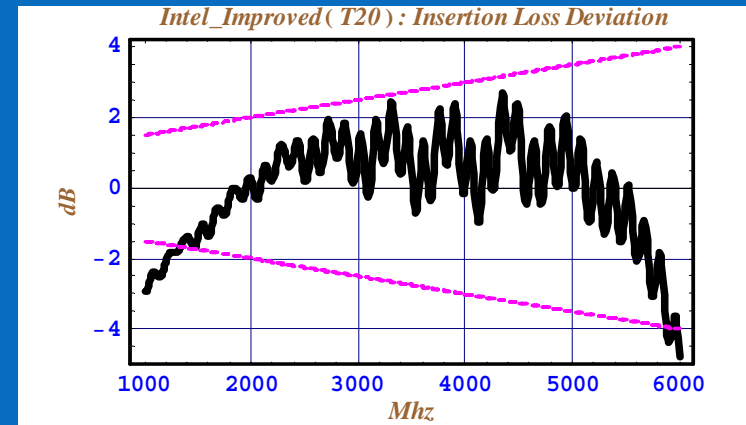
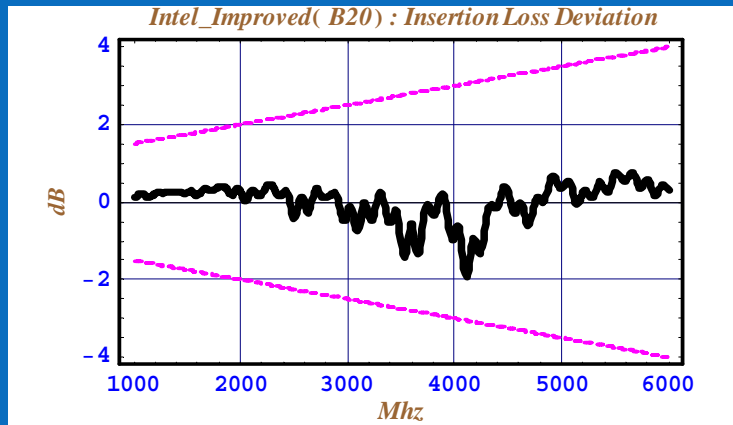
- Determine an appropriate level for the EIT test for the KR port type
  - this means finding an appropriate level for the sinusoidal interference which is representative of the levels of interference experienced in presence of crosstalk
  - because the EIT test methodology defined in Clause 69A is based on a high-loss channel (like the proposed ITTC23), it is important to determine the level of crosstalk experienced by a high loss channel
- Among the channels available in the database, there are several examples of high loss channels. In this presentation I will focus on the Intel channels (peters\_m1\_0605.zip) as they have been demonstrated to be more representative of a marginal channel.

*Note: in the following pages, all the channel parameters are referenced to the new  $A_{max}(f)$  defined in goergen\_01\_0206*

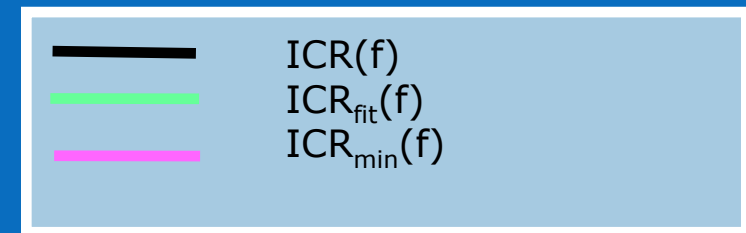
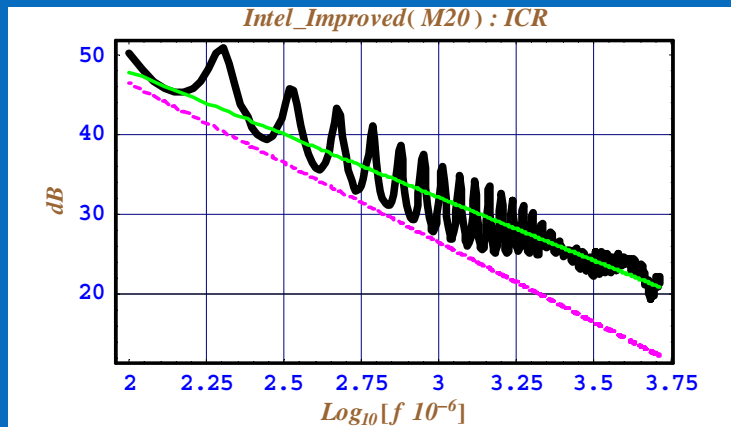
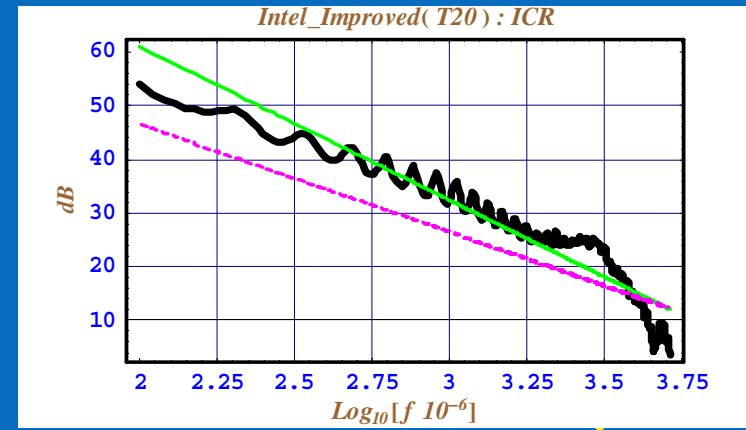
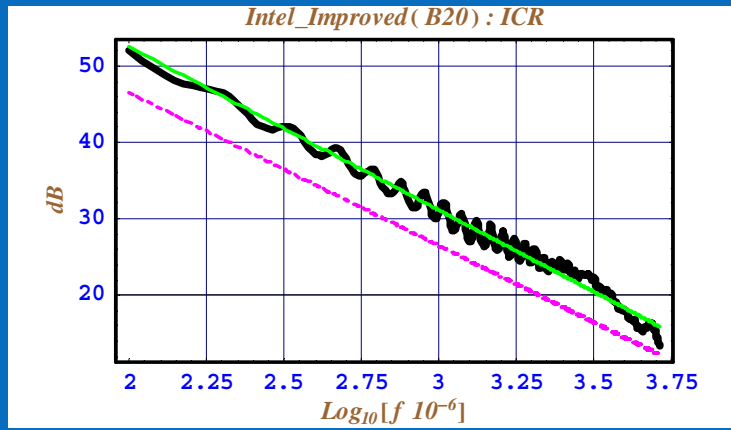
# Intel channels: long channels characteristics (KR port type)



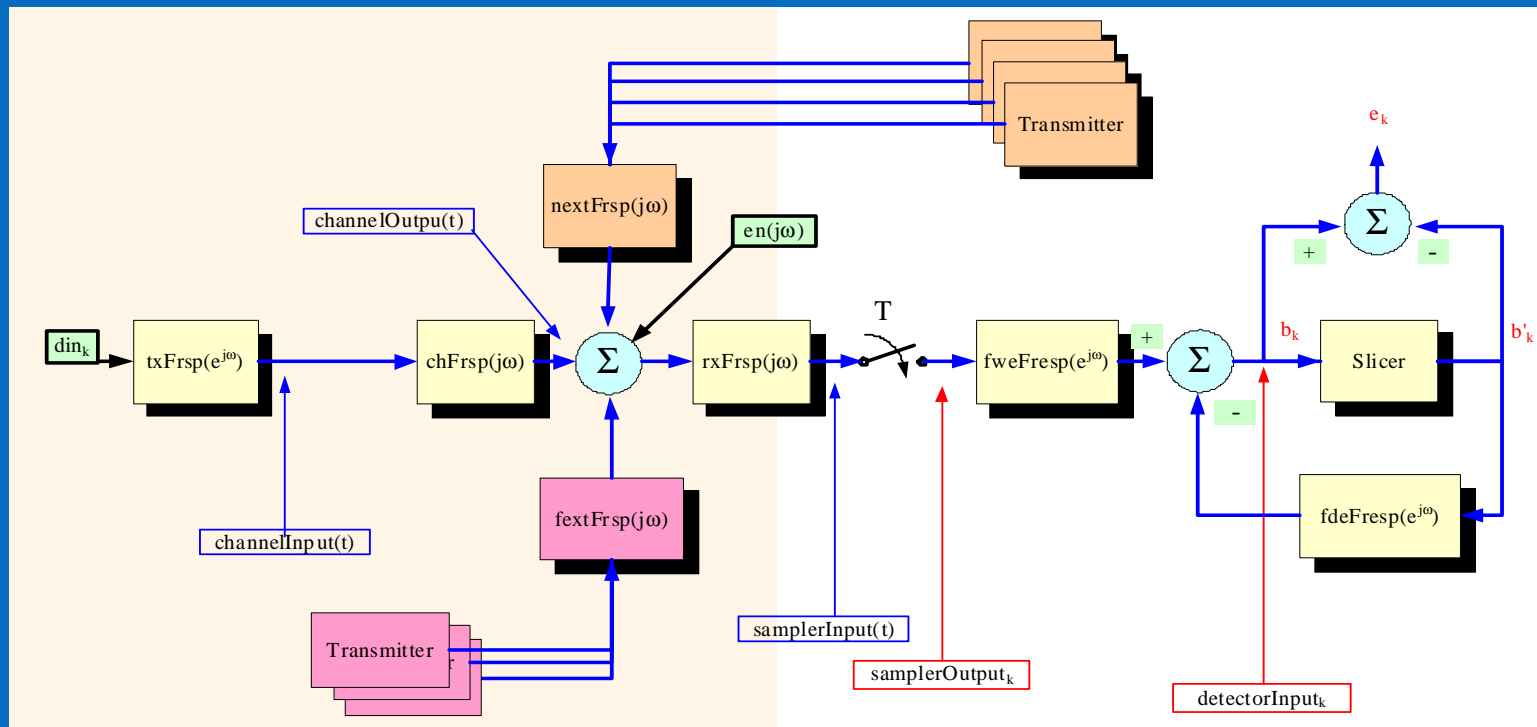
# Intel channels: long channels characteristics (KR port type)



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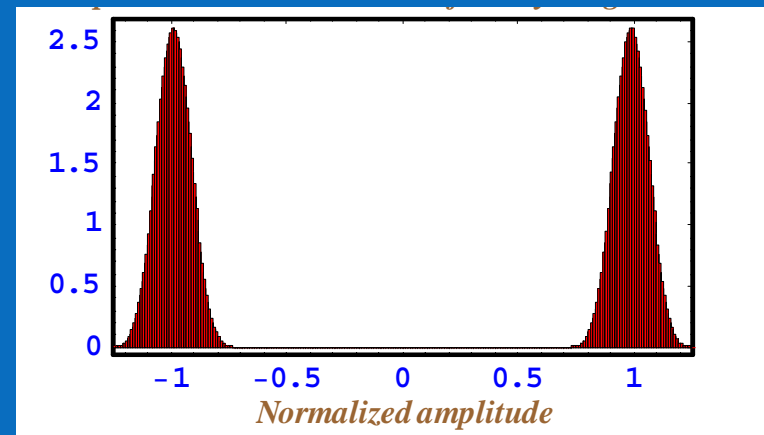
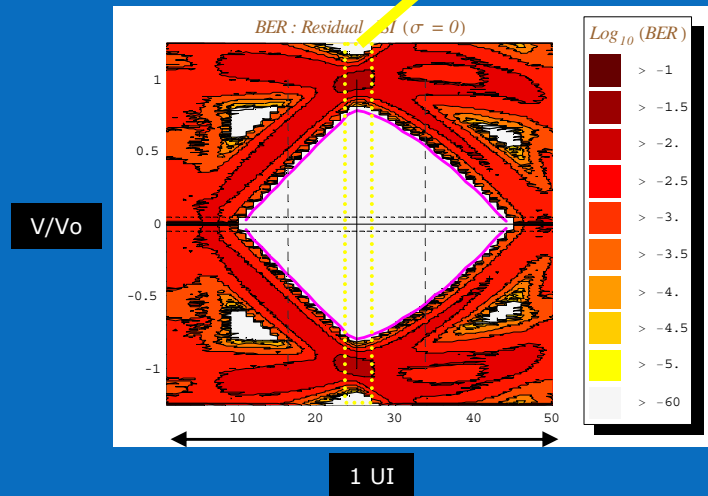


# Simulation Environment (1)

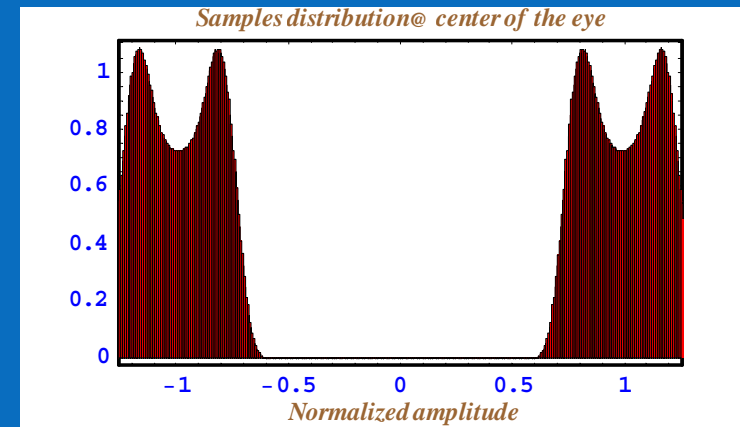
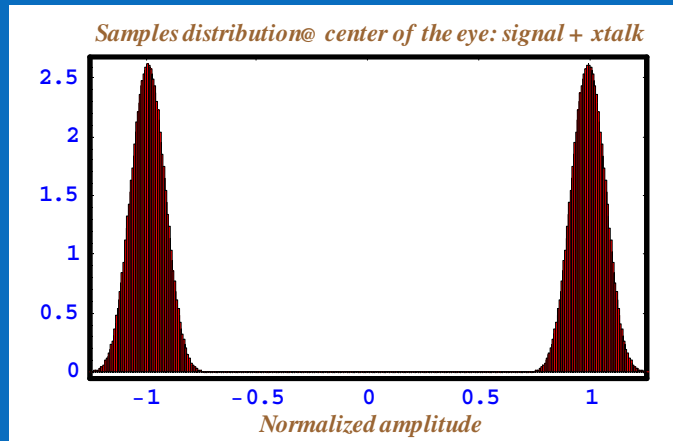
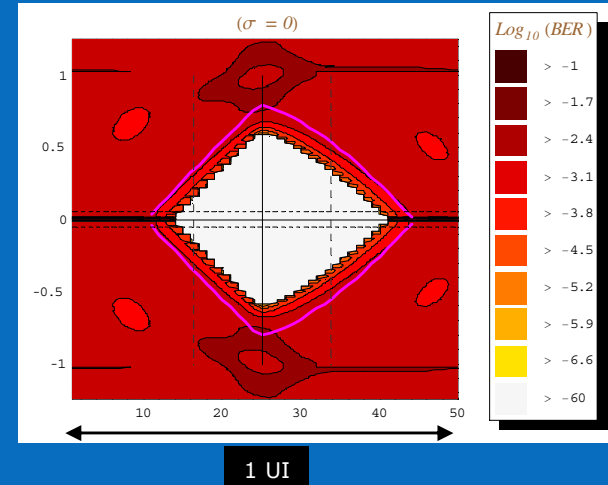
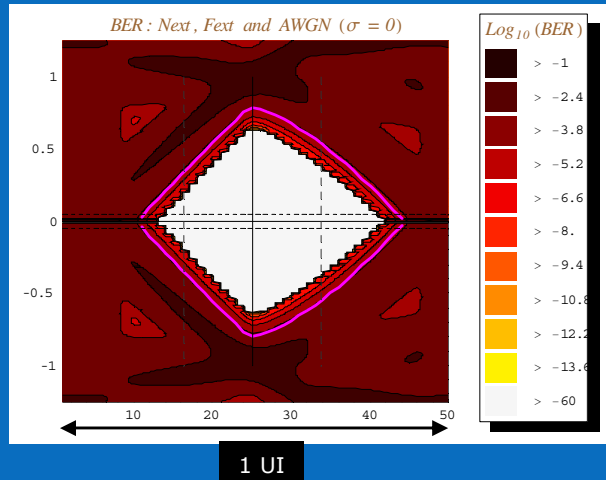


# Simulation Environment (2)

- Simulation conditions:
  - PRBS15 pattern
  - No timing jitter on either transmitter or receiver
  - 3 taps FFE, 5 taps DFE.
    - FFE boost subject to 802.3ap constraints
  - Cross-talk signal is subject to the same equalization conditions as main signal
    - Cross-talk and forward signal have same launch amplitude
  - Transmitter has finite rise/fall time
    - $t_r = t_f = 24$  pS
  - Receiver input amplifier modeled as a two pole low pass filter with poles at  $0.7 f_s$  and  $1.0 f_s$



# Simulation Environment (3)



**PRBS 15 aggressor:**

vertical opening :  $0.251 \text{ mV}_{pp}$   
 horizontal opening :  $0.440 \text{ UI}_{pp}$

**Equivalent sinusoidal aggressor:**

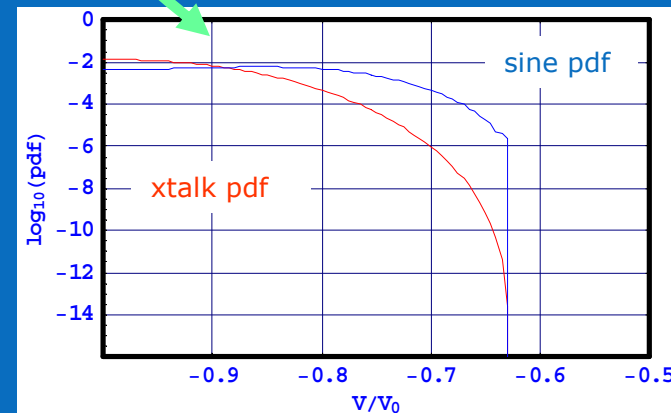
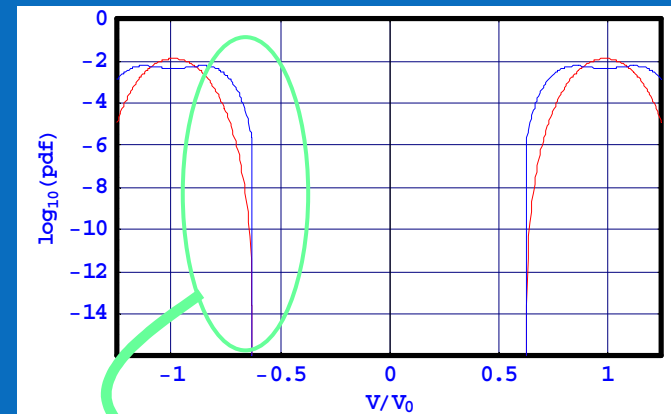
vertical opening :  $0.251 \text{ mV}_{pp}$   
 horizontal opening :  $0.440 \text{ UI}_{pp}$





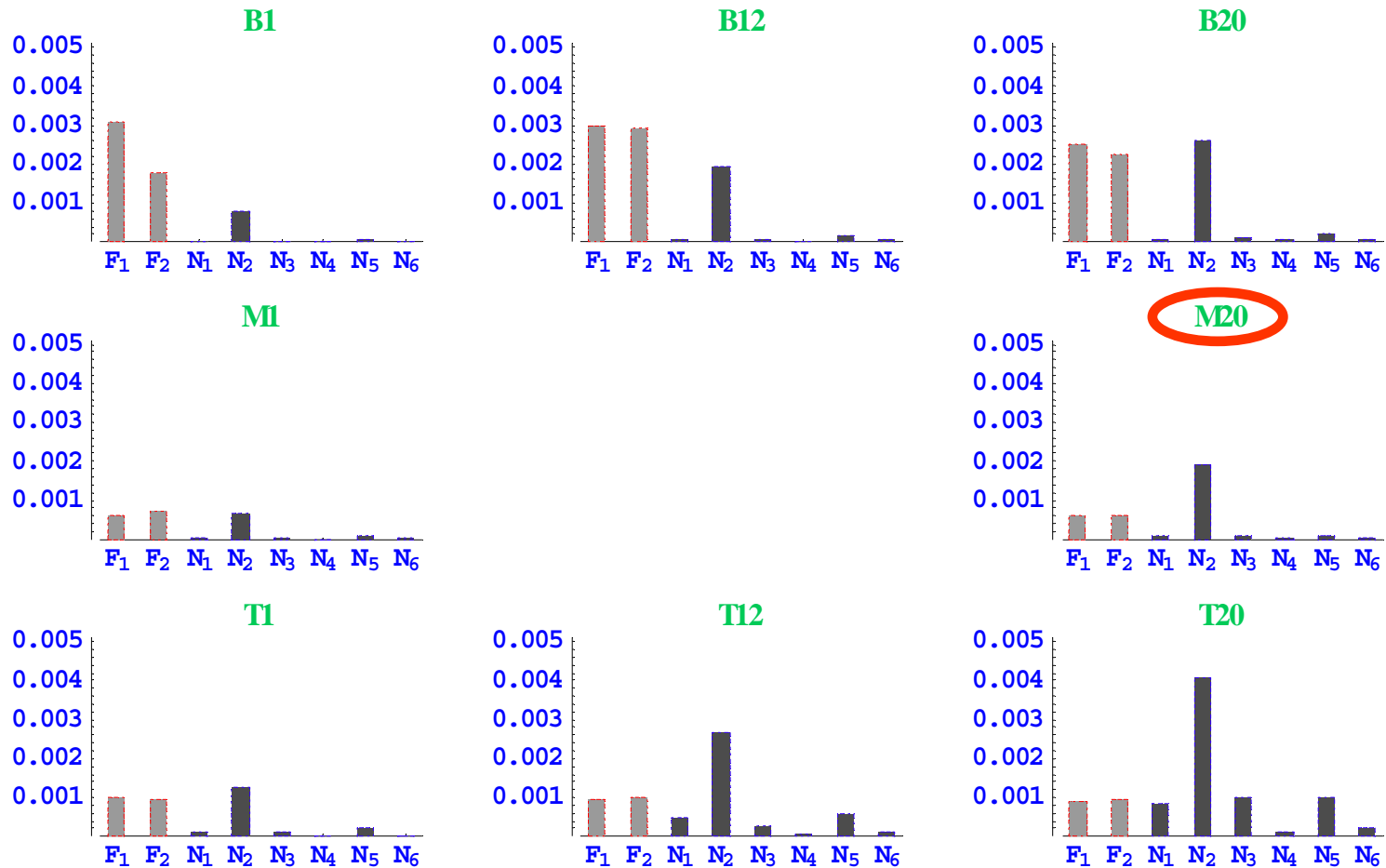
# Simulation Environment (4)

- Same launch voltage for forward and cross -talk signal does not represent a worst case scenario
  - Consistent with Abler\_01\_0106 and Abler\_01\_0206
  - It does not appear that handling of multiple sources of interferers is documented. Is this something that should be taken care of in Clause 69A?
- Use of PRBS15 instead of PRBS23 should still provide a reasonable approximation to the worst case eye at the slicer
  - No particular reason for this choice except simulation time
- Sinusoidal interference changes samples probability distribution at slicer input



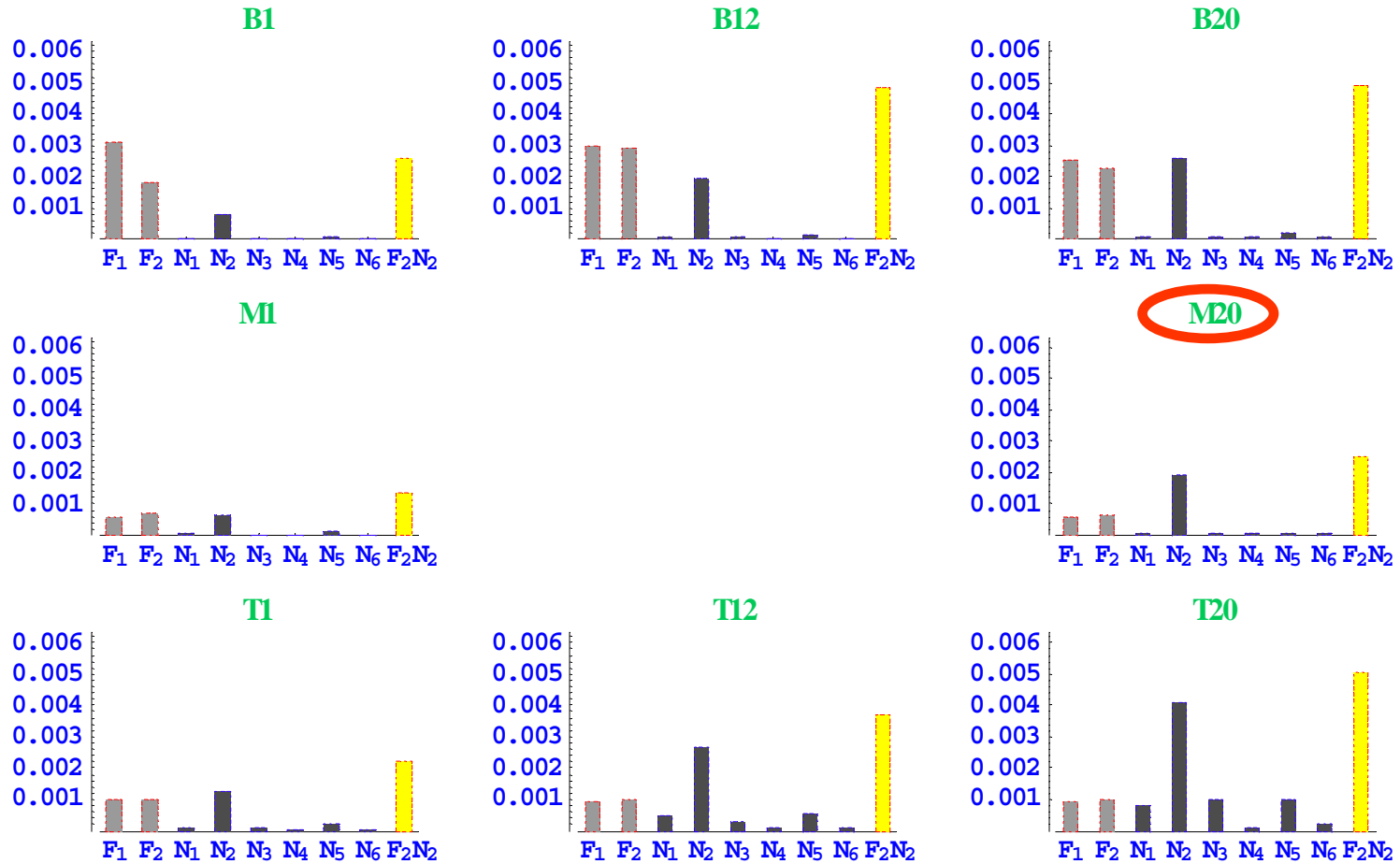
# Intel channels (1)

Intel\_Improved: Xtalk contributions from individual aggressors



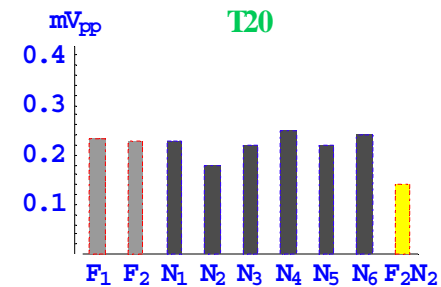
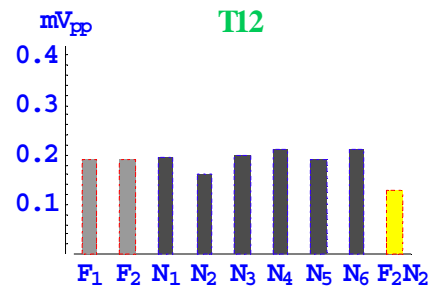
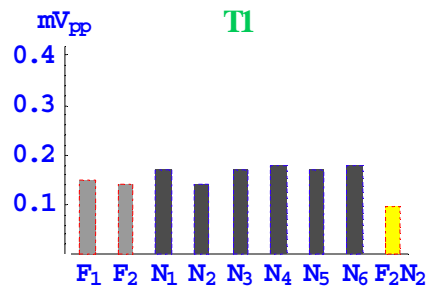
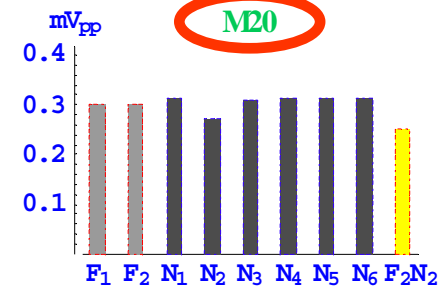
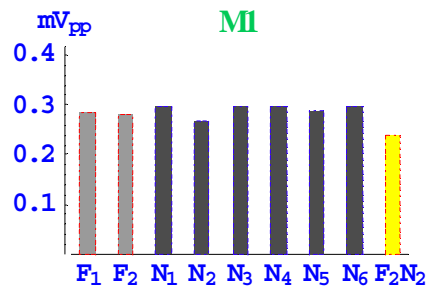
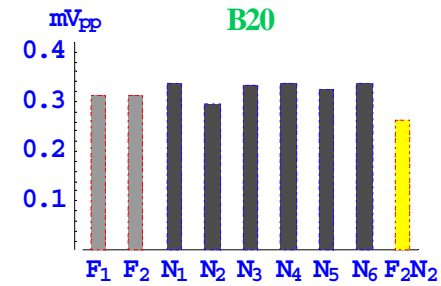
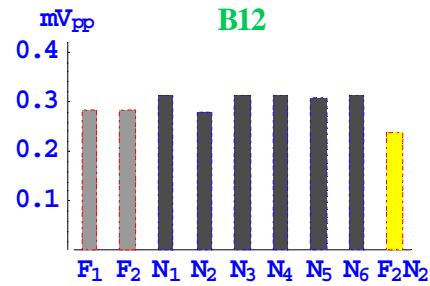
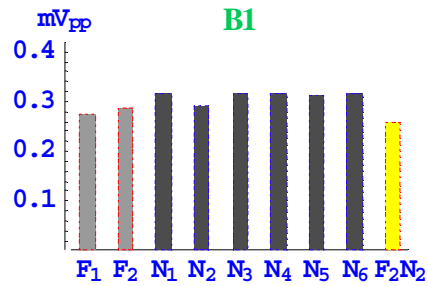
# Intel channels (2)

Intel\_Improved: Xtalk comparison of individual aggressors and mixed term (fext2 + next2)



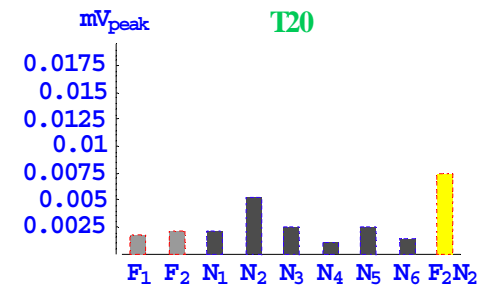
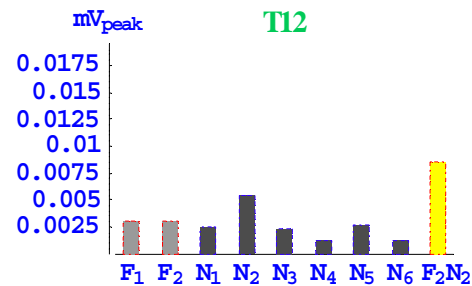
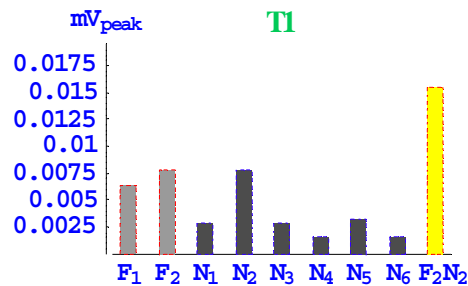
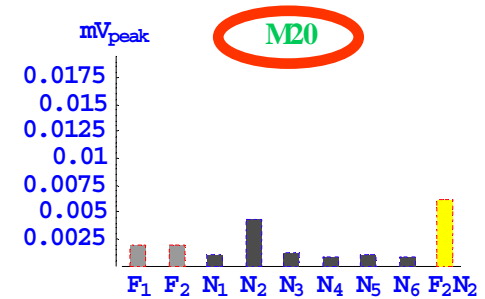
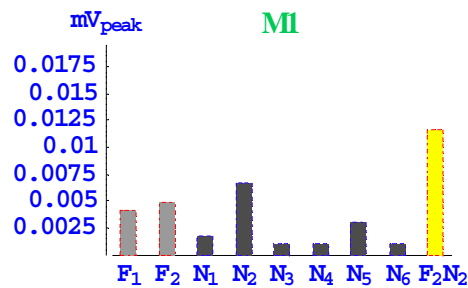
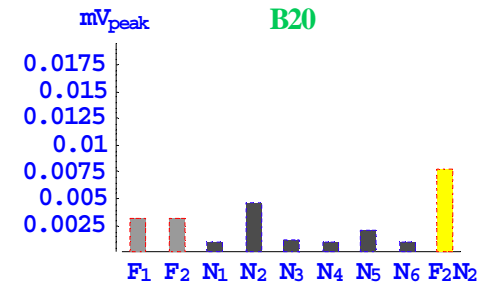
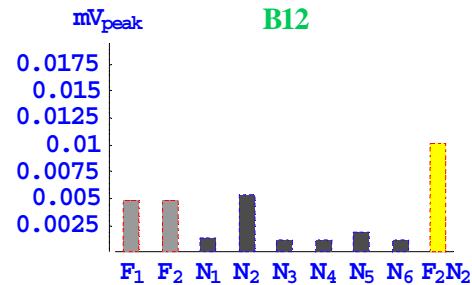
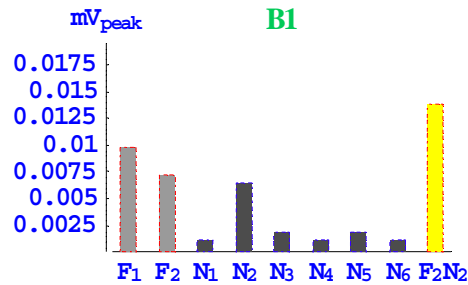
# Intel channels (3)

Intel\_Improved: vertical opening at slicer



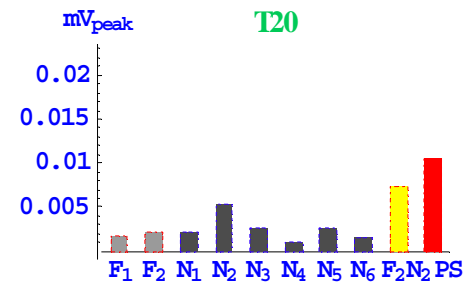
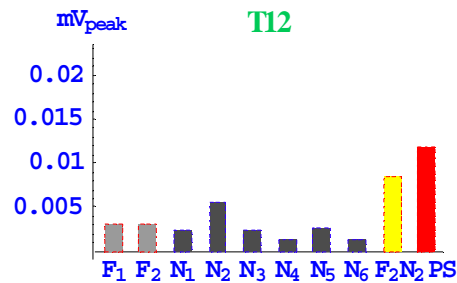
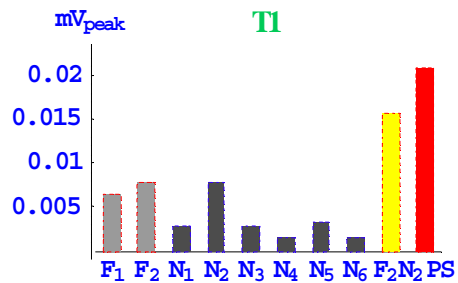
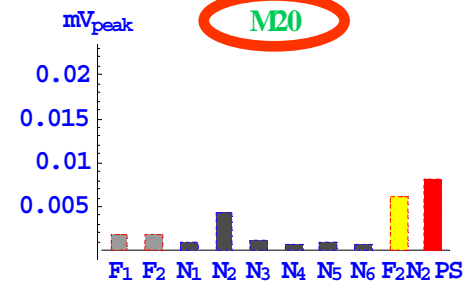
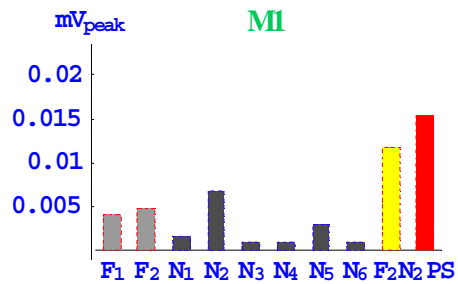
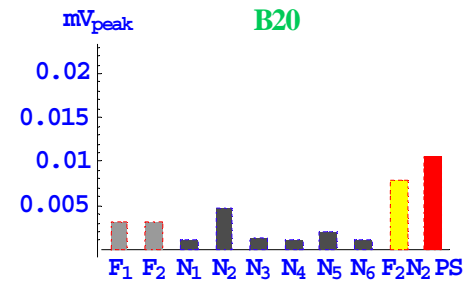
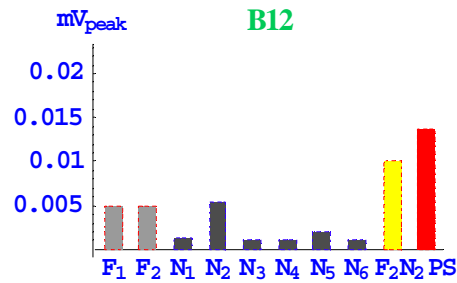
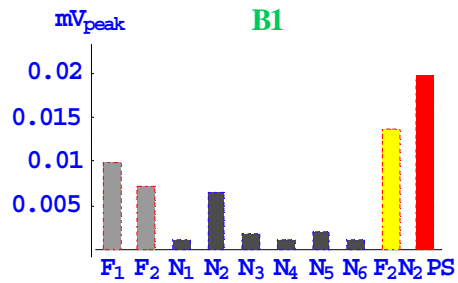
# Intel channels (4)

Intel\_Improved: equivalent sinusoidal interference



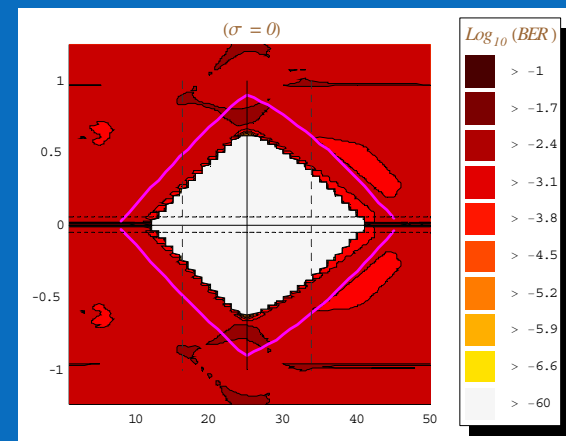
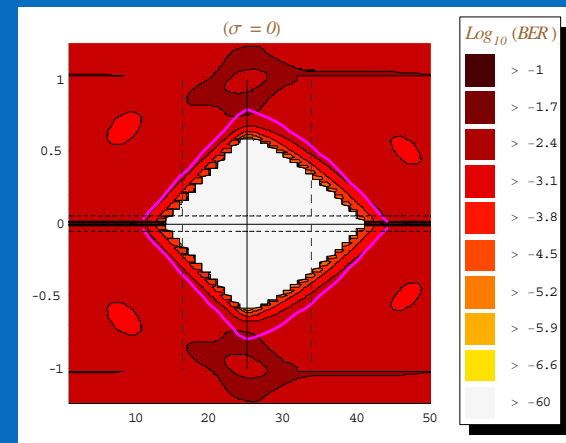
# Intel channels (5)

Intel\_Improved: equivalent sinusoidal interference  
 Comparison of individual terms, combined fe<sub>2</sub> + ne<sub>2</sub> (yellow) and power sum (red).



# M20 vs. ITTC23

- M20
  - Vertical opening: 0.235 mVpp
  - Horizontal opening: 0.4 UIpp
- ITTC23
  - Vertical opening: 0.246 mVpp
  - Horizontal opening: 0.48 UIpp
- Comparison of ITTC23 and M20 indicates a reasonable match in vertical opening.
- Horizontal opening in M20 is reduced with respect to ITTC23, most likely because of self-noise.
  - Comparison of the insertion loss deviation curves for the ITTC23 and M20 channels indicate that the latter Sdd21 curve has more ripple .



# Conclusions

- The amount of interference tolerable by a channel increases as the insertion loss decreases
- For a high loss channel like ITTC23 it is important to establish realistic levels of crosstalk
- The Intel M20 channel represents a reasonable approximation to the EIT channel.
  - The insertion loss curve is within a few dB from the  $A_{\max}(f)$  curve
  - One dominant NEXT aggressor and two significant FEXT aggressors
- The levels of crosstalk observed in the M20 are consistent, in a power sum fashion, with the existing EIT specification of  $15 \text{ mV}_{\text{pp}}$ .
- It is recommended that the EIT spec for a KR port type is maintained at  $15 \text{ mV}_{\text{pp}}$ .



