45. Management Data Input/Output (MDIO) Interface

Editor's notes: To be removed prior to final publication.

1. This clause contains all modifications to clause 45 required by the IEEE P802.3ap project. The text in this clause currently illustrates the new registers required to support AN over electrical backplanes (as referenced in Clause 73) and PMD-specific functions. These changes are written as an amendment to IEEE 802.3an. In some cases 802.3ap needs to change the text in 802.3am. Therefor all changes will proceed with an indication if it is a 802.3an or 802.3ap change. These changes need to be coordinated with changes from the IEEE P802.3an and IEEE P802.3aq projects.

3. Coordinate the combined registers with 802.3an. Place registers to flow sequentially based on 802.3REVam and any amendments to it.

45.2.1 PMA/PMD registers

This is an 802.3an Rev 2.3 change: Change and Insert the following registers 1.147 through 1.32 767 in Table 45-3 with the following:

Table 45–3—PMA/PMD registers

Register address	Register name
1.147 through 1.~~32 767~~149	Reserved
1.150	10GBASE-KR PMD control
1.151	10GBASE-KR PMD status
1.152	10GBASE-KR LP coefficient update
1.153	10GBASE-KR LP status report
1.154	10GBASE-KR LD coefficient update
1.155	10GBASE-KR LD status report
1.156 through ~~1.32 768~~1.32 767	Reserved

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

This is an 802.3am Rev 2.2 change: Change row in Table 45-4 to read as follows:

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[1]
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved 0 0 1 1 = Reserved 0 0 1 0 = 1000BASE-KX 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

[1]R/W = Read/Write, SC = Self Clearing

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.05:2)

This is an 802.3am Rev 2.2 change: Insert a new paragraph to the end of subclause 45.2.1.1.3:

When set to 0010, bits 5:2 select the use of the 1000BASE-KX PMA/PMD.

45.2.1.1.4 PMA loopback (1.0.0)

This is an 802.3am Rev 2.2 change: Change second paragraph to read:

The loopback function is mandatory for the 1000BASE-KX and 10GBASE-X port types and optional for all other port types, except 2BASE-TL and 10PASS-TS, which do not support loopback. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

This is an 802.3am Rev 2.2 change: Change and insert row to Table 45–6 as follows:

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W[1]
1.4.15:~~3~~ 4	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.3	1000BASE-KX	1 = PMA/PMD is capable of operating as 1000BASE-KX 0 = PMA/PMD is not capable of operating as 1000BASE-KX	RO

[1]RO = Read Only

This is an 802.3am Rev 2.2 change: Insert the following subclause before subclause 45.2.1.4.1. Renumber appropriately

45.2.1.4.1 1000BASE-KX capable (1.4.3)

When read as a one, bit 1.4.3 indicates that the PMA/PMD is able to operate as 1000BASE-KX. When read as a zero, bit 1.4.3 indicates that the PMA/PMD is not able to operate as 1000BASE-KX.

45.2.1.7.4 Transmit fault (1.8.11)

This is an 802.3an Rev 2.3 change: Insert before the last sentence in the first paragraph of subclause 45.2.1.7.4 to read as follows:

... The description of the transmit fault function for the 10GBASE-CX4 PMD is given in 54.5.10. The description of the transmit fault function for the 10GBASE-T PMA is given in 55.4.2.2. The description of the transmit fault function for the 1000BASE-KX is given in 70.5.8. The description of the transmit fault function for the 10GBASE-KX4 PMD is given in 71.5.10. The description of the transmit fault function for the 10GBASE-KR PMD is given in 72.5.8. The transmit fault bit shall be implemented with latching high behavior.

45.2.1.7.5 Receive fault (1.8.10)

This is an 802.3an Rev 2.3 change: Insert before the last sentence in the first paragraph of subclause 45.2.1.7.5 to read as follows:

... The description of the receive fault function for the 10GBASE-CX4 PMD is given in 54.5.11. The description of the receive fault function for the 10GBASE-T PMA is given in 55.4.2.4. The description of the receive fault function for the 1000BASE-KX is given in 70.5.9. The description of the receive fault function for the 10GBASE-KX4 PMD is given in 71.5.11. The description of the receive fault function for the 10GBASE-KR PMD is given in 72.5.9. The receive fault bit shall be implemented with latching high behavior.

This is an 802.3an Rev 2.3 change: Insert the following subclauses after 45.2.1.75

45.2.1.76 10GBASE-KR PMD control register (Register 1.150)

renumber following tables and subclauses as required.

Table 45–54—10GBASE-KR PMD control register

Bit(s)	Name	Description	R/W[1]
1.150.15:2	Reserved	Value always zero, writes ignored	R/W
1.150.1	Training enable	1 = Enable the 10GBASE-KR start-up protocol 0 = Disable the 10GBASE-KR start-up protocol	R/W
1.150.0	Restart training	1 = Reset 10GBASE-KR start-up protocol 0 = Normal operation	R/W SC

[1]R/W = Read/Write, SC = self-clearing

45.2.1.76.1 Restart training (1.150.0)

This bit maps to the state variable mr_restart_training as defined in 72.5.10.3.2.

45.2.1.76.2 Training enable (1.150.1)

This bit maps the state variable mr_training_enable as defined in 72.5.10.3.2.

45.2.1.77 10GBASE-KR PMD status register (Register 1.151)

The assignment of bits in the 10GBASE-KR PMD status register is shown in Table 45–54.

Table 45–55—10GBASE-KR PMD status register

Bit(s)	Name	Description	R/W[1]
1.151.15:3	Reserved	Value always zero, writes ignored	RO
1.151.2	Start-up protocol status	1 = Start-up protocol in progress 0 = Start-up protocol complete	RO
1.151.1	Frame lock	1 = Training frame delineation detected 0 = Training frame delineation not detected	RO
1.151.0	Receiver status	1 = Receiver trained and ready to receive data 0 = Receiver training	RO

[1]RO = Read Only

45.2.1.77.1 Receiver status (1.151.0)

This bit maps the state rx_trained as defined in 72.5.10.3.2.

45.2.1.77.2 Frame lock (1.151.1)

This bit maps the state variable frame_lock as defined in 72.5.10.3.2.

45.2.1.77.3 Start-up protocol status (1.151.2)

This bit maps the state variable training as defined in 72.5.10.3.

45.2.1.78 10GBASE-KR LP coefficient update register (Register 1.152)

The 10GBASE-KR coefficient update registers reflect the contents of the first 16-bit word of the training frame control channel. The LP coefficient update register mirrors the contents of the most recently received training frame.

The assignment of bits in the 10GBASE-KR LP coefficient update register is shown in Table 45–55.

45.2.1.78.1 Update gain (1.152.15:14)

The function and values of the update gain bits are defined in 72.5.10.2.3.1.

45.2.1.78.2 Vendor specific (1:152:9:6)

The function and values of the vendor specific bits are defined in 72.5.10.2.3.2.

45.2.1.78.3 Coefficient (k) update (1.152.5:0)

The function and values of the coefficient (k) update bits are defined in 72.5.10.2.3.3.

Table 45–56—10GBASE-KR LP coefficient update register bit definitions

Bit(s)	Name	Description	R/W[1]
1.152.15:14	Update gain	15 14 1 1 = 8 1 0 = 4 0 1 = 2 0 0 = 1	RO
1.152.13:10	Reserved	Value always zero, writes ignored	RO
1.152.9:6	Vendor specific		RO
1.152.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.152.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO
1.152.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	RO

[1]RO = Read Only

45.2.1.79 10GBASE-KR LP status report register (Register 1.153)

The 10GBASE-KR status report registers reflect the contents of the second 16-bit word of the training frame control channel. The LP status report register mirrors the contents of the most recently received training frame.

The assignment of bits in the 10GBASE-KR LP status report register is shown in Table 45–56..

Table 45–57—10GBASE-KR LP status report register bit definitions

Bit(s)	Name	Description	R/W[1]
1.153.15	Receiver ready	1 = The LP receiver has determined that training is complete and is prepared to receive data 0 = The LP receiver is requesting that training continue	RO
1.153.14:10	Reserved	Value always 0, writes ignored	RO
1.153.9:6	Vendor specific		RO
1.153.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO
1.153.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	RO

[1]RO = Read Only

45.2.1.79.1 Receiver ready (1.153.15)

The function and values for the receiver ready bit are defined in 72.5.10.2.4.1.

45.2.1.79.2 Vendor specific (1.153:9:6)

The function and values for the vendor specific bits are defined in 72.5.10.2.4.2.

45.2.1.79.3 Coefficient (k) status (1.153.5:0)

The function and values for the coefficient status bits are defined in 72.5.10.2.4.3.

45.2.1.80 10GBASE-KR LD coefficient update register (Register 1.154)

The 10GBASE-KR coefficient update registers reflect the content of the first 16-bit word of the training frame control channel as defined in 75.5.10.2. The LD coefficient update register represents the contents of the current outgoing training frame, as defined by the LD receiver adaptation process.

The assignment of bits in the 10GBASE-KR LD coefficient update register is shown in Table 45–57.

45.2.1.80.1 Update gain (1.154.15:14)

The function and values of the update gain bits are defined in 72.5.10.2.3.1.

45.2.1.80.2 Vendor specific (1.154.9:6)

The function and values of the vendor specific bits are defined in 72.5.10.2.3.2.

45.2.1.80.3 Coefficient (k) update(1.154.5:0)

The function and values of the coefficient (k) update bits are defined in 72.5.10.2.3.3.

Table 45–58—10GBASE-KR LD coefficient update register bit definitions

Bit(s)	Name	Description	R/W[1]
1.154.15:14	Update gain	15 14 1 1 = 8 1 0 = 4 0 1 = 2 0 0 = 1	R/W
1.154.13:10	Reserved	Value always 0, writes ignored	R/W
1.154.9:6	Vendor specific		R/W
1.154.5:4	Coefficient (+1) update	5 4 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.154.3:2	Coefficient (0) update	3 2 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W
1.154.1:0	Coefficient (–1) update	1 0 1 1 = reserved 0 1 = increment 1 0 = decrement 0 0 = hold	R/W

[1]R/W = Read/Write, SC = self-clearing

45.2.1.81 10GBASE-KR LD status report register (Register 1.155)

The 10GBASE-KR status report registers reflect the content of the second 16-bit word of the training frame control channel as defined in 75.5.10.2. The LD status report register represents the contents of the current outgoing training frame, as defined in the training state diagram in Figure 72–4.

The assignment of bits in the 10GBASE-KR LD status report register is shown in Table 45–58.

Table 45–59—10GBASE-KR LD status report register bit definitions

Bit(s)	Name	Description	R/W[1]
1.155.15	Receiver ready	1 = The LD receiver has determined that training is complete and is prepared to receive data 0 = The LD receiver is requesting that training continue	R/W
1.155.14:10	Reserved	Value always 0, writes ignored	R/W
1.155.9:6	Vendor specific		R/W
1.155.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W
1.155.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W
1.155.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W

[1]R/W = Read/Write, SC = self-clearing

45.2.1.81.1 Receiver ready (1.155.15)

The function and values for the receiver ready bit are defined in 72.5.10.2.4.1.

45.2.1.81.2 Vendor specific (1.155.9:6)

The function and values for the vendor specific bits are defined in 72.5.10.2.4.2.

45.2.1.81.3 Coefficient (k) status (1.155.5:0)

The function and values for the update gain bits are defined in 72.5.10.2.4.3.

45.2.7 Auto-Negotiation registers

This is an 802.3an Rev 2.3 change: Insert the following AN information as 45.2.7 and shift other subclauses. Renumber tables to flow sequentially based on 802.3REVam and any amendments to it.

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Table 45–117—AN MMD registers

Register Address	Register name
7.16, 7.17, 7.18	AN LD advertisement
7.19, 7.20, 7.21	AN LP base page
7.22, 7.23, 7.24	AN LD NP
7.25, 7.26, 7.27	AN LP NP
7.28 through 7.47	Reserved for 802.3an
7.48	BP Ethernet status
7.49 through 7.32 767	Reserved
7.32 768 through 7.65 535	Vendor specific

45.2.7.1 AN control register (Register 7.0)

This is an 802.3an Rev 2.3 change: Insert paragraph at the end of subclause 45.2.7.1:

A device that supports multiple port types may implement both Clause 22 control register operation and Clause 45 control register operation. Some control functions have been duplicated in both definitions. The register bits to control these functions are simply echoed in both locations, any reads or writes to these bits behave identically whether made through the Clause 22 location or the Clause 45 location.

45.2.7.2 AN status (Register 7.1)

This is an 802.3an Rev 2.3 change: Change and Insert rows in Table 45-119 as follows:

Table 45–119—AN status register bit definitions

Bit(s)	Name	Description	R/W[1]
7.1.15:~~8~~12	Reserved	Ignore on read	RO
7.1.11	LD Next Page Able	1 = LD is Next Page Able 0 = LD is not Next Page Able	RO
7.1.10	LP Next Page Able	1 = LP is Next Page Able 0 =LP is not Next Page Able	RO
7.1.9	Parallel detection Fault	1 = A fault has been detected via the parallel detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO LH
7.1.8	Reserved	Ignore on read	RO
7.1.7	Extended next page status	1 = Extended next page will be used 0 = Extended next page will not be used	RO
7.1.6	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO LH
7.1.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.1.4	Remote fault	1 = Remote fault condition detected 0 = no Remote fault condition detected	RO LH SC
7.1.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.1.2	Link Status	1 = Link is up 0 = Link is down	RO LL SC
7.1.~~2:0~~1	Reserved	Ignore on read	RO
7.1.0	LP Auto-Negotiation able	1 = LP is Auto-Negotiation able 0 = LP is not Auto-Negotiation able	RO

[1]RO = Read Only, LH = Latching High, SC = Self-Clearing, LL = Latching Low

This is an 802.3an Rev 2.3 change: Insert the following subclauses after Table 45-119 and renumber subclauses appropriatly:

45.2.7.2.1 LD Next Page Able (7.1.11)

The LD Next Page Able bit (7.1.11) shall be set to logic one to indicate that the local device supports the Next Page function. The LD Next Page Able bit (7.1.11) shall be set to logic zero if the Next Page function is not supported.

45.2.7.2.2 LP Next Page Able (7.1.10)

The LP Next Page Able bit (7.1.10) shall be set to logic one to indicate that the link partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the link partner does not support the Next Page function.

45.2.7.2.3 Parallel detection fault (7.1.9)

The parallel detection Fault bit (7.1.9) shall be set to one to indicate that more than one of 1000BASE-KX, or 10GBASE-KX4 or 10GBASE-KR PMAs have indicated sync_status=OK or sync_status=READY when the autoneg_wait_timer expires. The parallel detection fault bit shall be reset to zero on a read of the AN status register (Register 7.1).

45.2.7.2.4 LP AN able (7.1.0)

The LP AN ability bit (7.1.0) shall be set to one to indicate that the LP is able to participate in the AN function. This bit shall be reset to zero if the LP is not AN able.

45.2.7.3 AN Advertisement Registers (7.16, 7.17, 7.18)

Table 45–120—AN Advertisement register(s) bit definitions

Bit(s)	Name	Description	R/W[1]
7.18.15:0	Technology Ability Field	A[26:11] See 73.6.4	R/W
7.17.15:5	Technology Ability Field	A[10:0] See 73.6.4	R/W
7.17.4:0	Transmitted Nonce Field	T[4:0] See 73.6.3	R/W
7.16.15	Next Page	See 73.6.8	R/W
7.16.14	Acknowledge	See 73.6.7	RO
7.16.13	Remote Fault	See 73.6.6	R/W
7.16.12	C2	See 73.6	R/W
7.16.11:10	Pause	C1:C0 See 73.6.5	R/W
7.16.9:5	E4:E0	See 73.6.2	R/W
7.16.4:0	Selector Field	See 73.6.1	R/W

[1]R/W = Read/Write, RO = Read Only

If BP AN ability bit in the BP Ethernet status register (7.48) is set to one then the AN advertisement register(s) (7.16 through 7.18) contain the advertised ability of the BP Ethernet PHY. (See Table 73–4).The bit definition for the base page is defined in 73.6. On power-up, before AN starts, this register shall have the following configuration: The Selector Field (7.16.4:0) is set to an appropriate code as specified in Annex 28A.

When multiple registers are used, the value of the registers is latched when the first register is read and reads of the second and third registers and following return the latched value rather than the current value.

For writable registers, the value is only used by the state diagram when the first register is written. For the base page, the value is transferred to mr_adv_ability when the first word is written. For the next pages, the

value is transferred to mr_np_tx and mr_next_page_loaded is set when the first word is written. Therefore, when writing all three registers the second and third registers should be written before the first register.

The Acknowledge bit (7.16.14) is set to zero. The Technology Ability Field A[26:0] ({7.18.15:0, 7.17.15:5}) is set according to the appropriate Backplane Ethernet port type values set in the PMA/PMD registers 1.4, 1.7 and 1.11.

Only the bits in the Technology Ability Field that represent the technologies supported by the LD may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management before a renegotiation. This can be used to enable management to auto-negotiate to an alternate common mode.

The management entity may initiate renegotiation with the LP using alternate abilities by setting the Selector Field (7.16.4:0) and the Technology Ability Field A[26:0] ({7.18.15:0, 7.17.15:5}) to indicate the preferred mode of operation and setting the Restart AN bit (7.0.9) in the AN control register (Register 7.0) to one.

Any writes to this register prior to completion of AN as indicated by bit 7.1.5 should be followed by a renegotiation for the new values to be properly used for AN. Once AN has completed, this register value may be examined by software to determine the highest common denominator technology.

45.2.7.4 AN LP base page ability register(s) (7.19, 7.20, 7.21)

If BP AN ability bit in the BP Ethernet status register (7.48) is set to one then the AN LP base page ability register(s) (7.19 through 7.21) contain the LP base page ability of the BP Ethernet PHY. (See Table 73–4).

All of the bits in the AN LP ability registers are read only. A write to the AN LP ability registers shall have no effect.

These registers contain the Advertised Ability of the LP's PHY (Base page). (See Table 73–4 and 73.6.) The bit definitions shall be a direct representation of the received Link Code Word (Figure 73–5). Upon successful completion of AN, status register (Register 7.1) AN Complete bit (7.1.5) shall be set to one.

Table 45–121—AN LP base page ability register(s) bit definitions

Bit(s)	Name	Description	R/W[1]
7.21.15:0	Technology Ability Field	A[26:11] See 73.6.4	RO
7.20.15:5	Technology Ability Field	A[0:10] See 73.6.4	RO
7.20.4:0	Transmitted Nonce Field	T[4:0] See 73.6.3	R/W
7.19.15	Next Page	See 73.6.8	RO
7.19.14	Acknowledge	See 73.6.7	RO
7.19.13	Remote Fault	See 73.6.6	RO
7.19.12	C2	See 73.6	RO
7.19.11:10	Pause	C1:C0 See 73.6.5	RO
7.19.9:5	E4:E0	See 73.6.2	RO
7.19.4:0	Selector Field	See 73.6.1	RO

[1]R/W = Read/Write, RO = Read Only

45.2.7.5 AN LD NP transmit Register(s) (7.22, 7.23, 7.24)

If BP AN ability bit in the BP Ethernet status register (7.48) is set to one then the AN LD NP transmit Register(s) (7.22 through 7.24) contain the AN LD Next page Link Code Word of the BP Ethernet PHY. (See 73.7.7.1).

The AN LD NP Transmit register(s) contain the Next Page Link Code Word to be transmitted when Next Page ability is supported. (See Table 45–122.) The contents are defined in 73.7.7.1. On powerup, this register shall contain the default value which represents a Message Page with the Message Code set to Null Message. This value may be replaced by any valid Next Page Message Code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

Table 45–122—AN Next Page transmit bit definitions

Bit(s)	Name	Description	R/W[1]
7.24.15:0	Unformatted Code Field	U[31:16] or U[42:27] See 73.7.7.1	R/W
7.23.15:0	Unformatted Code Field	U[0:15] or U[26:11] See 73.7.7.1	R/W
7.22.15	Next Page	See 73.7.7.1	R/W
7.22.14	Acknowledge	See 73.7.7.1	R/W
7.22.13	Message/Unformatted Page	See 73.7.7.1	R/W
7.22.12	Acknowledge 2	See 73.7.7.1	R/W
7.22.11	Toggle	See 73.7.7.1	R/W
7.22.10:0	Message/Unformatted Code Field	See 73.7.7.1	R/W

[1]R/W = Read/Write

45.2.7.6 AN LP NP register(s) (7.25, 7.26, 7.27)

If BP AN ability bit in the BP Ethernet status register (7.48) is set to one then the AN LP NP register(s) Register(s) (7.25 through 7.27) contain the AN LP Next page Link Code Word of the BP Ethernet PHY. (See 73.7.7.1).

The AN LP Next Page register contains the next Page Link Code Word received from the LP as shown in Table 45–123. All of the bits in the AN LP Received Next Page register are read only. A write to the AN LP Received Next Page register shall have no effect.

The values contained in this register are valid only after the Page Received bit (7.30.1) has been set to logical one or once AN has successfully completed, as indicated by bit 7.1.5.

NOTE– If this register is used to store multiple LP Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent LP Next Pages.

Table 45–123—AN LP NP register(s) bit definitions

Bit(s)	Name	Description	R/W[1]
7.27.15:0	Unformatted Code Field	U[31:16] or U[42:27] See 73.7.7.1x	R/W
7.26.15:0	Unformatted Code Field	U[0:15] or U[26:11] See 73.7.7.1x	R/W
7.25.15	Next Page	See 73.7.7.1	R/W
7.25.14	Acknowledge	See 73.7.7.1	R/W
7.25.13	Message/Unformatted Page	See 73.7.7.1	R/W
7.25.12	Acknowledge 2	See 73.7.7.1	R/W
7.25.11	Toggle	See 73.7.7.1	R/W
7.25.10:0	Message/Unformatted Code Field	See 73.7.7.1	R/W

[1]R/W = Read/Write

Editor's notes: *To be removed prior to final publication*

1. The registers 7.48 through 7.83 are Backplane specific and for the purpose of this document will start the paragraph numbering with 45.2.7.100 and Table 45-200. When merging into the final 802.3am, renumber the paragraphs and tables appropriately

45.2.7.100 Backplane Ethernet status (Register 7.48)

Table 45–200—Backplane Ethernet status register (Register 7.48) bit definitions

Bit(s)	Name	Description	RO[1]
7.48.15:4	Reserved	Ignore on read	RO
7.48.3	10GBASE-KR	1 = PMA/PMD is negotiated to perform 10GBASE-KR 0 = PMA/PMD is not negotiated to perform 10GBASE-KR This bit is an exact copy of bit 1.11.2	RO
7.48.2	10GBASE-KX4	1 = PMA/PMD is negotiated to perform 10GBASE-KX4 0 = PMA/PMD is not negotiated to perform 10GBASE-KX4	RO
7.48.1	1000BASE-KX	1 = PMA/PMD is negotiated to perform 1000BASE-KX 0 = PMA/PMD is not negotiated to perform 1000BASE-KX	RO
7.48.0	BP AN ability	1 = PHY is able to perform BP Ethernet AN 0 = PHY is not able to perform BP Ethernet AN	RO

[1]RO = Read Only

45.2.7.100.1 Port Type Negotiated (7.48.1, 7.48.2, 7.48.3)

When AN process has been completed as indicated by the AN complete bit, one of the three bits (1000BASE-KX, 10GBASE-KX4, 10GBASE-KR) indicate the Port Type Negotiated. Only one of the 3 bits are set depending on the priority resolution function.

45.2.7.100.2 Backplane Ethernet AN ability (7.48.0)

When read as a one, bit 7.48.0 indicates that the PMA/PMD has the ability to perform Backplane Ethernet AN. When read as a zero, bit 7.48.0 indicates that the PMA/PMD lacks the ability to perform Backplane Ethernet AN.

45.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 45, MDIO Interface

45.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std. 802.3ap-200x, Clause 45 MDIO interface, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

45.5.2 Identification

45.5.2.1 Implementation identification

Supplier	
Contact point for enquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s)	
Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

45.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ap-200x, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ap-200x)	
Date of Statement	

45.5.2.3 Major capabilities/options

Insert following row at end of table:

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Implementation of Auto-negotiation MMD	45.2.7		O	Yes [ ] No [ ]

45.5.3 PICS proforma tables for Management Data Input Output (MDIO) interface

45.5.3.2 PMA/PMD MMD options

Insert following row to end of table:

Item	Feature	Subclause	Value/Comment	Status	Support
*BPE	Implementation of a Backplane Ethernet PMA/PMD	45.1		PMA:O	Yes [ ] No [ ]

45.5.3.3 PMA/PMD management functions

Modify existing rows in table, identified by Item column, as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MM23	10G PMA/PMD type is selected using bits ~~2~~3:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]

Add rows to table. Order placement alphabetically by Item column

Item	Feature	Subclause	Value/Comment	Status	Support
MM20a	Extensions for Backplane Ethernet at 1.150 through 1.155	45.2.1.2.2		BPE:M	Yes [ ] N/A [ ]

45.5.3.4 Auto-negotiation options

Insert a new subclause after TC management function and renumber subclauses appropriately:

Item	Feature	Subclause	Value/Comment	Status	Support
*AB	Implementation of Backplane Ethernet Auto-negotiation	45.2.7		AN:O	Yes [ ] No [ ] N/A [ ]
*ABN	Implementation of Next Page support for Backplane Ethernet Auto-negotiation	45.2.7		AB:O	Yes [ ] No [ ] N/A [ ]

45.5.3.5 Auto-negotiation management functions

Insert a new subclause immediately following "Auto-negotiation options":

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Action on reset	45.2.7.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	AN:M	Yes [ ] N/A [ ]
AM2	Return one until reset completed	45.2.7.1.1		AN:M	Yes [ ] N/A [ ]
AM3	Reset completes within 0.5 s	45.2.7.1.1		AN:M	Yes [ ] N/A [ ]
AM4	Device responds to reads of register bit 7.0.15	45.2.7.1.1	All other register bits should be ignored	AN:M	Yes [ ] N/A [ ]
AM5	Auto-negotiation enabled by setting bit 7.0.12	45.2.7.1.2		AN:M	Yes [ ] N/A [ ]
AM6	Bits 1.0.13, 1.0.6, 1.0.5:2, and 1.7.3:0 will have not effect and auto-negotiation will determine link configuration	45.2.7.1.2		AN:M	Yes [ ] N/A [ ]
AM7	Attempts to write a ONE to 7.0.12 shall be ignored	45.2.7.1.2	if 7.48.3 indicates LD lacks ability to perform Backplane Ethernet AN	AN:M	Yes [ ] N/A [ ]
AM8	PMA/PMD returns ZERO in bit 7.0.9	45.2.7.1.3	If PMA/PMD lacks ability to perform AN or if AN is disabled	AN:M	Yes [ ] N/A [ ]
AM9	Writes will be ignored to bit 7.0.9	45.2.7.1.3	If PMA/PMD lacks ability to perform AN or if AN is disabled	AN:M	Yes [ ] N/A [ ]
AM10	Setting bit 7.0.9 to one restarts auto-negotiation if supported and enabled	45.2.7.1.3		AN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
AM11	Bit set until auto-negotiation started then self cleared to zero	45.2.7.1.3		AN:M	Yes [ ] N/A [ ]
AM12	Setting the bit to zero has no effect on auto-negotiation process	45.2.7.1.3		AN:M	Yes [ ] N/A [ ]
AM13	Writes to register ignored	45.2.7.2		AN:M	Yes [ ] N/A [ ]
AM14	LD Next Page Able bit (7.1.11)	45.2.7.2.1	Set to indicate that the LD supports Next Page function	AN:M	Yes [ ] No [ ] N/A [ ]
AM15	LD Next Page support (7.1.11)	45.2.7.2.1	ONE to indicate LD supports Next Page function	AN:M	Yes [ ] N/A [ ]
AM16	LD Next Page Able bit (7.1.11)	45.2.7.2.1	ZERO to indicate LD does not support Next Page function	AN:M	Yes [ ] N/A [ ]
AM17	LP Next Page support (7.1.10)	45.2.7.2.2	ONE to indicate LP supports Next Page function	AN:M	Yes [ ] N/A [ ]
AM18	LP Next Page Able bit (7.1.10)	45.2.7.2.2	ZERO to indicate LP does not support Next Page function	AN:M	Yes [ ] N/A [ ]
AM19	Parallel detection fault (7.1.9)	45.2.7.2.3	ONE to indicate more than one Backplane Ethernet PMA indicates sync_status of OK or READY when autoneg_wait_timer expires	AB:M	Yes [ ] N/A [ ]
AM20	Parallel detection fault clearing	45.2.7.2.3	ZERO on read of the AN status register.	AN:M	Yes [ ] N/A [ ]
AM21	Page Received (7.1.6)	45.2.7.2.4	ONE to indicate a new Link Code Word has been stored in AN LP ability registers	AN:M	Yes [ ] N/A [ ]
AM22	Page Received clearing	45.2.7.2.4	ZERO on read of the AN status register.	AN:M	Yes [ ] N/A [ ]
AM23	Auto-Negotiation complete (7.1.5) behavior when AN disabled	45.2.7.2.5	returns value of ZERO	AN:M	Yes [ ] N/A [ ]
AM24	Auto-Negotiation complete (7.1.5) behavior when AN not supported	45.2.7.2.5	returns value of ZERO.	AN:M	Yes [ ] N/A [ ]
AM25	Remote fault bit latches high	45.2.7.2.6	Remains set until cleared.	AN:M	Yes [ ] N/A [ ]
AM26	Remote fault bit behavior when register 7.1 is read	45.2.7.2.6	Bit cleared.	AN:M	Yes [ ] N/A [ ]
AM27	Remote fault bit behavior when AN reset	45.2.7.2.6	Bit cleared.	AN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
AM28	Link Status (7.1.2) latches low	45.2.7.2.8	Remains cleared until bit is read via management	AN:M	Yes [ ] N/A [ ]
AM29	LP AN able (7.1.0) set	45.2.7.2.9	ONE if LP is able to participate in the AN function	AN:M	Yes [ ] N/A [ ]
AM30	LP AN able (7.1.0) no set	45.2.7.2.9	ZERO if LP is not AN able	AN:M	Yes [ ] N/A [ ]
AM31	AN advertisement register values on power-up	45.2.7.3	Selector field is set per Annex 28A	AN:M	Yes [ ] N/A [ ]
AM32	Writes do not effect AN LP ability register values	45.2.7.4		AN:M	Yes [ ] N/A [ ]
AM33	AN LP ability register value	45.2.7.4	Set by received Link Code Word	AN:M	Yes [ ] N/A [ ]
AM34	AN Complete bit (7.1.5) set	45.2.7.4	Upon successful completion of AN	AN:M	Yes [ ] N/A [ ]
AM35	AN LD NP transmit registers value on power-up	45.2.7.5	Default value corresponding to a Null Message.	ABN:M	Yes [ ] N/A [ ]
AM36	AN LD NP transmit registers action when written	45.2.7.5	mr_next_page_loaded set to true.	ABN:M	Yes [ ] N/A [ ]
AM37	Writes do not effect AN LP NP registers values	45.2.7.6		ABN:M	Yes [ ] N/A [ ]