Transmitter DCD Limits

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Characteristics of DCD (Duty Cycle Distortion)

- A Form of Tx Deterministic Jitter
- Primary Frequency Component is High (at Nyquist)
- Subject to Phase Noise Amplification (PNA)
  - Jitter Amplified by Lowpass Filter or Lowpass Channel
  - DCD Jitter at TP4 May Be 2X or 3X DCD Jitter at TP1
  - Reduced By Rx Equalizer (Equalizer Counteracts Lowpass Effects)
- Net Jitter Into Slicer Still High

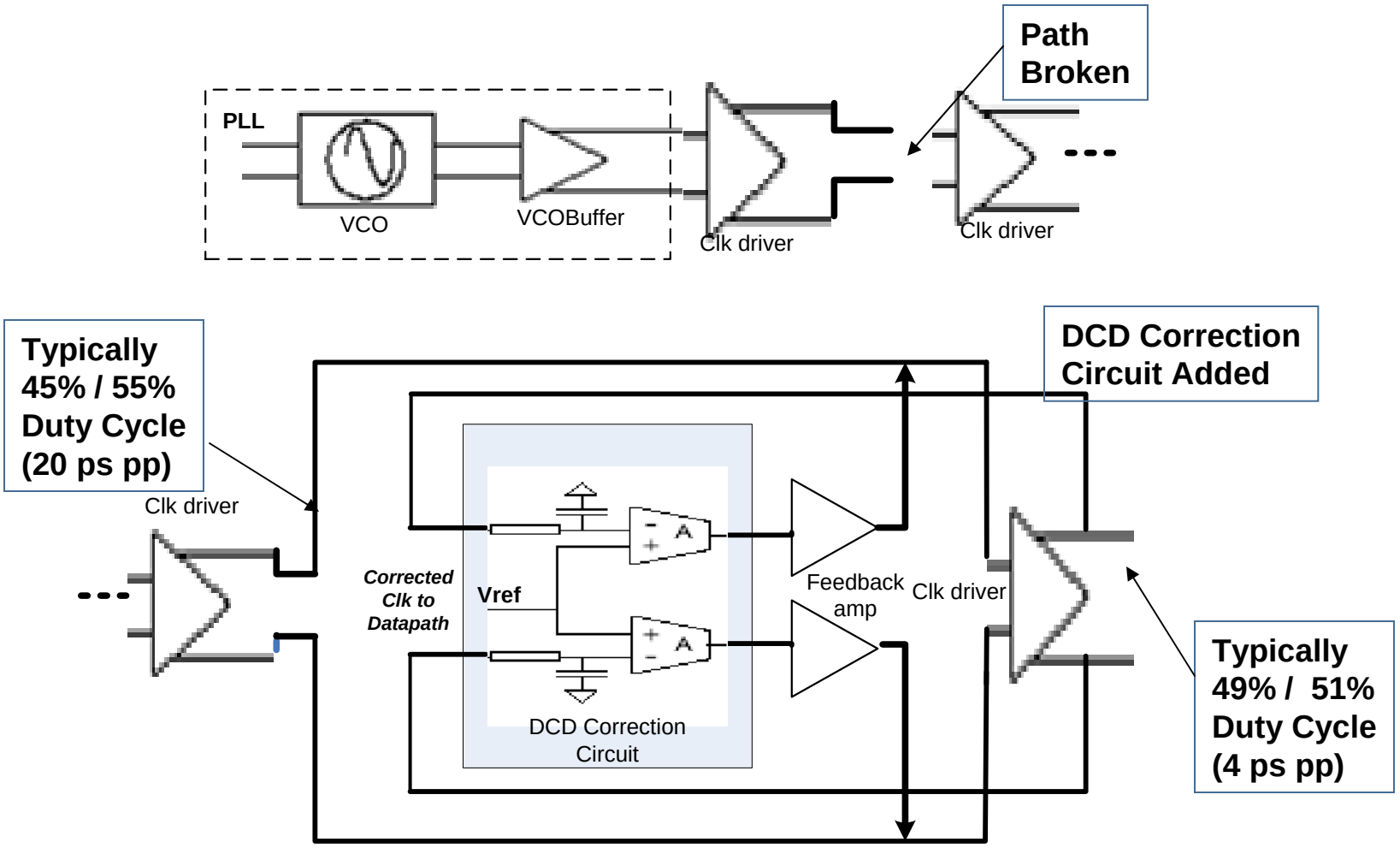
Problem

- DCD Significantly Affects Signaling Performance (see abler_01_0106)
  - Shows System Typically Fails with DCD = 6%
  - Given the PNA Effect, This Outcome Is Not Unexpected
- What to Do? Alternatives:
  - Provide For Existing Draft Channel Recommendations By Specifying Lower DCD
  - Require Better Channels and Keep Existing DCD or Increase DCD

Existing DCDs

- Our Current Draft Limits DCD to 5% = 0.05 UI pp
- OIF CEI Limits DCD to 5% = 0.05 UI pp

Controlling DCD –
DCD Correction Circuit



With Process and Temperature Variation, Corrected DCD Increases To > 4 ps pp

Observation

- One DCD Stage Gets Close To the Existing Spec
- Adding Another DCD Control Stage is Possible, But We Get Very Diminished Improvement After the First One
- Getting DCD to 5% Over Process and Temp Variation is Difficult

Conclusion, Recommendation

- Controlling DCD to 5% is Difficult
- Keep Existing Limit of 5%, Improve Channel Recommendations or EIT as Necessary

Background – DCD Definitions

- “5% DCD” – Used in Presentations
- 0.05UIpp – Used in Specs
- 97.5/102.5 – As % of Bit
- 48.75/51.25 – As % of Nyquist Period
- “1.25% DCD” – Another Common Definition