74.7.4.3 FEC transmission bit ordering

The format of the FEC block and the transmit bit ordering is shown in Figure 74–2.

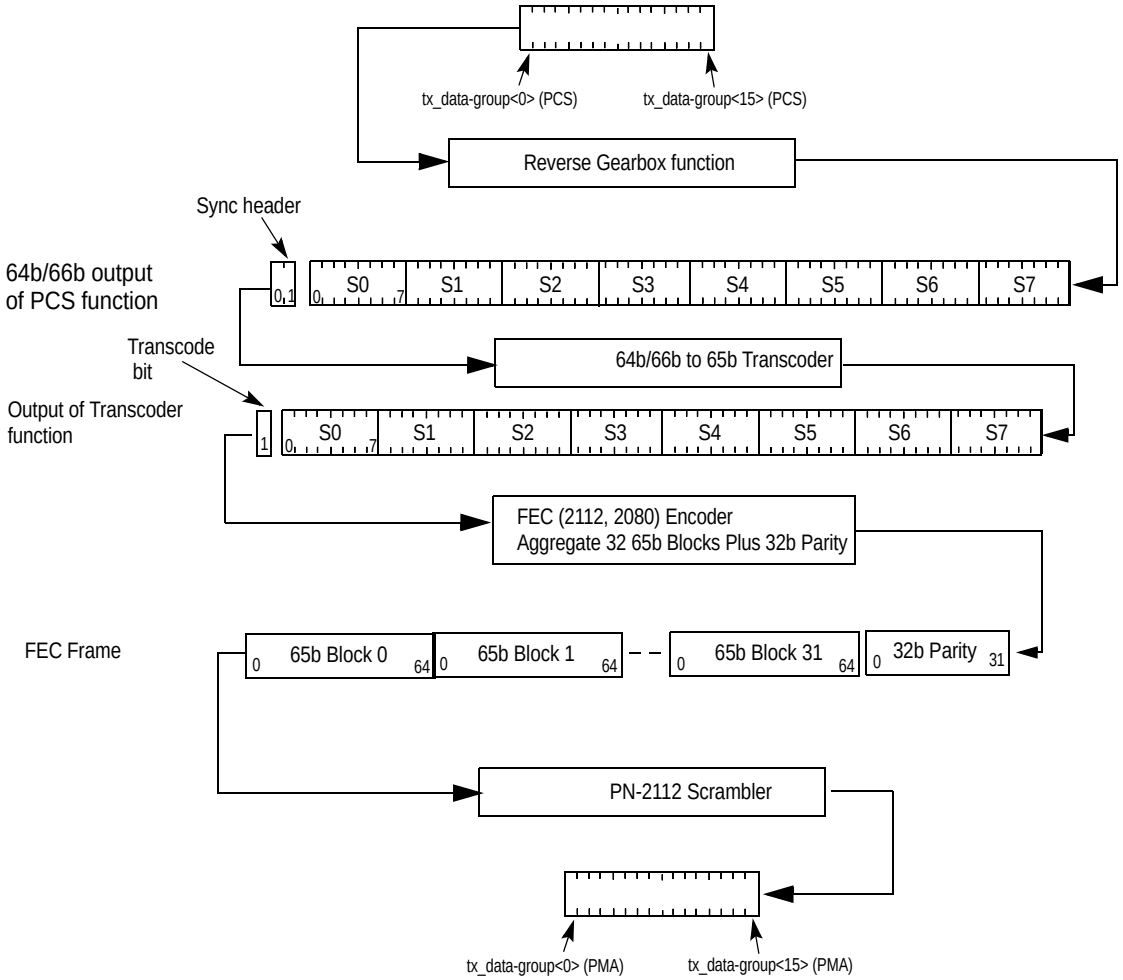

Figure 74–2—FEC Transmit bit ordering

74.7.4.4 FEC (2112,2080) encoder

The block diagram of the FEC Encoder is illustrated in Table 74–1. The 32 x 65 bit payload blocks are encoded by the (2112,2080) code. This code is a shortened cyclic code that can be encoded by generator polynomial *g(x)*. The resulting payload block including the T bits is scrambled using the PN-2112 pseudo-noise sequence as described in 74.7.4.4.1.

The generator polynomial *g(x)* for the (2112, 2080) parity-check bits is defined as given below.

(74–1)

$$g(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^{2} + 1$$

74.7.4.6 FEC receive bit ordering

The format of the FEC block and the receive bit ordering is shown in Figure 74–2.

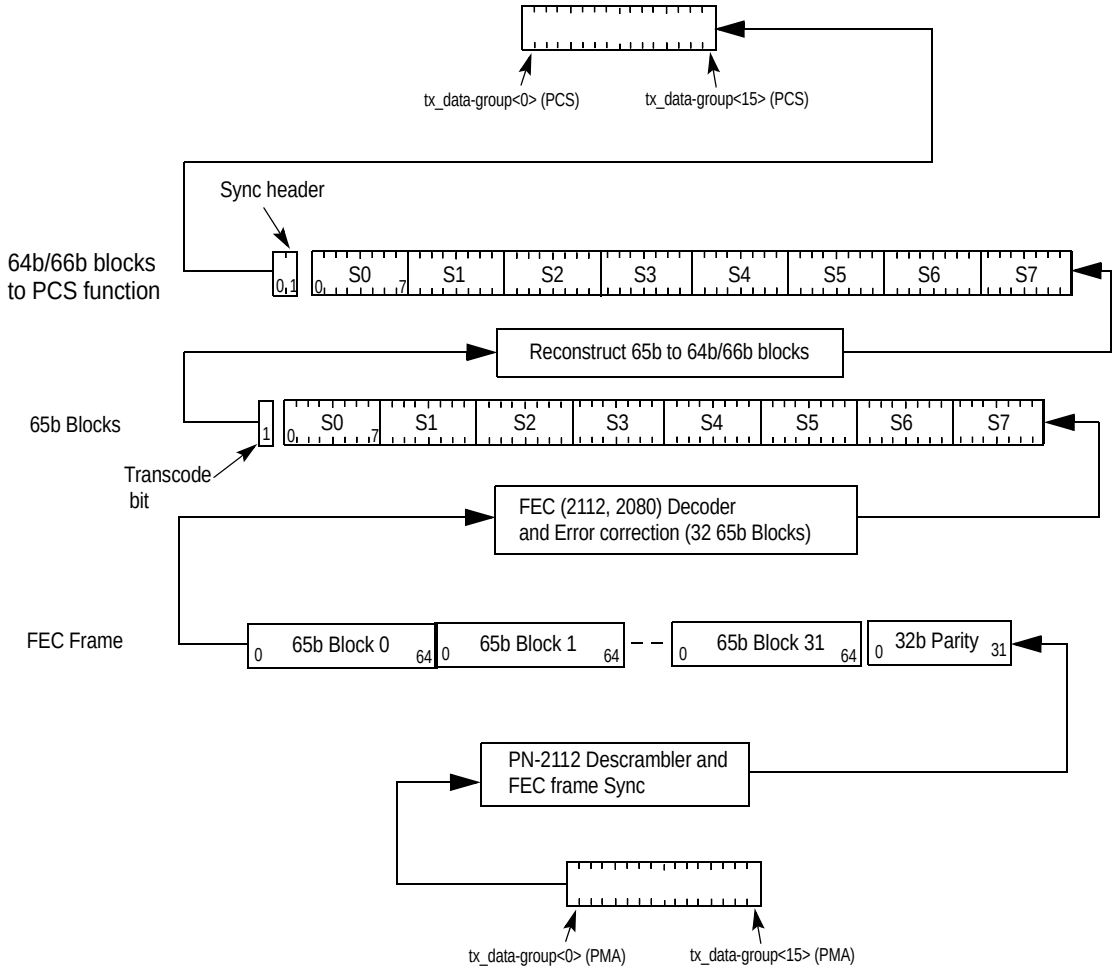

Figure 74–8—FEC Receive bit ordering

74.13.1 Detailed functions and state diagrams

74.13.1.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

74.13.1.2 State variables

74.13.1.2.1 Constants

m
: Positive integer constant set to value 8.

n
: Positive integer constant set to value 4.

74.13.1.2.2 Variables

fec_block_lock
: Boolean variable that is set true when receiver acquires FEC block delineation

reset
: Boolean variable that controls the resetting of the FEC sublayer. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on.

signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK) . It is true if the value was OK and false if the value was FAIL.

fec_signal_ok
: Boolean variable that is set based on the most recently received value of PMA_UNITDATA.indication(SIGNAL_OK) and fec_block_lock. It is set to true if the fec_bock_lock value is true and PMA_UNITDATA.indication(SIGNAL_OK) value was OK and set to false otherwise. The value is sent to the PCS layer through the primitive FEC_SIGNAL.indication as specified in 74.6.

slip_done
: Boolean variable that is asserted true when the SLIP requested by the FEC Block Lock State Machine has been completed indicating that the next candidate block sync position can be tested.

test_fec_frame
: Boolean variable that is set true when a new FEC frame is available for testing and false when TEST_FEC_FRAME state is entered. A new FEC frame is available for testing when the FEC Block Sync process has accumulated one FEC block from the candidate start position (fec_frame<2111:0>) from the PMA to evaluate the parity of the next block

fec_frame<2111:0>
: Vector containing 2112 bits of a new FEC frame accumulated from the candidate start position received from the PMA and descrambled using PN-2112 as specified in 74.7.4.4.1. For each frame processing the PN-2112 is returned to the initial state as described in 74.7.4.4.1

parity_good
: Boolean indication that is set true if the FEC_PARITY_CHECK function returns “match” and false if the FEC_PARITY_CHECK function returns any other value.

parity_correctable
: Boolean indication that is set true if the FEC_PARITY_CHECK function returns “correctable” and false if the FEC_PARITY_CHECK function returns any other value.

parity_uncorrectable
: Boolean indication that is set true if the FEC_PARITY_CHECK function returns “uncorrectable” and false if the FEC_PARITY_CHECK function returns any other value.

74.13.1.2.3 Functions

FEC_PARITY_CHECK(fec_frame<2111:0>)
: Computes parity based on the FEC generator polynomial *g(x)* on fec_frame<2079:0> and compares it against the received 32-bit parity bits fec_frame<2111:2080>. The FEC_PARIY_CHECK function returns “match” if the parity check matches; returns “correctable” if the computed parity does not match the received parity but the error is correctable; returns “uncorrectable” if the computed parity does not match and the error is uncorrectable.

SLIP
: Causes the next candidate FEC block sync position to be tested. The precise method for determining the next candidate block sync position is not specified and is implementation dependent. However, an implementation shall ensure that all possible bit positions are evaluated.

74.13.1.2.4 Counters

parity_good_cnt
: Count of the number times the computed parity of received message bits matched the received parity.

parity_invalid_cnt
: Count of the number of times the computed parity of received message bits did not match the received parity.

correctable_error
: Count of the number of times the computed parity of received message bits did not match the received parity and the error is correctable. The counter is incremented every time the FEC lock state machine transitions to CORRECTABLE_PARITY state

uncorrectable_error
: Count of the number of times the computed parity of received message bits did not match the received parity and the error is uncorrectable. The counter is incremented every time the FEC lock state machine transitions to INVALID_PARITY state

74.13.1.3 State diagrams

The FEC Lock state machine shown in Figure 74–10 determines when the PCS has obtained lock to the received data stream.

The FEC sublayer shall perform the functions of FEC Lock function as specified in these state machines.

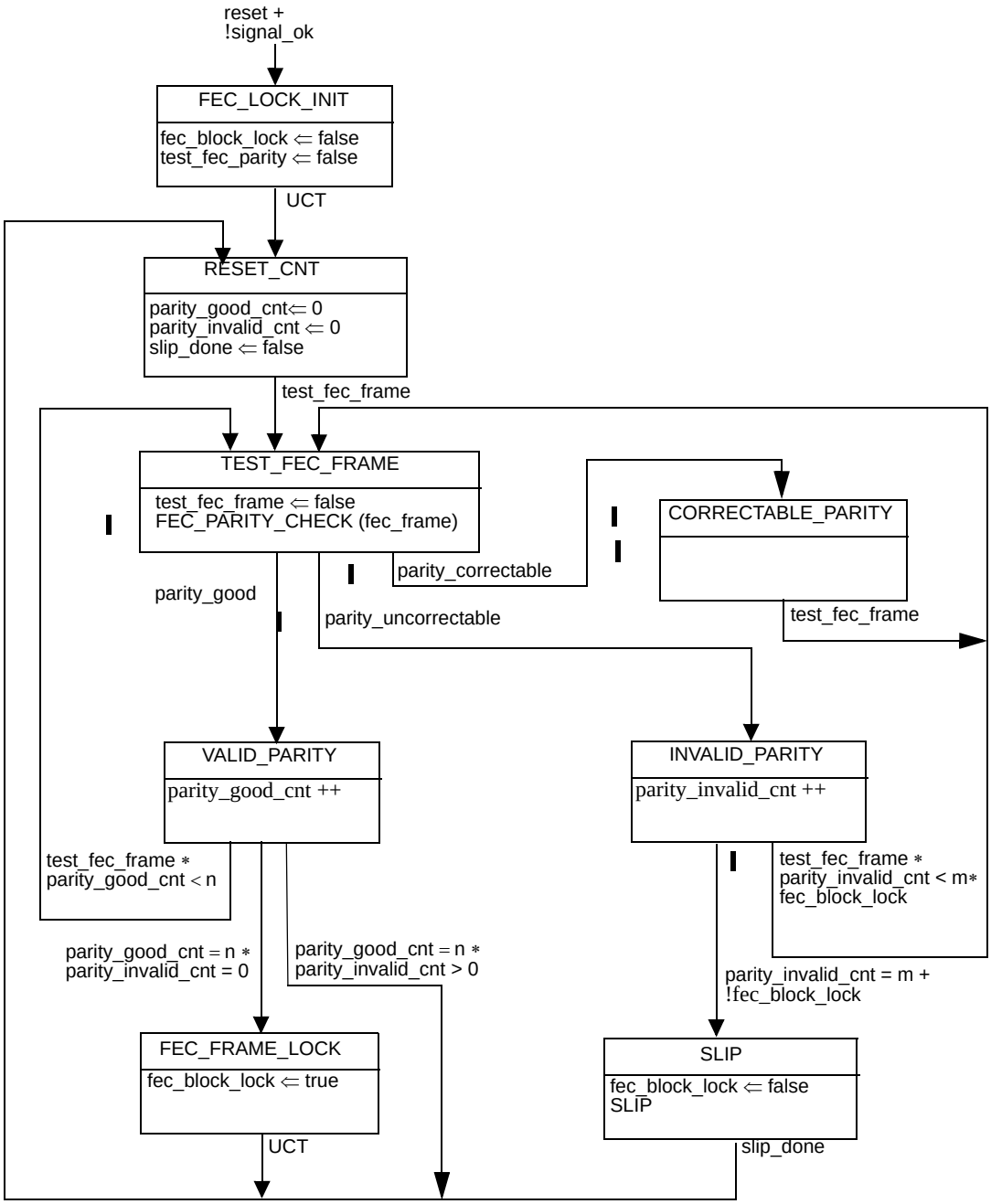

Figure 74–10—FEC Lock state machine