The Need For a Normative Channel Model Approach

### John D'Ambrosia, Tyco Electronics Joe Abler, IBM January 24, 2005



# Supporters

- Jimmy Sheffield, Tyco Electronics \*
- Andre Szczepanek, Texas Instruments
- Matt Hendrick, Intel \*
- Aniruddha Kundu, Intel \*
- Mike Altmann, Intel \*
- Fulvio Spagna, Intel \*
- Brian Von Herzen, Rapid Prototypes
- Cathy Liu, LSI Logic
- Anthony Sanders, Infineon \*
- Jeff Lynch, IBM
- Petre Popescu, Quake Technologies
- Charles Moore, Agilent
- Shannon Sawyer, Agilent
- Ted Rado, Analogix
- Mike Resso, Agilent

Note – This individual supports an end-to-end normative analysis tool. This support does not imply support for the NRZ signaling scheme used in the simulation of this presentation.



# **Review of Tyco Channels**

Test Case	Line Card		Backplane		Total	Commonto		
Test Case	Length	Material	Length	Material	Stub	Length	Comments	
1	10" (254mm)	Nelco 4000 13SI	20" (508mm)	Nelco 4000 13SI	Bottom (or counter- boring)	40" (1016mm)	Channel Model <i>Tyco – Data is available.</i>	
2	10" (254mm)	Nelco 4000 13	20" (508mm)	Nelco 4000 13SI	Bottom (or counter- boring)	40" (1016mm)	Margin Test Case <i>Tyco - Data is available.</i>	
3	10" (254mm)	Nelco 4000 6	20" (508mm)	Nelco 4000 13SI	Bottom (or counter- boring)	40" (1016mm)	Margin Test Case <i>Tyco - Data is available.</i>	
4	6" (152mm)	Nelco 4000 13	20" (508mm)	Nelco 4000 13SI	Bottom (or counter- boring)	32" (812mm)	ATCA Full Mesh <i>Tyco - Data is available.</i>	
5	6" (152mm)	Nelco 4000 13	10" (254mm)	Nelco 4000 13	Bottom (or counter- boring)	22" (558mm)	ATCA Dual Star Tyco - Data is available.	
6	6" (152mm)	Nelco 4000 13	10" (254mm)	Nelco 4000 13	Top Layer (with stub)	22" (558mm)	ATCA Dual Star <i>Tyco - Data is available.</i>	
7	6" (152mm)	Nelco 4000 13SI	1" (25mm)	Nelco 4000 13SI	Near Top- Layer (with stub)	13" (330mm)	Adjacent Slot <i>Tyco - Data is available.</i>	
NOTE: Data for all test cases includes dominant, adjacent NEXT and FEXT aggressors.								



# **Review of IBM Simulations**

- Channels with stubs were most difficult
- Device packaging had an impact
- Simulations done using 6G IC model (ESD Diodes and load termination)

#### Case 5 with Organic Package

Simulation Results* (opening at 10 <sup>-12</sup> BER)					
	FFE2	FFE3	FFE4		
DFE0	5.7%	9.5%	20.2%		
DFE1	9.8%	21.1%	9.8%		
DFE2	12.2%	17.4%	9.7%		
DFE3	16.0%	18.9%	15.4%		
DFE4	18.8%	23.1%	12.2%		
DFE5	21.3%	22.2%	10.4%		

#### **Case 5 with Plastic Package**

#### Simulation Results\* (opening at 10<sup>-12</sup> BER)

	FFE2	FFE3	FFE4
DFE0	e-6	e-7	11.2%
DFE1	9.7%	15.7%	17.1%
DFE2	9.7%	15.0%	17.1%
DFE3	14.6%	16.7%	15.2%
DFE4	16.5%	15.8%	20.9%
DFE5	20.8%	15.5%	21.1%

#### Case 6 with Organic Package

Simulation Results* (opening at 10 <sup>-12</sup> BER)					
FFE2 FFE3 FFE4					
DFE0	e-3	e-4	e-6		
DFE1	e-8	0%	e-11		
DFE2	e-8	0%	0%		
DFE3	e-8	0%	2.8%		
DFE4	e-9	4.6%	3.4%		
DFE5	e-11	5.5%	8.4%		

#### **Case 6 with Plastic Package**

#### Simulation Results\* (opening at 10<sup>-12</sup> BER)

	FFE2	FFE3	FFE4
DFE0	e-3	e-3	e-4
DFE1	e-7	0%	e-9
DFE2	e-8	0%	e-11
DFE3	e-8	4.1%	0.1%
DFE4	e-10	4.4%	0%
DFE5	0%	4.6%	3.9%

#### Case 7 with Organic Package

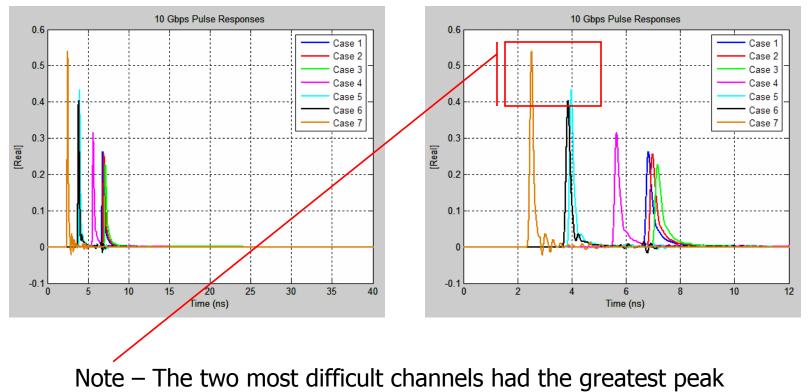
Simulation Results* (opening at 10 <sup>-12</sup> BER)						
	FFE2 FFE3 FFE4					
DFE0	e-5	e-5	e-6			
DFE1	e-9	0.1%	0%			
DFE2	e-11	4.6%	3.8%			
DFE3	0.1%	4.4%	4.8%			
DFE4	6.2%	6.2%	12.1%			
DFE5	10.9%	9.7%	9.7%			

#### **Case 7 with Plastic Package**

Simulation Results* (opening at 10 <sup>-12</sup> BER)						
	FFE2 FFE3 FFE4					
DFE0	e-4	e-4	e-5			
DFE1	e-11	e-9	0.4%			
DFE2	e-9	0.4%	5.4%			
DFE3	4.1%	1.7%	3.9%			
DFE4	1.5%	4.7%	5.8%			
DFE5	5.9%	3.8%	4.2%			



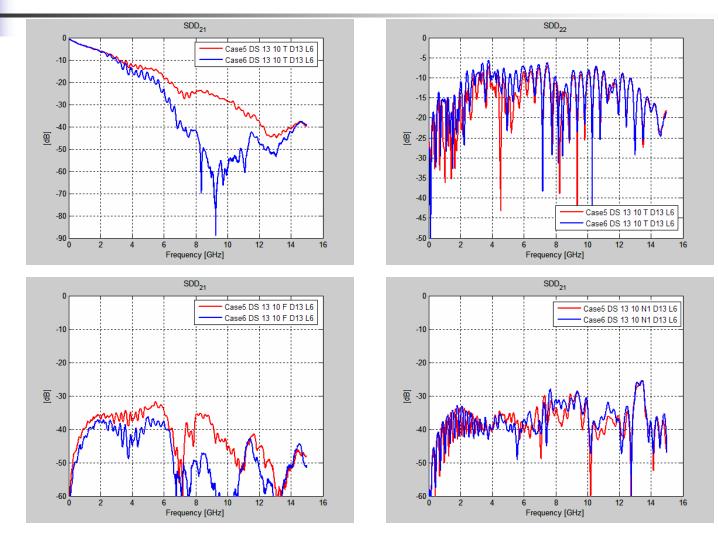
### Pulse Reponse of All Tyco Channels



Let's look at Cases #5 and #6

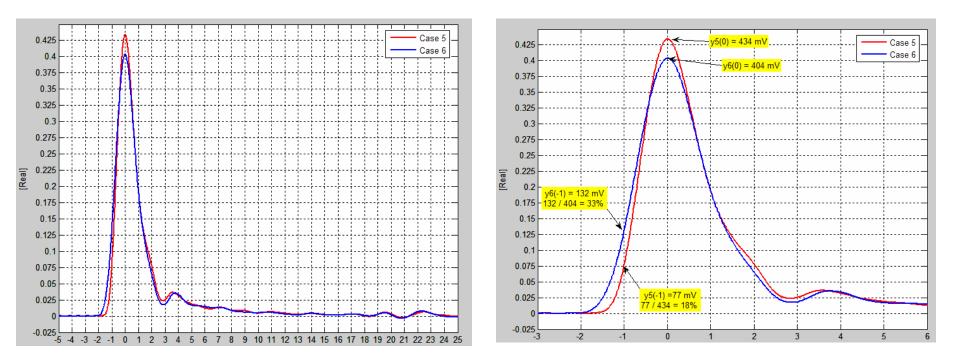


### Cases #5 and #6 Frequency Characterization





### Cases #5 and #6 TP1-4 Pulse Response



Case #6 vs Case #5

- 7% Reduction in peak (but still larger than other signals)
- 15% increase in t(-1) contribution
- Little different in tail

IEEE Vancouver Interim Meeting, January 2005

Electronics

TUCO

### Additional Simulations for Cases #5 and #6

	Case 5 FFE3/DFE3	Case 5 FFE3/DFE5	Case 6 FFE3/DFE3	Case 6 FFE3/DFE5
1. Original results	18.9%	22.2%	0% (BER floor at E-12)	5.5%
2. No Packaging	15.7%	17.1%	<0 (BER floor at E-8)	<0 (BER floor at E-11)
3. No Packaging, No IC	27.4%	27.0%	16.5%	19.9%
4. No Packaging, No IC, No Xtalk	32.9%	33.0%	20.8%	22.1%

Simulation 1 – Original simulations, as specified in abler\_01\_00904.pdf

Simulation 2 – As stated in Simulation #1, except packaging removed

Simulation 3 – As stated in Simulation #2, except IC Model (ESD and load structures) replaced with perfect  $50\Omega$  terminations.

Simulation 4 – As stated in Simulation #3, except all crosstalk removed



### Conclusions

- Case #5 vs Case #6 Frequency Behavior
  - SDD21 classic stub effect comparison
  - SDD22 very similar
  - NEXT higher for Case #5
  - FEXT similar
  - Pulse behavior similar except t(-1)
- Case #5 Simulations
  - No package decreased opening, suspect less attenuation of reflections
  - No IC model eliminates reflections, largest contributor to increasing eye opening
  - No xtalk approximate 6% improvement
- Case #6 Simulations
  - No package decreased opening, suspect less attenuation of reflections
  - No IC model eliminates reflections, largest contributor to increasing eye opening
  - No xtalk approximate 2% to 4% improvement
- Simulations were done using 6G IC model (ESD Diodes and load termination). Improved IC return loss should yield better results.



### Recommendations

- Throughput "typical" comparison point, but predicted perfomance is a system issue
- Reflections are driven by a number of factors
  - Tx Launched Signal
  - Channel (TP1 / TP4) throughput
  - Channel (TP1 / TP4) return loss
  - Device return loss
  - Package and IC (ESD / termination) effects
- A synergistic view point is necessary, so a normative end-to-end analysis tool is needed
- Future analysis will need to include effects of AC coupling cap.

