45. Management Data Input/Output (MDIO) Interface

Editor's notes: To be removed prior to final publication.

1. This clause contains all modifications to clause 45 required by the IEEE P802.3ap project. The text in this clause currently illustrates the new registers required to support AN over electrical backplanes (as referenced in Clause 73) and PMD-specific functions. These changes are written as an amendment to IEEE 802.3an. In some cases 802.3ap needs to change the text in 802.3am. Therefor all changes will proceed with an indication if it is a 802.3an or 802.3ap change. These changes need to be coordinated with changes from the IEEE P802.3an and IEEE P802.3aq projects.

3. Coordinate the combined registers with 802.3an. Place registers to flow sequentially based on 802.3REVam and any amendments to it.

45.2.1 PMA/PMD registers

This is an 802.3an Rev 2.3 change: Change and insert the following registers 1.147 through 1.32 767 in Table 45-3 with the following:

Table 45–3—PMA/PMD registers

Register address	Register name
1.147 through 1.~~32 767~~149	Reserved
1.150	10GBASE-KR PMD control
1.151	10GBASE-KR PMD status
1.152	10GBASE-KR LP coefficient update
1.153	10GBASE-KR LP status report
1.154	10GBASE-KR LD coefficient update
1.155	10GBASE-KR LD status report
1.156 through 1.~~157~~ 159	~~10GBASE-KR FEC corrected blocks counter~~ Reserved
~~1.158 through 1.159~~	~~10GBASE-KR FEC uncorrected blocks counter~~
1.160	1000BASE-KX control
1.161	1000BASE-KX status
1.162 through 1.169	Reserved
1.170	Clause 74 FEC capability
1.171	Clause 74 FEC control
1.172 through 1.173	Clause 74 FEC corrected blocks counter
1.174 through 1.175	Clause 74 FEC uncorrected blocks counter
1.~~162~~ 176through ~~1.32 768~~1.32 767	Reserved

Table 45–54—10GBASE-KR PMD control register

Bit(s)	Name	Description	R/W[1]
1.150.15:~~5~~ 2	Reserved	Value always zero, writes ignored	RO
~~1.150.4~~	~~Enable FEC Error Indication~~	~~A write of 1 to this bit configures FEC decoder to indicate Error to the upper layer~~	~~R/W~~
~~1.150.3~~	~~Enable FEC~~	~~A write of 1 to this bit enables FEC in the 10GBASE-KR PHY~~	~~R/W~~
~~1.150.2~~	~~FEC Capable~~	~~A read of 1 in this bit indicates that the 10GBASE-KR PHY is FEC capable~~	~~RO~~
1.150.1	Training enable	1 = Enable the 10GBASE-KR start-up protocol 0 = Disable the 10GBASE-KR start-up protocol	RO
1.150.0	Restart training	1 = Reset 10GBASE-KR start-up protocol 0 = Normal operation	R/W SC

[1]R/W = Read/Write, SC = self-clearing

45.2.1.76.1 Restart training (1.150.0)

This bit maps to the state variable mr_restart_training as defined in 72.6.10.3.2.

45.2.1.76.2 Training enable (1.150.1)

This bit maps the state variable mr_training_enable as defined in 72.6.10.3.2.

45.2.1.76.3 FEC Capable (1.150.2)

When read as a one, this bit indicates if the 10GBASE-KR PHY supports Forward Error Correction (FEC). When read as a zero, the 10GBASE-KR PHY does not support Forward Error Correction.

45.2.1.76.4 Enable FEC (1.150.1)

When written as a one, this bit enables the FEC for the 10GBASE-KR PHY. When written as a zero, FEC is disabled in the 10GBASE-KR PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.76.5 Enable FEC Error Indication (1.150.4)

This bit enables the FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-KR PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero the error indication function is disabled.

The assignment of bits in the 10GBASE-KR LD status report register is shown in Table 45–59.

Table 45–59—10GBASE-KR LD status report register bit definitions

Bit(s)	Name	Description	R/W[1]
1.155.15	Receiver ready	1 = The LD receiver has determined that training is complete and is prepared to receive data 0 = The LD receiver is requesting that training continue	R/W
1.155.14:6	Reserved	Value always 0, writes ignored	R/W
1.155.5:4	Coefficient (+1) status	5 4 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W
1.155.3:2	Coefficient (0) status	3 2 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W
1.155.1:0	Coefficient (–1) status	1 0 1 1 = maximum 1 0 = minimum 0 1 = updated 0 0 = not_updated	R/W

[1]R/W = Read/Write

45.2.1.81.1 Receiver ready (1.155.15)

The function and values for the receiver ready bit are defined in 72.6.10.2.4.1.

45.2.1.81.2 Coefficient (k) status (1.155.5:0)

The function and values for the coefficient status bits are defined in 72.6.10.2.4.2.

45.2.1.82 10GBASE-KR FEC corrected blocks counter (Register 1.157, 1.156)

The assignment of bits in the FEC corrected blocks counter register is shown in Table . See 74.10.1 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45-60 10GBASE-KR FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	RO[1]
1.156.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO
1.157.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO

[1]RO = Read Only

45.2.1.83 10GBASE-KR FEC uncorrected blocks counter (Register1.159, 1.158)

The assignment of bits in the FEC uncorrected blocks counter register is shown in Table. See 74.10.2 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45-61 10GBASE-KR FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	RO[1]
1.158.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO
1.159.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO

[1]RO = Read Only

45.2.1.82 1000BASE-KX control register (Register1.160)

Table 45–60—1000BASE-KX control register

Bit(s)	Name	Description	R/W[1]
1.160.15:1	Reserved	Value always zero, writes ignored	RO
1.160.0	PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

[1]RO = Read Only, R/W = Read/Write

45.2.1.82.1 PMD transmit disable (1.160.0)

This bit disables the 1000BASE-KX transmitter as defined in 70.6.5.

45.2.1.84 Clause 74 FEC registers

This is an 802.3-2005 change: Insert the following Clause 74 FEC registers information as 45.2.1.84 and shift other subclauses. Renumber tables to flow sequentially based on 802.3-2005 and any amendments to it.

The assignment of registers for Clause 74 FEC is provided in Table 45–62. .

Table 45–62—Clause 74 FEC registers

Register Address	Register name
1.170	Clause 74 FEC capability
1.171	Clause 74 FEC control
1.172, 1.173	Clause 74 FEC corrected blocks counter
1.174, 1.175	Clause 74 FEC uncorrected blocks counter

45.2.1.84.1 Clause 74 FEC capability register (Register 1.170)

The assignment of bits in the Clause 74 FEC capability register is shown in Table 45–63.

Table 45–63—Clause 74 FEC capability register bit definitions

Bit(s)	Name	Description	R/W[1]
1.170.15:1	Reserved	Value always zero, writes ignored	RO
1.170.0	10GBASE-KR FEC capable	A read of 1 in this bit indicates that the 10GBASE-KR PHY is FEC capable	RO

[1]R/W = Read/Write, RO Read Only, SC = self-clearing

45.2.1.84.1.1 10GBASE-KR FEC capable (1.170.0)

When read as a one, this bit indicates if the 10GBASE-KR PHY supports Clause 74 Forward Error Correction (FEC). When read as a zero, the 10GBASE-KR PHY does not support Forward Error Correction.

45.2.1.84.2 Clause 74 FEC control register (Register 1.171)

The assignment of bits in the Clause 74 FEC control register is shown in Table 45–64.

Table 45–64—Clause 74 FEC control register bit definitions

Bit(s)	Name	Description	R/W[1]
1.171.15:2	Reserved	Value always zero, writes ignored	RO
1.171.1	Enable FEC Error Indication	A write of 1 to this bit configures FEC decoder to indicate Error to the upper layer	R/W
1.171.0	Enable FEC	A write of 1 to this bit enables Clause 74 FEC A write of 0 to this bit disables Clause 74 FEC	R/W

[1]R/W = Read/Write, RO Read Only, SC = self-clearing

45.2.1.84.2.1 Enable FEC (1.171.0)

When written as a one, this bit enables Clause 74 FEC for the 10GBASE-R PHY. When written as a zero, FEC is disabled in the 10GBASE-R PHY. This bit shall be set to zero upon execution of PHY reset.

45.2.1.84.2.2 Enable FEC Error Indication (1.171.1)

This bit enables the Clause 74 FEC decoder to indicate decoding errors to the upper layers (PCS) through the sync bits for the 10GBASE-R PHY in the Local Device. When written as a one, this bit enables indication of decoding errors through the sync bits to the PCS layer. When written as zero the error indication function is disabled.

45.2.1.84.3 Clause 74 FEC corrected blocks counter (Register 1.172, 1.173)

The assignment of bits in the Clause 74 FEC corrected blocks counter register is shown in Table 45–65. See 74.10.1 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the management function or upon PHY reset. These bits shall be held at all ones in the case of overflow.

Table 45–65—Clause 74 FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[1]
1.172.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, NR
1.173.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, NR

[1]RO = Read Only, NR = Non Roll-over

45.2.1.84.4 Clause 74 FEC uncorrected blocks counter (Register1.174, 1.175)

The assignment of bits in the Clause 74 FEC uncorrected blocks counter register is shown in Table 45–66. See 74.10.2 for a definition of this register. These bits shall be reset to all zeroes when the register is read by the managem

Table 45–66—Clause 74 FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W[1]
1.174.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, NR
1.175.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, NR

[1]RO = Read Only, NR = Non Roll-over