IEEE 802.3ap
Power & Complexity Discussion Guidelines

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Issue

- Forward looking standards developments need to make projections for power and complexity
- Need metrics to enable finding an optimal standard solution
- Current reporting lacks consistency in details
- Tendency is to create high-level metrics, but detailed comparisons become difficult

Proposal

- Adopt a standard list of considerations for BP Ethernet power & complexity reporting
- Presentations WRT line coding & equalization should divide power & complexity comparisons into subsections
  - Transmitter
    - Tx serializer and line coder
    - Tx equalization / pre-emphasis block
    - Driver
      - Peak vs. RMS output voltage (or launch power)
      - Topological constraints (ex. bridge vs. CML-style launch)
      - Driver V_{DD} requirements
  - Receiver
    - Equalizer
      - Longer and more complex equalization structures requires significant fraction of total power
      - Express relative power using industry-accepted structures (linear FFE and sampled DFE)
    - CDR complexity/power
  - Core
    - Synthesizer PLL for clock generation
    - Data coding for dispersion, error correction & detection, management
    - Expressed as gate count or comparative digital complexity
- Totalized power must include <u>all</u> power from <u>all</u> PHY/SerDes functions

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