Unconfirmed Minutes
IEEE P802.3AP - Backplane Ethernet
July 13- 15th, 2004
Portland, OR

Prepared by: John D'Ambrosia

Meeting convened at 8:34 am, July 13, 2004.

Agenda / Housekeeping Issues

- Introductions
- Agenda
  - Motion to adopt – John D'Ambrosia
    - Second - Tom Palkert
  - Approved by voice vote without objection
- Motion to approve minutes from May meeting that are posted on web
  - No corrections requested
  - Moved by – Charles Moore
  - Second – Joel Goergen
  - Minutes were accepted by voice vote without objection
- Goals for meeting discussed
  - Development of Draft 1.0
  - Presentations
  - Backplane Channel Model
  - Candidate architectures for 10 Gb/s Serial PHY and Auto-negotiation
- IEEE rules read to the body by Chair
- IEEE Patent policy read to the body by Chair
- Project Flow Discussed
- Project Details
  - Approved PAR - http://standards.ieee.org/board/nes/projects/802-3ap.pdf
  - 5 Criteria - http://ieee802.org/3/ap/802_3_ap_5criteria.pdf
  - Objectives - http://ieee802.org/3/ap/802_3_ap_objectives.pdf
- Review of Project Objectives
  - Discussion of motion from May – "Define a 4-lane 10 Gb/s PHY for operation over the 802.3ap channel model."
    - Intent of motion was a 4-lane interface with an aggregate 10 Gb/s, not 40 Gb/s.
    - This motion, however conflicts with "Distinct Identity" response that calls out that "at most one PHY for 1 Gb/s operation and at most one PHY for 10 Gb/s operation."
- Project schedule discussed
  - See agenda_1_0704 for Project Timeline
    - "Last new proposal" refers to radical new concepts, not refinements / extensions to existing proposals
    - Motion to adopt schedule – approved by voice vote without objection

- Chair requested
    - All questions on presentation be held to end
    - All questions relevant to content and clarification of content

Presentation #1

Title – "System Vendor Requirements for 10 Gb/s Backplane"
By – Mary Mandich, Lucent Technologies
See – mandich_01_0704.pdf

Discussion

- Power target 1.2X 2.5G per Tx/Rx pair (two pairs = 1 lane per previously agreed convention).
- Focus on reach does not need to change, but since developing only 1 PHY but could be challenging if trying to support "legacy" backplanes
- No input regarding legacy backplanes in relation to proposed channel model.
- Maximum latency tolerance will be application specific.
    - In telecom specified at system level. Was estimated by Lucent down to the link level, but Mary could not recall numbers at time.
- Auto-negotiation –
    - System will set it up
    - Probably won't need auto-negotiation
        - but a nice feature
        - could add complexity and overhead
- Cards could either be for closed systems (vendor owns both plug-in cards) or open system (cards that can be plugged into the backplane can come from any line card vendor).

Presentation #2

Title – "Backplane Channel Ad Hoc Recommendations"
By – Joel Goergen, Force10 Networks
See Goergen_03_0704.pdf

Discussion

- Test time – Joel – 5minutes, but others have informed Joel of 11 minutes test time.
    - Contributors –
        - IF BW
        - Averaging – Graeme / Petre provided input that 16 is the minimum number, and could require raising on some measurements for desired accuracy
        - Step size
- Packaging effects are outside the defined physical channel model, and won't affect proposed masks. The effects are for refinement of the overall system problem.
- Crosstalk masks are for "multiple disturber"
- Group delay variation – calculate the mean of the group delay measurement, and then subtract measurement at each frequency from mean
- Group delay measurement aperture –

- Has been discussed, but not resolved
- What the equipment provides for a group delay measurement needs to be resolved

Presentation #3

Title – "FR-4 Definition III"
By – Joel Goergen, Force10 Networks
See Goergen_01_0704.pdf

Discussion

- Backplane stack up definition needs to be done carefully. "Average" Dk / Df values are not sufficient. High-end "improved FR-4" materials can be made to fail, and low-end "improved FR-4" materials can be made to pass.
- Temperature range should be modified from 55C to 70C.

Break 10:30
Reconvened at 10:45

Presentation #4

Title – "Channel Compliance to Proposed: Test Cards"
By – Joel Goergen, Force10 Networks
See goergen_02_0704.pdf

Discussion

- SMA issue
  - Low impedance discontinuity
  - Representative of BGA package?
  - Do we tune for impedance or for accurate representation?
- Should shape of lower frequency range (0-1 GHz) portion of the model.
  - Concern expressed at impact of opening up materials to allow for more loss in lower frequencies.
- Barrel to trace coupling covered
- Barrel to barrel via coupling will be in next round
- What is separation between single aggressor and mask for NEXT / FEXT?
  - Potential for tolerancing of xtalk in relation to mask.

Presentation #5

Title – Specifying a Channel Through Impulse Response
By – Charles Moore, Agilent Technologies
See moore_01_0704.pdf

Discussion

- Probability of worst case pattern will be related to interference width as well as distribution of majority of interference in the overall interference width
- How does one get an accurate pulse response? S-Parameter measurement techniques are known.
- To get to impulse response, go through s-parameter measurement phase and do inverse FFT.
- Have to worry about 50 MHz to dc interpolation scheme
- Charles opinion is that this might be more useful for informative model. Joel requested that this be looked at as more of a step to a normative model.
- Ali – use impulse response from chip
- Charles is not prepared to use this technique to get to a specification using actual models.

Lunch break @ 12:10 pm
Reconvened at 1:15pm

Presentation #6

Title – Advanced TCA Channel Data and Comparisons to Proposed Channel Model
By – William Peters, Intel
See peters_01_0704.pdf

Discussion

- System designed by Intel
- Was designed to support XAUI / Fibre Channel (3.2 Gb/s) with room for upper upgrade
- Need to clarify how much stub was on the line card, as it was pointed out that layer connection on the daughter card can be an issue
- Stub is a dominant impact on failure of SDD21.
    - Daughtercard stub may also be contributing.
    - Previous presentations showed counterboring is not a significant cost adder, but customer acceptance issue. Also, can't counterbore existing backplanes in field, but can counterbore existing designs that are in manufacturing queue.
- Use of better materials on line cards could help improve SDD21, but could cause further SDD11 / SDD22, NEXT, and FEXT issues.
- Strategy for addressing backplanes – data of interesting legacy backplanes in comparison to the channel model to further adjust and refine the channel model.

Presentation #7

Title – S-Params for IEEE Channel Ad Hoc
By – Stephen Anderson, Xilinx
See Anderson_01_0704.pdf

Discussion

- Non-causal / precursor response – not necessarily real
- S4P files need to be checked for confirmation to channel adhoc
- Modeling to the limits for return loss could be an issue
    - SDD11 model does not represent real return loss data

Presentation #8

Title – Further Channel Model Data
By – Brian Seemann, Xilinx
See seaman_01_0704.pdf

Discussion

- File was modified after update period with significant changes. Chair limited presentation to slides that were submitted by deadline. Final presentation was not permitted to be shown or will be uploaded. Requests for presentation should be forwarded to Brian Seemann directly.
- Test pattern was a short pattern, 2^7 PRBS for DC Balance reasons.
- Channel seen by device will be different than characterization data presented, i.e. cabling and extra length on device EVM.
- Continuous time filter used
- Presenter thought Tx launch voltage used was 800 mV

Presentation #9

Title – A Migration Path from 6.25 Gb/s Operation to 10 Gb/s Operation
By – Dave McCallum, Molex
See mccallum_01_0704.pdf

Discussion

- Extrapolation for BER was done to 10Gb/s
- Data on Df was pulled for single point for comparison, and does not include variability.
- Length was 1m from Tx to Rx, and is showing that lower frequency range of the channel violates the model
- Extrapolation of phase information needs to be reviewed.
- Crosstalk measurement
    - Parallel traces on the backplane
    - Multi-aggressor
    - Adjacent through the connector.
- Real measurements were done @ 6.25 Gb/s.
- Extrapolated to 10 Gb/s using same chip technique.

Break – 2:40 pm
Reconvened at 3:10pm

Presentation #10

Title – Compatibility Negotiation Considerations
By – Yong Kim, Broadcom
See kim_01_0704.pdf

Discussion

- Other methods looked at
    - Fibre Channel
    - PCI Express
- If an optical transceiver were driving directly across a backplane clause 37 would be friendly
- MAC doesn't determine the PMD, the PHY does the negotiation and is controlled by the MDIO registers
- In an Ethernet switch, it may be all in the same switch
- If Clause 37 is used as the basis, an electrical interface may have to be developed since would require some communications with the PCS
- If Clause 37, Yong felt the best way would be to keep it above the PCS layer
- Why exchange data below slowest speed (1G) that needs to be negotiated?
- If you do 8b/10b doesn't make sense to do below PCS
- Need to do where coding function is
- As long as it is 8B/10B PCS makes sense, but if not 8B/10B then this would be an issue
- Clause 37 would establish baseline BER for channel, which Clause 28 doesn't
- If 8B / 10B is not done, then Clause 28 would allow freedom on modulation scheme
- Incremental speed increase as part of auto-negoation, it could be attractive
- Difficulty in implementing clause
    - Early implementation issues
- Trying different speeds can be complex to implement and needs to be fully exercised
- All the techniques will have their own types of complexity

Presentation #11

Title – SerDes Compatible FLP AN Proposal
By – Andre Szczenpanek, Texas Instruments
See szczenpanek_01_0704.pdf , szczenpanek_02_0704.pdf

Discussion

- The PCS layer is in synch to operate, would require modification to Clause 37, as Clause 37 runs at one rate.
- Clause 37 would have to be extended to enable arbitration to deal with devices that run at different rates
- Andre was trying to move it outside the PCS for future proofing
- Numbers for cap on DC balance is similar to CX4
- CX4 numbers were picked for CX4
- Get the energy across, don't try to determine different data patterns for different speeds
- DC balance and size of capacitor could have an impact on the channel
- May have same limitation as Clause 28, since link may not provide adequate channel to pass signal
- Links in field would not be able to use technique, so then would have to fall back to current parallel scheme, so why define something new anyway.
- Joe Abler felt use of SD in backplanes going away due to new techniques , but Andre indicated that he is seeing the opposite, and putting SD back in to devices. Based on PCS lock wasn't proving adequate, requiring putting SD back in. Joe said this was a 3G space item, but Andre said they are seeing in 3 and 6.
- Clause 37 channel testing is only partial unless another phase is added.

Presentation #12

Title – SerDes Compatible Auto Negotiation for Backplane Ethernet
By – Ali Ghiasi, Broadcom
See Ghiasi_01_0704.pdf

Discussion

- As Clause 37 exists today, a device would need to operate at 1G
- In the future there may be presentations on how to do Clause 37 at different rates
- Mary Mandich indicated from a vendor perspective that they don't want an idle state
- Pat Thaler replied that just because one vendor doesn't want it, doesn't mean that is true for all applications
- Ali – the protocol is backwards compatible
- Period of time to negotiate might cause large time to auto-negotiate due to number of PHY's there are.
- Clause 28 is "most proven" (but it does need modification) because it is most implemented

Presentation #13

Title – 802.ap Auto-Negotiation with Clause 28 State Machines
By – Ilango Ganga, Intel

See ganga_01_0704.pdf

Discussion

- Yong Kim said there was difficulty industry wide every time a new PHY was implemented
- Use of selector field vs. new base page: subjective view of what would minimize industry confusion
- Yong supported use of Clause 45
- Eric Lynskey –
    - whatever direction the group chooses, interoperability will be an initial issue that will be worked through
    - Some form of Clause 28 below the PMD would be the best course of action
- Mary Mandich - Why put something into the SerDes that may impact power
- Pat Thaler – different view points from interaction with SAN, Datacom, Telecom customers
    - Service issue associated with how quick the light comes on
    - System boot time issue – add up all the things that happened, and it can become a significant issue to some customers
- Defining how to auto negotiate with legacy devices is an issue
    - Receive parallel detection
        - Fatal flaw with Clause 37 no parallel detection if auto-negotation is "on" one side and "off" the other. The side with "off" shows "link."
            - Everyone has to agree to develop 1G PHY
- You could auto-negotiate, but still not know details regarding the other link
- Is this a management issue or because different vendors build different parts of the system do we need to test the channel to make sure it can support the speed that has been negotiated.
- What happens if you have 4x next to 1x
- Look at system issues, and ignoring 1G for blade server market will be a serious issue.
- Why does using Clause 28 change the SerDes – putting logic there that is currently not there. This was debated.
    - Circuitry can be added above
    - No Signal Detect circuitry needed at PHY
- No auto-negotiation for backplanes currently exists.
- PCS is where auto-negotiation is performed, but it is not part of MAC and not part of SerDes
- Pat Thaler
    - With envelope detect parallel detect is simplified
    - Do it where it works
        - Higher – closer to intelligence
        - Lower – more flexibility in relation to coding
    - Stick to existing state machines as much as possible for higher chance of success for interoperability
- Bob Grow
    - Neither proposal will protect against bad design
    - Auto-negotiation is not link verification. Clause 28 or 37 will both run to completion across crappy channels

- Focus should be on exchange of information to bring up a well designed system
- If you care about the channel you need to do something else for link tolerance

Meeting adjourned for day 6pm

Wednesday, July 13, 2004
Meeting reconvened 8:33am

Agenda –

Motion to move Mike Altmann's presentation to after the 10:05 break
Approved by voice vote without objection.

Presentation #14

Title – New Base Page / Selector Field Proposal
By – Yong Kim, Broadcom
See kim_02_0704.pdf

Presentation #15

Title – Receiver Testing Using Interference Tolerance Measurements
By – Charles Moore, Agilent Technologies
See moore_02_0704.pdf

Discussion

- What sinusoidal frequency was used – something close to Nyquist Frequency. For example for 10 Gb/s NRZ, the sine wave would be close to 5 GHz.
- How does this compare with jitter tolerance test specified in XAUI
  - Different
  - Charles believes problem is xtalk, and this is right approach for that environment
- Concern that use of sine wave stress is symmetrical
- Stresses in vertical direction, which believes is symmetrical and the real limitation
- Charles believes technique is coding agnostic
- Charles prefers use of sine waves because characteristics are known and predictable
- Single frequency testing vs. frequency sweep
  - Length of time for testing?
  - Extra testing in addition to jitter testing?

Presentation #16

Title – Thoughts on testing of devices with 10^-15 confidence using test times historically used for 10^-12
By – Tom Waschura, SyntheSys Research

See waschura_01_0704.pdf

Discussion

- Any issues with noise on clock source? None seen. Measuring femto-second time-steps can be an issue under environmental conditions
- Group needs more presentations from test equipment vendors
- Need to have calibrated Tx to get the sort of enclosure you expect to see.
- Need to see stressing eye of Rx at device not just equipment, but Tom suggested looking at the eye going into the Rx, so it is essentially calibrated going in.
- Time domain measurements will have limitations due to implementation in Rx decision circuit

Presentation #17

Title – Power & Complexity Discussion Guidelines
By – Mike Altmann, Intel
See altmann_01_0704

Discussion

- Power assessments need to converge with system requirements
- Mike sees this as a way to compare competing solutions
- Joe Abler supported, and wanted to have an agreed upon matrix by everyone
- Joe was concerned with going to too small a block as that may not be useful in the end
- Implementation can affect architecture which might impact the usefulness of an agreed upon power matrix
- Charles suggested defining what must be included in the power analysis as opposed to a detailed breakdown
- Could make sense to do analysis on a block basis, as some functions can be shared, which would impact how the power would be reported
- Joe Abler meant that the matrix summarize what needs to be included, and total numbers shared down, but not broken down per characteristics in matrix
- Rob Brink supported Joe Abler's position
- Mike Altmann asked how to bring about a document to detail such a matrix
- Subsequent conversation this week or conference call to discuss: 1) the merits of such an approach; and 2) the actual items in the matrix, will occur

Presentation #18

Title – Signaling Analysis Using IEEE Channel Ad Hoc Templates
By – Stephen Anderson, Xilinx
See Anderson_02_0704.pdf

Discussion

- It was not known whether reflections from channel / device return losses occurred during the time that the DFE could deal with them
- Amplitude of the first tap in relation to the amplitude of the sample point
    - Meet harmonic (tap weight of DFE) for error propagation?
    - Steve has to check

Presentation #19

Title – PAM-4 versus NRZ Signaling: Basic Theory
By – Joe Abler, IBM
See abler_01_0704.pdf

Discussion

- Joel Goergen – In anticipation that the next step for Ethernet will be 100 Gb/s, and start-up companies are showing that NRZ won't work- why not switch today?
    - Joe Abler response is that not sure that PAM-4 will do 25 Gb/s
    - Joe says they have SERDES running in the lab at 25 Gb/s, but not across the channel being proposed.
- Rob Brink –
    - Has experience that is directly contradictory to Joe's statement that NRZ is outperforming PAM-4, where PAM-4 is working where NRZ isn't.
    - Analysis did not include xtalk, which is a real issue for backplanes. NRZ will have more xtalk since working at higher frequencies.
    - Joe admitted that they have seen this in certain cases, but not in all, as they have seen
- Jeff Sinksy's questions to Joe Abler.
    - Was phase included – expectation is yes.
    - Can you design a high density ASIC with lots of lines where each line is using 20 taps? Not proposed implementations or that they are needed.
    - Is this a mathematical exercise? Was done to eliminate implementation issues.
    - What do you do when there is a negative SNR?
    - Was Pre-emphasis used? Yes
    - Will a follow-on model address what a lesser number of taps can be done? Yes. Expectation is 5 tap DFE will suffice. Can be implemented into a large ASIC.
- In the simulations CDR was running.
- Bill Peters – Have you looked at any nulls in the 5 – 7 GHz region. Answer: Yes. Dealing with suckouts, becomes too wide or too deep is a situation that varies. Location of null in relation to modulation frequency spectrum will have an impact on the difference that nulls will have.

- Mike Altmann – Presentation shows that use of enough equalization to get rid of the loss of the channel. Not surprising. Similar results in a noise free environment from any scheme would be expected when not constraining amount of equalization.
    - Joe Abler –
        - presentation is a theoretical treatment of the comparison between PAM-4 and NRZ.
        - Rely on the DFE and less on the FFE. More on the FFE would exasperate the xtalk.
- Ali Ghiasi – how will process issues affect choice, since 90 um and 65 um
    - Joe Abler
        - Dropping voltages are being seen, but PAM-4 is staying at 1.8V
        - Will you be able to run PAM-4 at lower voltages? SNR keeps going down and causes integration issue.
        - At 3Gb/s Joe seeing more problems with amplitude closure.
    - Don't let future requirements that are not known should influence this work.
- Brian Seemann – stay to channels that are related to the channel model
- Use a low pass filter to reduce noise,
- John D'Ambrosia – Is Joe prepared to discuss additional techniques that might be used. Yes, but need channel model defined so that the need for these techniques can be analyzed.
- Majid – Complexity of a PAM-4 DFE – Joe's team has looked at it, but not familiar with the analysis. Joe feels both that PAM-4 and DFE are complex, and combining them together will be even more complex.
- Mary Mandich
    - Concerned that the solution is shifting the problem over to the system vendors
    - Joe Abler
        - DFE adaptation is in receiver only, and not affecting other pairs, so there isn't a system level ripple affect.
        - This is an advantage of DFE
    - Mary – then the system vendor needs to exercise it over the full range of adaptation.

Lunch Break at 12:08 pm
Reconvened at 1:20pm

Presentation #20

Title – A Comparison of NRZ and PAM-4 Using the IEEE Channel Model
By – Cathy Liu, LSI Logic
See liu_01_0704.pdf

Discussion

- Joel Goergen – since PAM-4 and NRZ appear similar, should we consider using PAM-4 for future. Use error control coding and FEC.
- Adam Healey – the pulse response indicates a lot of pre-emphasis being used, which Cathy confirmed. Comment on the swing –
    - Same degree of emphasis was used on crosstalk
- Rob Brink – Why are the XBASE-T using PAM if NRZ can be better.
    - Cathy not familiar with that project
    - Adam / Majid – not same channel or application
- Mike Altmann – the Tx filter being applied is included in the pulse response
    - With just that filter on, how much did it close both the NRZ and PAM-4 eyes?
        - Cathy didn't know
    - Is the improvement being seen by the larger impact of increased number of taps for NRZ (# taps > 10) caused by the filter on the Tx
        - Cathy has check this.
    - Per Mike - Scaling of the filter has more of an impact on the PAM-4 eye, and in reality you wouldn't do this, you would give the Tx the bandwidth it needs

Presentation #21

Title – A Study of NRZ Signaling over Proposed IEEE Ethernet Backplane
By – Nirmal Warke , Texas Instruments
See warke_01_0704.pdf

Discussion

- Jitter distributed assumed for the Tx/Rx and for that distribution the BER plotted

Presentation #22

Title – Edge-Equalized NRZ
By – Brian Brunn, Xilinx
See brunn_01_0704.pdf

Discussion

- RX eye (Page 9) with same Tx swing and no gain in Rx
- Pattern is 2^7 PRBS

Break at 2:45
Reconvened at 3:00

Presentation #23

Title – Comparison of PAM-4 and NRZ signaling based on measurements from a dual-mode device
By – Robert Brink, Agere Systems
See brink_01_0704.pdf

Discussion

- Brian Von Herzen – would edge equalization help. Rob- the part has Quadrature equalization, but that was not investigated.
- Joe Abler –
    - not a fair comparison since only Tx equalization was used.
    - define how the power was reported – (Rob: Power as reported for the device)
- Cathy Liu
    - Which eye was used – margin curves shown . The effect of all eyes taken into consideration.
- Charles Moore – why did the eye drop off so deeply. Not known.
- Majid – was pre-emphasis fixed? No – device equalized by itself to the best of ability.
- Brian Seemann – Why is the NRZ peaks at top of eyes not as crisp? Device self-optimized to the best of its ability.
- Justin Gaither – why wasn't periodic jitter scaled on UI basis? Testing was done to represent a single periodic jitter source on both. Same in terms of ps.
- Can update presentation to include SDD11.

Presentation #24

Title – Proposal for 10Gb/s single-lane PHY based on PAM-4 signaling
By – Robert Brink, Agere Systems
See brink_02_0704.pdf

Discussion

- Brian Seemann – xtalk of channel exceeds mask at 5G. Crosstalk from same channel was used.
- 100mW per pair for XAUI x 4 was used for power comparison
- Joe Abler – What p-p jitter should be used for proposal? Much discussion, since presentation showed 0.05, 0.1, and 0.15. Nothing was being proposed, but eye was opened both vertically and horizontally
- Mary Mandich –
    - training time? – wasn't known
    - Training at 5G and equalization scheme need to work with auto-negotiation scheme
- Mike Altmann –
    - if all equalization was in Rx how much faster would be adaptation time?
    - timing diagram would be needed
    - startup - there may be some system vendors with hard requirements.

Presentation #25

Title – Proposal for 10Gb/s single-lane PHY based on PAM-4 signaling
By – Jeff Sinsky, Lucent Technologies
See sinsky_01_0704.pdf

Discussion

- Mike Altmann –
    - why duo-binary instead of modified duobinary – Jeff - modified duobinary has less spectrum at DC. Not taking advantage of the backplane shape. Can force a more complex filter in the Tx. However, there may be other things to consider.
    - would you gain anything by putting delay and add filter back in Tx to compress launch spectrum. Jeff - It may, and going to explore.
    - Transmit spectrum? - Does have spectral launch shape of duobinary but not rolling humps.
- Brian Brunn
    - Some similarity between EE NRZ and duobinary.
    - Masks on slide #14 were calculated, not arbitrarily placed.
- Joe Abler
    - A BERT was used as a Tx.
    - Translating into CMOS?
    - Pre-emphasis filter – Jeff - done with lab equipment, going into CMOS should improve things.
- Decoder is not complicated
- Ali Ghiasi –
    - partial response coding - yes
    - some older papers stated that DFE has less improvement on duobinary
- Steve Anderson
    - For Edge equalization only single slicer being used
- Brian Seemann
    - What happens with short channels?
        - Change a threshold voltage and it becomes a NRZ pass-through?
- Mike Altmann –
    - In presence of noise would it adapt to another solution. Jeff - Yes, and further analysis is underway.

A late presentation request was received from Brian Von Herzen.
Chair asked group if it would hear the presentation.
Approved by voice vote without objection.

Presentation #26

Title – Crosstalk and Receiver Equalization for 10G Serial Ethernet
By – Majid Barazande-Pour, Vitesse
See barazande_pour_01_0704.pdf

Discussion

- Ali Ghiasi -Would the code still be DC-balanced? Majid – didn't check
- Charles – if we use scrambled data –

Presentation #27

Title –
By – Brian Von Herzen, FPGA Prototypes
See vonherzen_01_0704.pdf

Discussion

- Presentation will be uploaded
- Mary Mandich – "half diagonal" matrix needs to be considered as all systems do not necessarily meet the architecture of central located A/B'S
- Jeff Cain – the channel model should not have anything to do with the implementation
- John D'Ambrosia – does this presentation suggest to change the objectives or is it input into the channel adhoc.
    - Brian –
        - not changing the objectives
        - can optimize the channel to enable the 30" inch market with 4000-13
    - John to Joel Goergen – is 4000-13 enabled for use with the current definition of "improved FR-4."
        - Yes, and at 40" it met the mask, which means a 30" 4000-13 would already meet the channel model
- Joel Goergen –
    - The matrix of estimating the backplane length on the diagonal of the enclosure is inappropriate as the enclosure includes more than the backplane.

Meeting adjourned for day at 5:30pm

Thursday, July 15, 2004
Meeting reconvened at 8:44am

The meeting will have a hard-stop at noon today.

Presentation #27

Title – To-Do List
By – Adam Healey
See healey_01_0704

Distinct Identity Issue

Straw Poll #1: The following motion from the May Interim is conflict with the "Distinct Identity" for 802.3ap.

> Motion: Move to augment the existing 802.3ap objectives to include defining a 4-lane 10Gb/s PHY for operation over the 802.3ap channel model.
>
> Add the following bullet to the objectives:
> - Define a 4-lane 10Gb/s PHY for operation over the 802.3ap channel model

Method of resolution

Option A – Ignore conflict with "Distinct Identity"
Option B – Modify the Distinct Identity
Option C – Drop 4-lane 10 Gb/s PHY objective

Results: Option A - 0
Option B - 32
Option C - 6

Motion # 1 General Session Motion
Description: Modify "Distinct Identity" criteria, bullet #2, to:

The standard will define at most one single lane PHY for 1Gb/s, at most one single lane 10Gb/s PHY, and at most one four-lane 10Gb/s PHY.

Motion Type: Technical 75 % required
Moved By: Charles Moore
Seconded By: Schelto van Doorn

Results:	All	Yes – 40	No – 0	Abstain - 4
	802.3	Yes – 23	No – 0	Abstain - 1
P/F	**Motion Passes**			

Straw Poll#2 – Preference for definition of "Improved-FR-4"
Option A - Slide #5 from Goergen_01_0704 (original numbers)
Option B - Slide #6 from Goergen_01_0704 (proposed modified numbers)

Results Option A - 21
Option B - 15

Motion # 2 General Session Motion
Description: Move to adopt the Dk/Df values defined in goergen_01_0704, (pdf) page 5, as the minimum definition of "Improved FR-4" with modification to temperature tolerance from "0 to 55°C" to "0 to 70°C."

Reference goergen_01_0704, goergen_01_0504, and Goergen_02_0304.

Motion Type: Technical 75 % required
Moved By: Joel Goergen
Seconded By: Jeff Cain

Results:	All	Yes – 41	No – 0	Abstain - 6
	802.3	Yes – 14	No – 0	Abstain - 6
P/F	**Motion Passes**			

Motion #3 General Session Motion
Description: Clause 45 Register Set and Clause 45 MDIO interface be adopted.

Motion Type: Technical 75 % required
Moved By: Yong Kim
Seconded By: Thomas Joergensen

Results:	All	Yes – 35	No – 0	Abstain - 15
	802.3	Yes – 16	No – 0	Abstain - 5
P/F	**Motion Passes**			

Motion #4 General Session Motion
Description: Auto-negotiation as a minimum include port-type (e.g. 1G 1 lane, 10G 4 lane, 10G 1 lane) negotiation and any parameter exchange required to select the proper PMA.

Motion Type: Technical 75 % required
Moved By: Thomas Joergensen
Seconded By: Yong Kim

Results:	All	Yes – 39	No – 0	Abstain - 8
	802.3	Yes – 19	No – 0	Abstain - 4
P/F	**Motion Passes**			

Discussion
- Defines minimum "bringing up" link
- What is definition of "bringing up" the link

Motion #5 **General Session Motion**
Description: **Auto-negotiation not be restricted to existing base page definitions.**

Motion Type: Technical 75 % required
Moved By: Thomas Joergensen
Seconded By: Yong Kim

Results:	All	Yes – 34	No – 0	Abstain - 11
	802.3	Yes – 17	No – 0	Abstain - 6
P/F	**Motion Passes**			

Discussion
Aligns with direction in 10GBASE-T

Straw Poll # – Autonegotiation Signaling / Methodology Proposals

- Option A - Prefer [Clause 28, SSP - modified link pulse].
- Option B - Prefer [Clause 37, Serdes – 8B/10B].
- Option C - Prefer a solution, and other than presented.
- Option D - Prefer a solution, and I do not care which.

Vote Once

Results
Option A - 18
Option B - 11
Option C - 2
Option D - 5

Straw Poll # - Is it valuable to be electrically compatible with other signaling applications over the lowest common denominator channel, such as OIF CEI 11G SR/LR, Fibre channel 8G and 10G, and XFI?

Vote once.

Results
Important - 13
Some value - 11
Not important - 15

Discussion

- Very high level goal
- Does this force chip-to-chip solutions onto the backplane solution space
- This would be a lot of work.
- Is this a signaling or channel issue?
- Do you want the electrical specifications to be compliant with other electrical specifications?
- Value in being able to use same backplane

Motion #6 **General Session Motion**

Description: Move that the IEEE P802.3ap Task Force request approval of the amended 5 criteria and objectives, as shown in agenda_01_0704, by the 802.3 WG and request that the 802.3 WG forward the 5 criteria to the 802 SEC for approval

Motion Type: Technical 75 % required
Moved By: Charles Moore
Seconded By: Schelto van Doorn

Results:	All	Yes – 37	No – 0	Abstain - 0
	802.3	Yes – 20	No – 0	Abstain - 0

P/F **Motion Passes**

September Interim – TBD
November Interim – San Antonio, TX, Hyatt Regency. Information posted on web.

New ad hoc to be formed – tentatively called “signaling ad hoc”
Define parameters for simulation

Motion to adjourn approved by voice vote without objection.
Meeting adjourned 11:30 pm