SERDES compatible FLP AN Proposal

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Agenda

1. **Clause 14 Link Pulses**
   - SERDES compatability
2. **OOB signaling in other Stds bodies**
   - PCI-Express
   - SATA
3. **Applying this to 802.3ap**
   a) Overview of the proposal
   b) Proposed signalling for 1.25 & 3.125G baud rates
   c) SSP detection & validation
   d) SERDES requirements
4. **Potential for removal of driven Idle**

Clause 14 Link Pulse specification

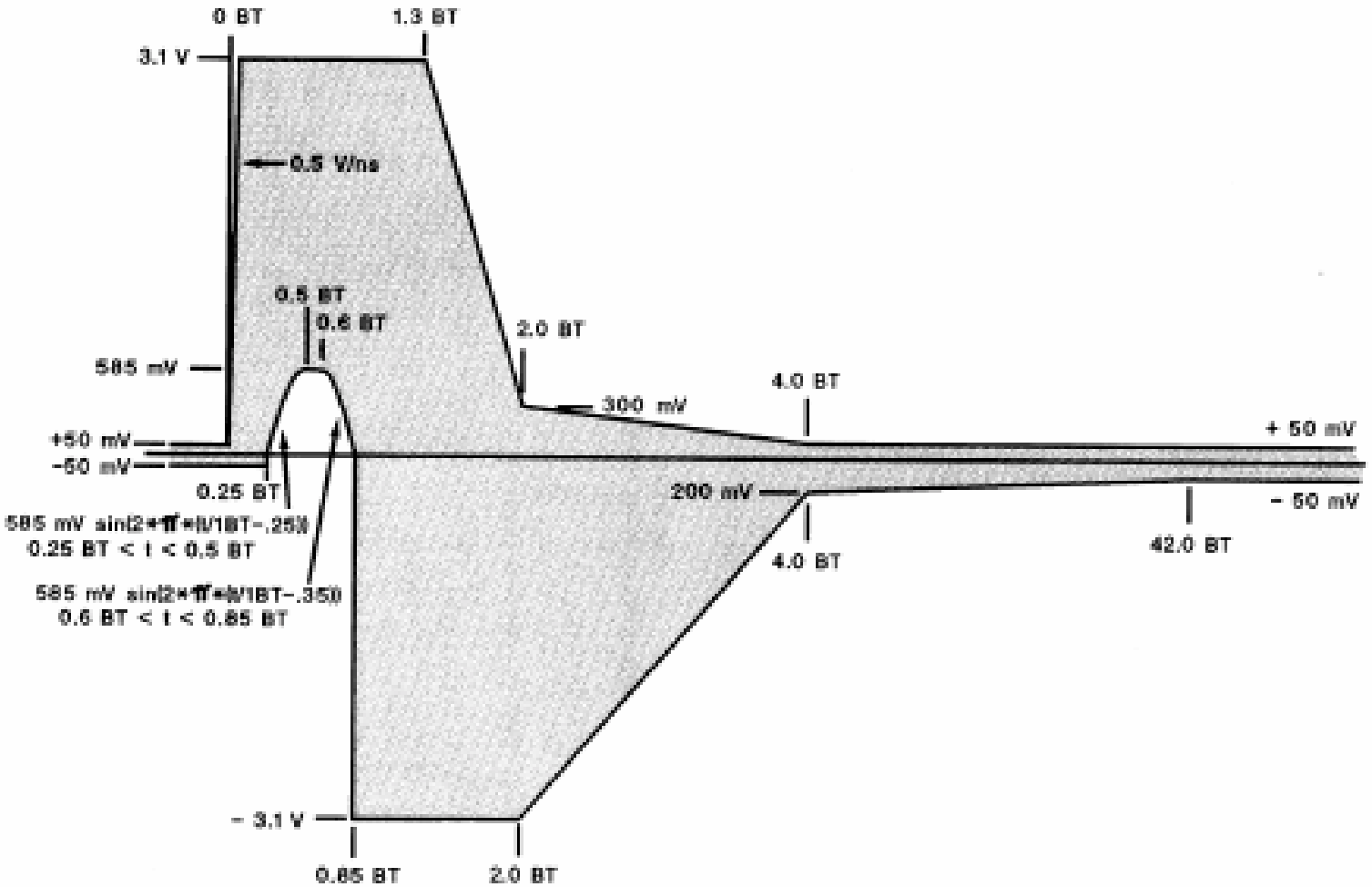


Figure 14–12— Transmitter waveform for link test pulse

Clause 14 Link Pulse specification

- **10BaseT defined original link pulse for transformer coupled operation across 100m of twisted pair**
  - The link pulse mask must be met at all points from the Tx transformer secondary to the receiver
    - In practise this required wave-shaping or external filter modules at the transmitter
  - Poor fit with CML transceiver levels
    - Template allows up to ± 3.1V of amplitude.
      - May cause ESD circuits to switch on (clamping) in some implementations
      - 3.3V compatible oxide may not be a process option at 90nm or below
        - » In spec link pulses could cause gate oxide breakdown
  - Not DC-balanced
    - DC balance not a problem when transformer coupled due to long decay time constants.
- **Not impossible to meet, but**
  - Inappropriate for an advanced CMOS process which is AC coupled and optimised for operation at 2.5Gb/s+
  - Tangential to developments in other SERDES standards
    - No re-use

Work in other standards bodies

- **PCI-Express and Serial ATA use low speed (OOB) signalling for power management and configuration**
  - Signalling uses bursts of data symbols separated by electrical idle
    - In Electrical Idle $V_{diff} = 0$, with normal V_{cm} maintained
  - Bursts are received by detection of a differential signal above a defined threshold
    - Symbols used and symbol rate are (within reason) unimportant
    - However bursts are required to be DC-balanced
  - The Burst detector doubles up as a loss-of-signal detector in normal operation

PCI-Express

- **Uses "Beacon" pulses to transmit wake-up requests from powered down devices across powered down links**
  - Lack of main power & clocks requires that the beacon be loosely specified.
    - Minimum pulse width 2nS, maximum pulse width 16.67us
      - Maximum period 33.333us
    - Transmission of a Comma character at full rate qualifies as a valid beacon
  - A signal detection threshold in the range of 65-175mV is sufficient to detect compliant beacons through a 75-200nF capacitor
    - *Ref PCI-Express Base specification 1.0a section 4.3.2.4.1*

Serial ATA

- **Bursts of "Align" primitives separated by electrical idle are used to indicate "comreset/cominit" and "comwake"**
  - Align primitive is K28.5,D10.2,D10.2,D27.3
  - 106.7ns burst length is of a similar duration to a clause 14 link pulse (nominally 100ns)
  - Bursts start at end Asynchronously to Align primitive
    - Analog switching issues
- **Indication type is dependant on gap between bursts**
  - Comreset/Cominit bursts are seperated by 320ns of idle
  - Comwake bursts are seperated by 106.7ns of idle
- **Although transmission is at normal symbol rates, receiver may be powered down (Aux power no clocks)**
  - Reception uses differential signal level detection
  - SATA detector threshold is specified as 50 to 200mv
    - Same as 10GbaseCX4

Overview of Proposal

- **Replace clause 14 Link pulses with ~100ns symbol sequence Pulses (SSPs) separated by electrical idle**
  - Practicality of 100ns bursts already demonstrated by SATA
  - SSP length will vary due to Analog switching delays
    - Non-instantaneous; Non-Synchronous !
    - Define length as an allowable range : eg 96-112ns
- **Transmitter shall transmit SSPs at its lowest capable rate**
  - Support AN of multi-rate PHYs in lower performance systems
  - Less implementation freedom = less interoperability problems
  - Less EMI
- **Use a differential signal detector to detect these "pulses" irrespective of Tx'ed symbol rate**
- **Replace FLPs with SSPs in clause 28 FLP protocol**

1.25G Signaling

- **To transmit an SSP, the transmitter shall transmit between 96-112ns of D21.5 symbols (1010101010).**
  - D21.5 is chosen because it's DC balanced and disparity neutral.
  - At this symbol rate, the time to transmit 13 8b10b symbols is 104ns.
- **An SSP can start and end Asynchronously to the symbol boundaries.**
  - Allows asynchronous modulation of the analog Transmitter (as in SATA)
- **Within an SSP all normal 1.25G data transmit electrical specifications hold**
  - Allows existing datapath to be used as source of SSP
  - Ensures a non SSP-capable 1.25G Rx'er will see a benign symbol stream

3.125G Signaling

- **To transmit an SSP, the transmitter shall transmit between 96-112ns of D21.5 symbols (1010101010).**
  - D21.5 is chosen because it's DC balanced and disparity neutral.
  - At this symbol rate, the time to transmit 32 8b10b symbols is 104ns.
- **An SSP can start and end Asynchronously to the symbol boundaries.**
  - Allows asynchronous modulation of the analog Transmitter (as in SATA)
- **Within an SSP all normal 3.125G data transmit electrical specifications hold**
  - Allows existing datapath to be used as source of SSP
  - Ensures a non SSP-capable 3.125G Rx'er will see a benign symbol stream

10G Signaling

- **To transmit an SSP, the transmitter shall transmit between 96-112ns of appropriate symbols.**
  - The Symbol sequence will depend on the Signaling and coding schemes chosen for 10G operation.
    - It will be DC balanced and of sufficient energy to meet the detection threshold levels defined for 1 & 2.5Gbps operation.
    - At this symbol rate, the time to transmit 16 64b66 symbols is 104ns.
- **An SSP can start and end Asynchronously to the symbol boundaries.**
  - Allows asynchronous modulation of the analog Transmitter (as in SATA)
- **Within an SSP all normal 10G data transmit electrical specifications hold**
  - Allows existing datapath to be used as source of SSP

SSP detection and validation

- **Use a differential signal detector to detect these SSPs irrespective of Tx symbol rate**
  - Define threshold range : 65-175mV
    - All signals detected above this threshold are potential SSPs
    - All signals below this threshold are regarded as “IDLE”
- **Validate SSP width**
  - Detector shall reject all SSPs outside of range 48-176ns
    - 6-22 symbols @ 1.25Gbd
    - 15-55 symbols @ 3.125Gbd
  - Detector shall accept all SSPs inside of range 96-112ns
    - 12-14 symbols @ 1.25Gbd
    - 30-35 symbols @ 3.125Gbd
- **Validate SSP spacing**
  - Should we define a blinding period after a valid SSP ?

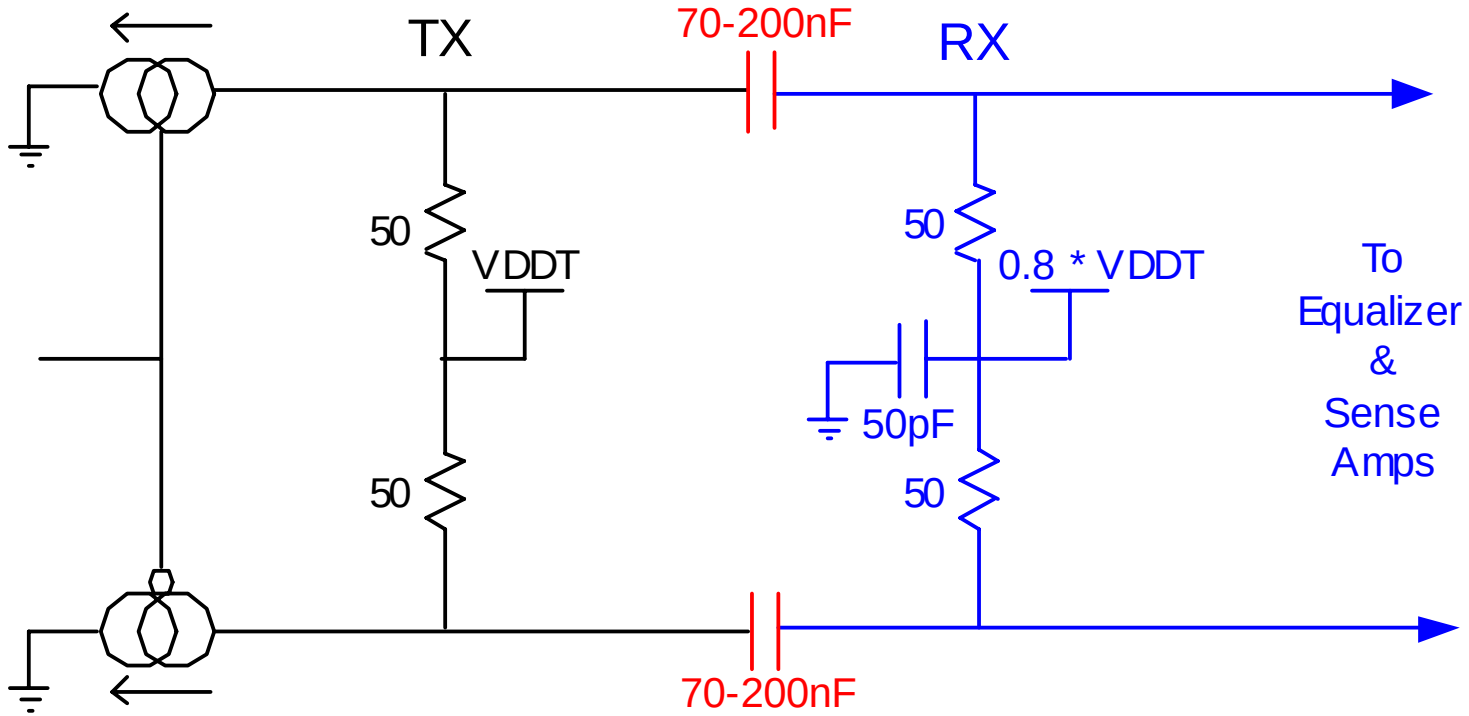
SERDES requirements

- **Serdes Transmitter must support an electrical idle state**
  - A simple Transmitter disable may be sufficient if Vcm is not maintained in electrical Idle state
- **Receiver must implement a true signal detect**
    - A signal detection threshold in the range of 65-175mV would be sufficient and compatible with PCI-Express & SATA
    - Detection latency should be no more than 50ns to meet detection thresholds
- **Multi-purpose SERDES with support for PCI-Express or SATA will already have these features**

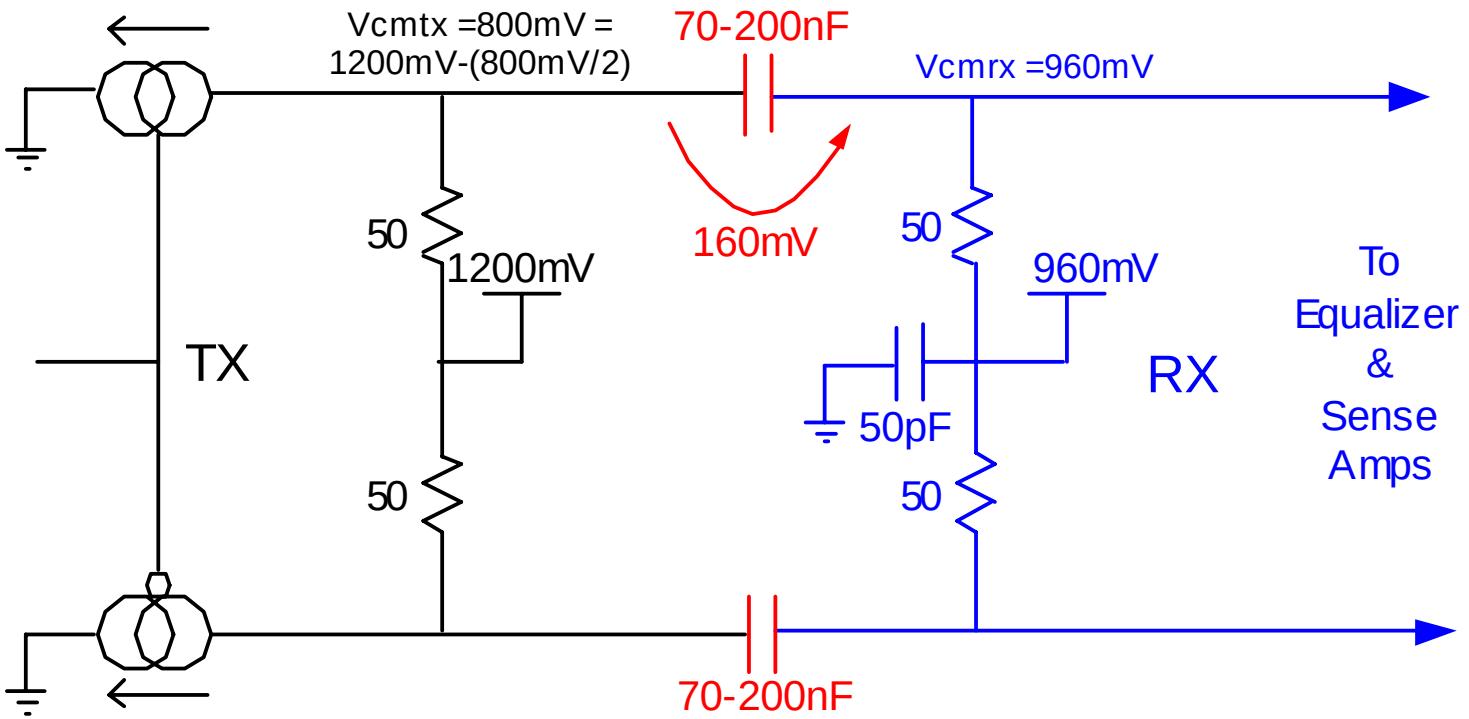
AC coupling cap time-constant issues

- **Our conclusions are that the charge/discharge time of the AC coupling capacitor is dependant on the Tx termination resistance (50 Ohms), So the time constant is derived from this and the capacitor value.**
  - For a 75nF capacitor the time constant would be 3.75uS. So applying the rule of thumb that it takes 5 time constants for "complete" decay, gives a value of approximately 19us.
  - Similarly for a 200nF capacitor the decay time would be about 50us.
    - 75-200nF is the specified coupling capacitor range for PCI-Express
- **These decay times are similar to the SSP separation (62.5us), but much larger than the SSP width (100ns).**
  - So we can expect no real change in stored charge on the coupling capacitors during the SSP bursts.
- **We can also conclude that the DC-balance over a 100nS SSP will have no perceivable effect on the charge on the AC coupling caps**
  - Especially as it will have 62.5us to recover
  - So there is no need for absolute DC balance during the burst
    - Crude modulation can be allowed

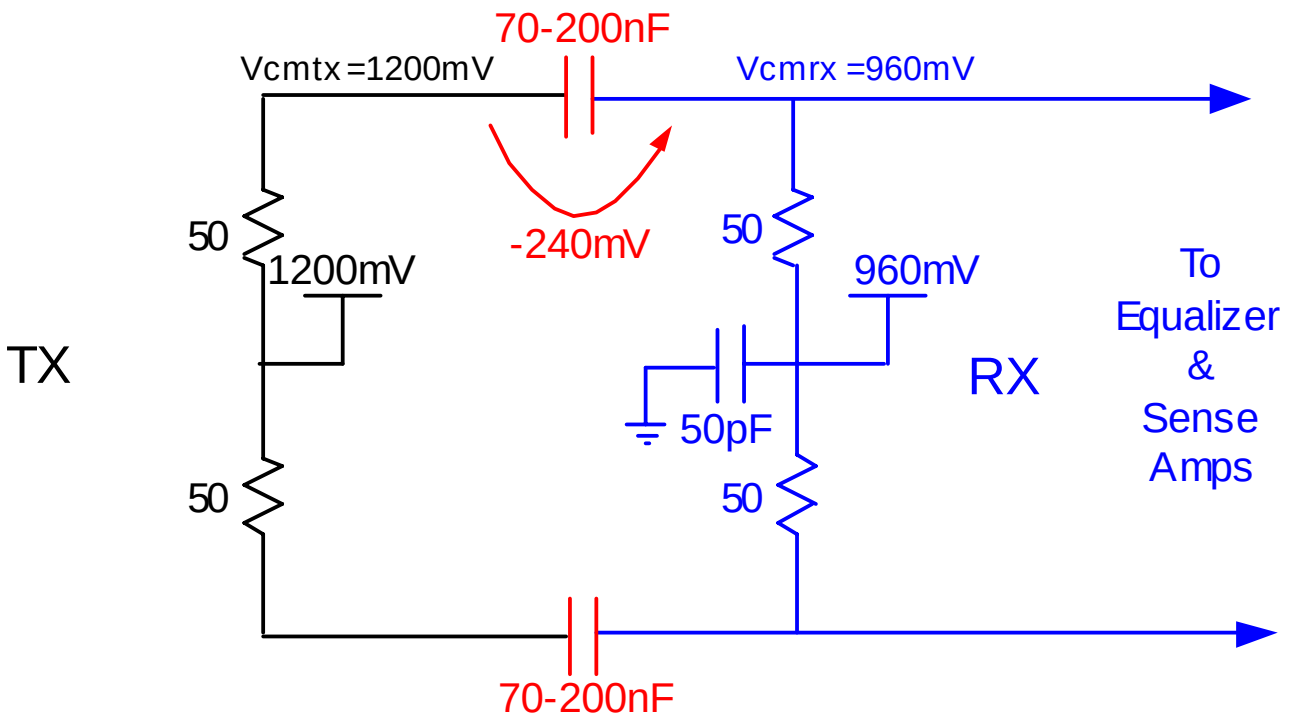
Simplified AC coupling diagram



Charge on AC Coupling cap in normal operation



Charge on AC coupling cap if Tx'er disabled



Effect of TX'er not driving an Idle level

- **When disabled the transmitter outputs will quickly both move to their Termination rail, and the burst separation is sufficient to allow the capacitors to charge to the difference between this rail and the receivers termination voltage.**
  - Typically this would be about half the single ended swing.
- **When a burst starts the stored charge will depress the signals on both sides of the receiver differential pair by this value (say 0.4V).**
  - This may cause the negative going side of the pair to go below the normal common mode range of the receiver, potentially causing the receiver current source to come out of saturation and reducing the received eye.
- **This would all be really bad if we were actually trying to lock to and derive data from the burst, however all we are trying to do is detect the presence of the differential signal. This should still be possible.**

- **Note also that this condition is exactly the same as the effect of turning on a disabled link, and is no more harmful.**

Further work

- Driven or undriven IDLE
- 10G SSPs