Proposed Text for SERDES compatible FLP AN Proposal

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Proposal to Transmit FLPs Using SERDES Signaling

Background

IEEE 802.3 Clause 28 introduced the concept of auto-negotiation among link partners operating at different speeds. The auto-negotiation procedure uses 10BASE-T link pulses to establish speed and capability for the link partners. This approach has been suggested for 802.3ap study group. However, FLP signaling level is not compatible with common SERDES designs operating at 1Gbps and above. This proposal discusses a means to transmit and receive pulses like FLPs using SERDES compatible signaling.

Link Pulse Transmission

A 10BASE-T link integrity test pulse is a transformer coupled differential pulse that meets the transmitter waveform mask in clause 14 (Figure 14–12). This pulse is approximately 100ns in duration. Clause 28 renames these pulses “Fast Link Pulses” (FLPs) and uses bursts of them to transfer information between link partners.

The proposed Auto-Negotiation method replaces the 10BaseT link integrity test pulses that make up FLPs in clause 28 with equivalent duration sequences of DC balanced symbols at one of the specified data rates. For clarity these will be referred to as “Symbol Sequence Pulses” or SSPs.

During the period between SSPs, the transmitter shall maintain an electrical IDLE level. Electrical IDLE is defined by limiting the differential output of the transmitter to no more than 20mV (|TXD+ - TXD-| <20mV).

SSPs can be detected by an analogue differential signal detector irrespective of the symbol rate at either side of the link.

In order to ensure compatibility with legacy implementations we propose explicitly defining the Symbol sequences used at the 1G and 2.5G Bit rates. With no legacy issues at 10G we may be able to define a looser specification, however final definition of the 10G AN signaling awaits adoption of a 10G signaling and coding scheme.

A multi-rate capable transmitter shall always send SSPs at its lowest capable rate.

Symbol Sequence Pulse Specification (1Gbps)

To transmit a pulse, the transmitter shall nominaly transmit 13 D21.5 symbols (1010101010). The symbol period is 8ns. The baud period is 800ps. D21.5 is chosen because it’s DC balanced and disparity neutral. The symbol period is chosen so it’s compatible with 1Gbps SERDES implementations. At this symbol rate, the time to transmit 13 symbols is 104ns.

The transition to and from the electrical Idle state is an analog process and is not required to be (and cannot be) synchronous to symbol boundaries. To allow for this the transmitter will be required to actively transmit D21.5 symbols to normal data transmit specifications for between 96 and 112ns. This equates to 12-14 symbol periods.

Symbol Sequence Pulse Specification (2.5Gbps)

To transmit a pulse, the transmitter shall nominally transmit 32 D21.5 symbols (1010101010). The symbol period is 3.2ns. The baud period is 320ps. D21.5 is chosen because it's DC balanced and disparity neutral. The symbol period is chosen so it's compatible with XAUI SERDES implementations. At this symbol rate, the time to transmit 32 symbols is 102ns.

The transition to and from the electrical Idle state is an analog process and is not required to be (and cannot be) synchronous to symbol boundaries. To allow for this the transmitter will be required to actively transmit D21.5 symbols to normal data transmit specifications for between 96 and 112ns. This equates to 30-35 symbol periods.

Symbol Sequence Pulse Specification (10Gbps)

The Symbol sequence used will depend on the Signaling and coding schemes chosen for 10G operation. It shall be DC balanced and of sufficient energy to meet the detection threshold levels defined for 1 & 2.5Gbps operation.

SSP Burst Encoding

A SSP burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a SSP and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a SSP present in an even-numbered pulse position represents a logic one, and a SSP absent from an even-numbered SSP position represents a logic zero. Clock SSPs are differentiated from data SSPs by the spacing between them, as shown in Figure 2 and enumerated in Table 1.

The encoding of data using SSPs in an SSP Burst is illustrated in Figure 1.

Burst Timing

The first SSP in an SSP Burst shall be defined as a clock SSP. Clock SSPs within an SSP Burst shall be spaced a minimum of 88μs apart with a typical spacing of 125 ± 14 μs.
These values are chosen so they are compatible with charging and discharging times across AC coupling caps of value 100nF or above. If the data bit representation of logic one is to be transmitted, a SSP shall occur a minimum of 32.5μs (typically 62.5 ± 7 μs)

after the preceding clock SSP. If a data bit representing logic zero is to be transmitted, there shall be no SSPs within 88 µs of the preceding clock SSP.

The minimum number of pulses in a burst is 17, same as Clause 28. The maximum number of pulses in a burst is 33, also the same as Clause 28. The minimum burst width is 1.1ms. Typical burst width is 2ms.

Minimum time from FLP burst to FLP burst is 4ms. Typical time from FLP burst to FLP burst is 16ms. This is illustrated in Figure **3** and enumerated in Table 1.

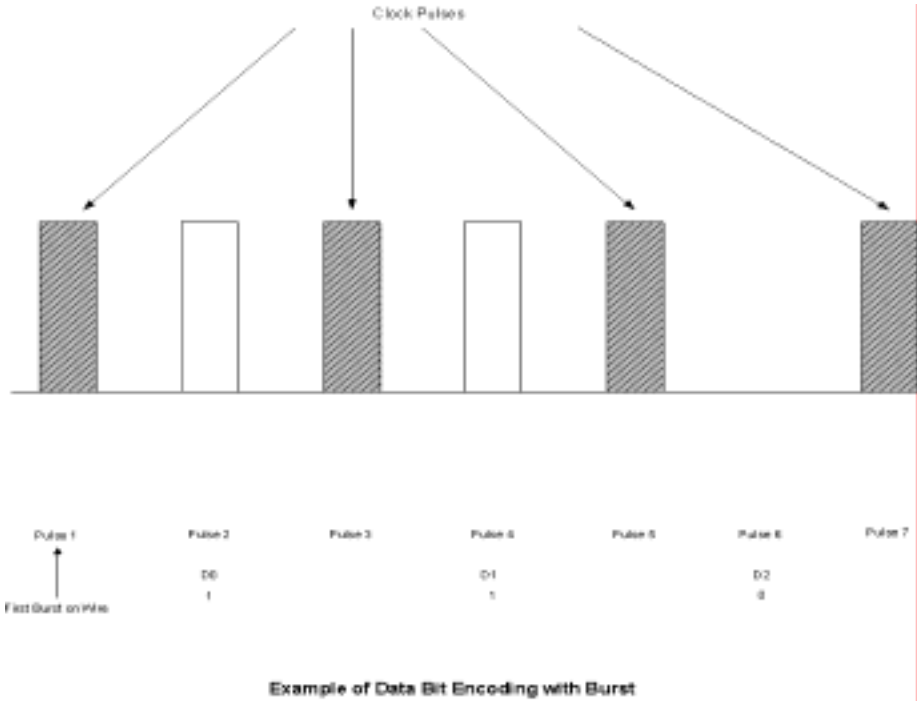

Figure 1 Example of Data Bit encoding within SSP Bursts

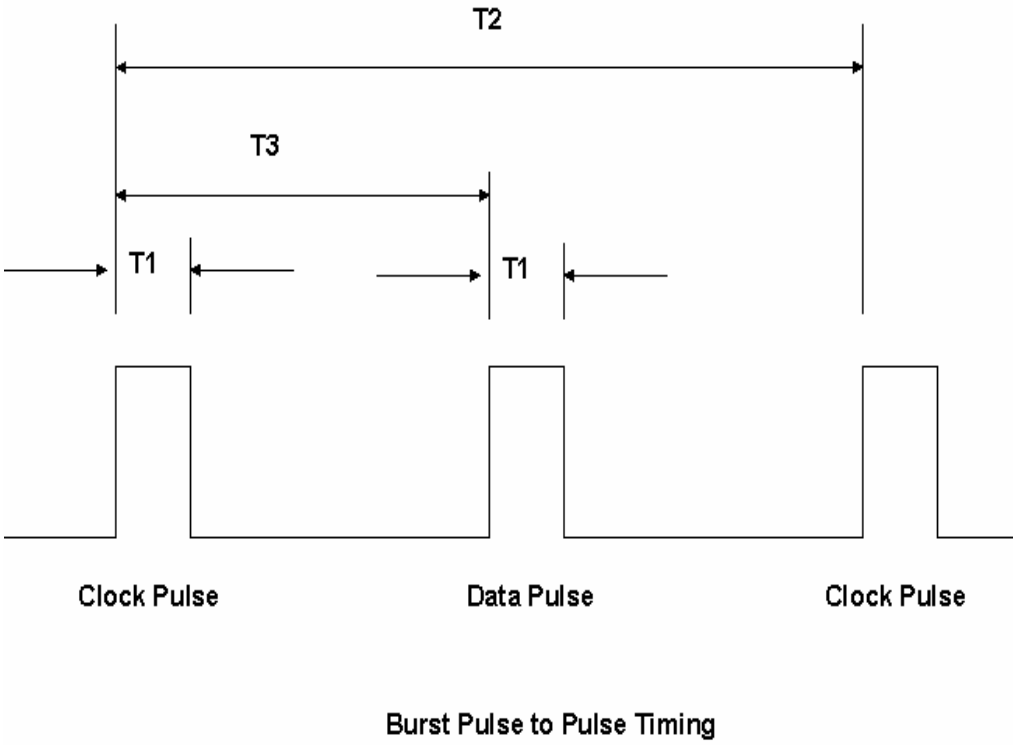

Figure 2 Burst Pulse to Pulse Timing

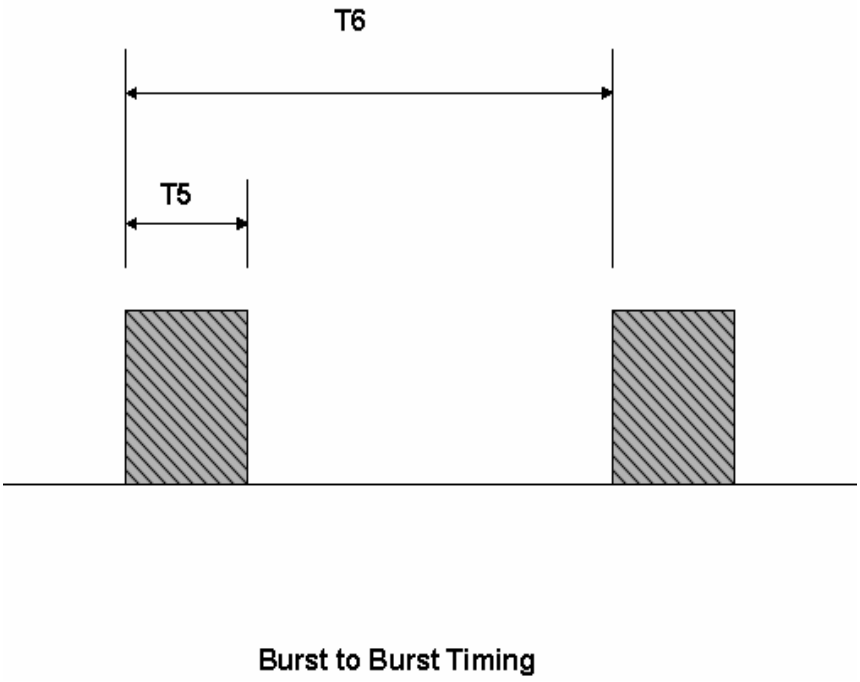

Figure 3 Burst to Burst Timing

The following table summarizes the timing parameters:

#	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width		100		ns
T2	Clock Pulse to Clock Pulse	88	125		µs
T3	Clock Pulse to Data Pulse (Data=1)	32.5	65		
4	Pulses in a Burst	17		33	#
T5	Burst Width	1.1	2		ms
T6	FLP Burst to FLP Burst	4	16		ms

Table 1 SSP Burst Timing Summary

The following table summarizes the electrical parameters for the transmitter:

#	Parameter	Min	Typ	Max	Units
1	Differential Peak to Peak Voltage	800	1000	1350	mV
2	Transmitted SSP width	96	100	112	ns
3	Electrical Idle Differential Peak Output Voltage[1]			20	mV

Table 2 Transmitter Electrical Specifications

Receiver Specification

To be able to detect the SSPs, the receiver can be implement a simple differential threshold detector. If must be able to determine the differences between a transmitted pulse and electrical IDLE level. The following table summarizes the receiver electrical parameter:

#	Parameter	Min.	Typ.	Max	Units
1	Differential Peak to Peak Voltage	175	1000	1350	mV
2	Electrical IDLE Detect Threshold[2]	65		175	mV
3	Receive SSP width reject threshold[3]	48		176	ns
4	Receive SSP width accept threshold[4]	96		112	ns

Table 3 Receiver Electrical Specifications

[1] $V_{TX\text{-}IDLE\text{-}DIFFp} = |V_{TX\text{-}Idle\text{-}D+} - V_{Tx\text{-}Idle\text{-}D-}| <= 20$ mV

[2] $V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*|V_{RX\text{-}D+} - V_{RX\text{-}D-}|$ Measured at the package pins of the Receiver

[3] The Receiver shall reject all SSPs outside of this specifcation

[4] The Receiver shall accept all SSPs inside of this specifcation