Measured Dispersion Compensation Performance on Intel Backplane Channels

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Acknowledgements

- Thanks to Intel for providing the backplane infrastructure and related support.

Introduction

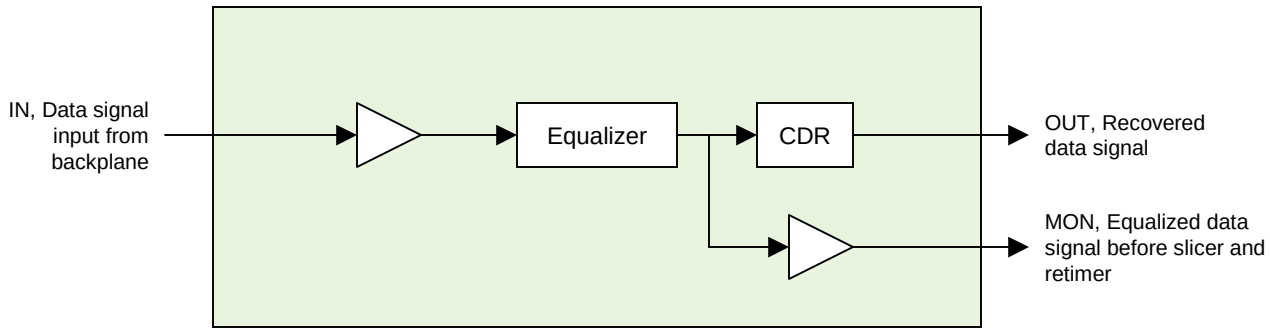
- This slide package summarizes tests integrating an Electronic Dispersion Compensation (EDC) device with the Intel backplane specified in peters_01_0904.
- These measurements represent the first phase of a series of measurements (see next slide). The main focus of this phase was to assess the ability to equalize the data signals traversing a backplane channel.
- Three sets of measurements are presented:
  - Unequalized pulse response of channels
  - Equalized error performance
  - Equalized eye opening

Measurement Phases

- In consideration of time and equipment availability, this first phase was limited in the following areas:
  - a sub-set of channels was considered: 8”, 12”, 20”, and 32”
  - PRBS7 was used for most measurements
  - interfering signals were not included
  - drive levels were not considered
- In the sub-sequent phases, the following will also be considered:
  - the remaining channels
  - use PRBS15 and/or PRBS31
  - measure the characteristics and effect of crosstalk
  - effect of drive level
  - other backplanes

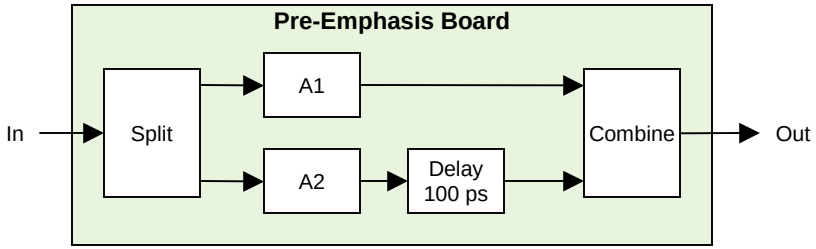
EDC Device

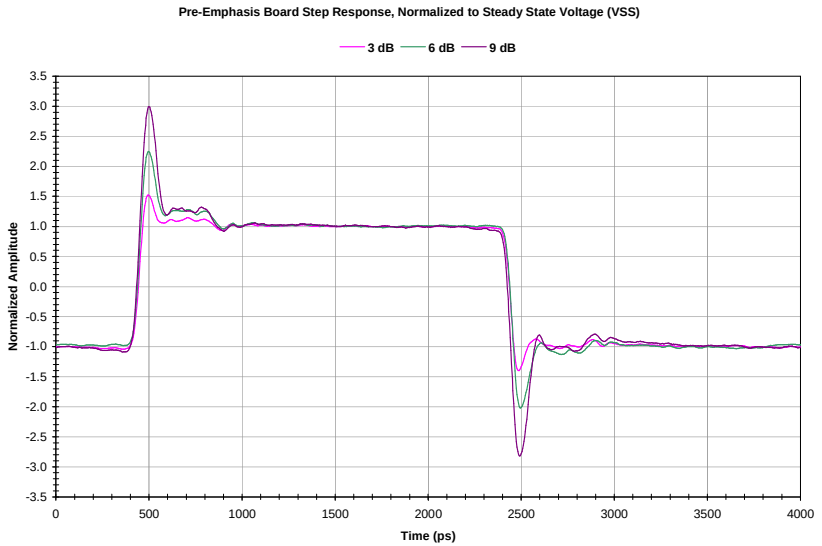
- The EDC device (shown below) equalizes the distorted data signal from the backplane and recovers the data signal.
- A monitor point permits observation of the equalized data signal before slicing and retiming.



Pre-Emphasis Emulation

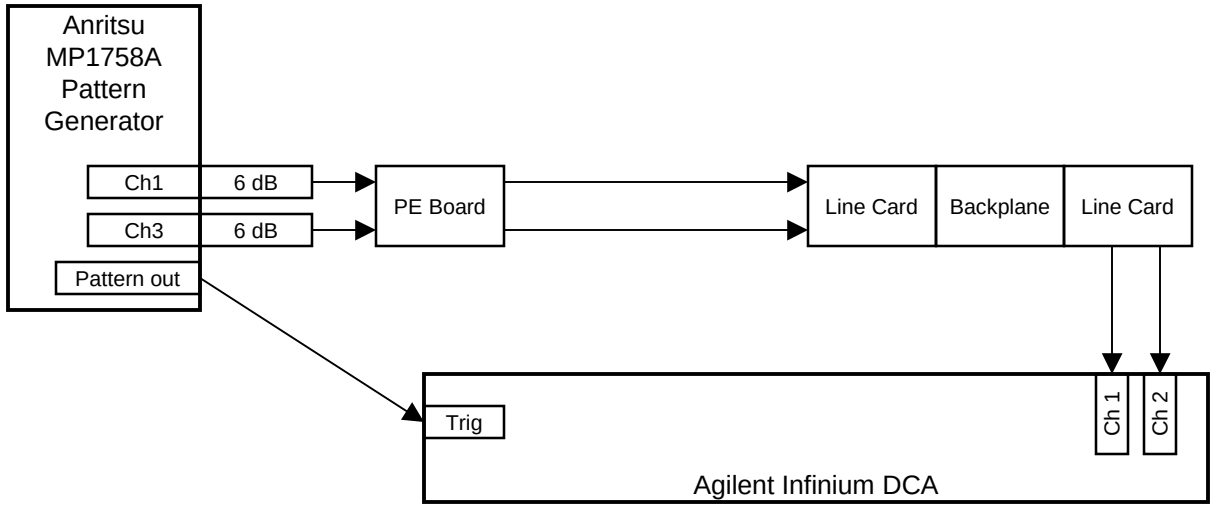
- To emulate the effect of a 2-tap Tx FFE, a linear pre-emphasis board (shown below) was employed.
- Pre-emphasis (same as RPST defined in 72.6.1.11), expressed in dB, is defined as the ratio of the peak voltage to the steady state voltage at the output when a step is applied to the input.
- The measured step response for three configurations (3, 6, and 9 dB pre-emphasis) are shown below.





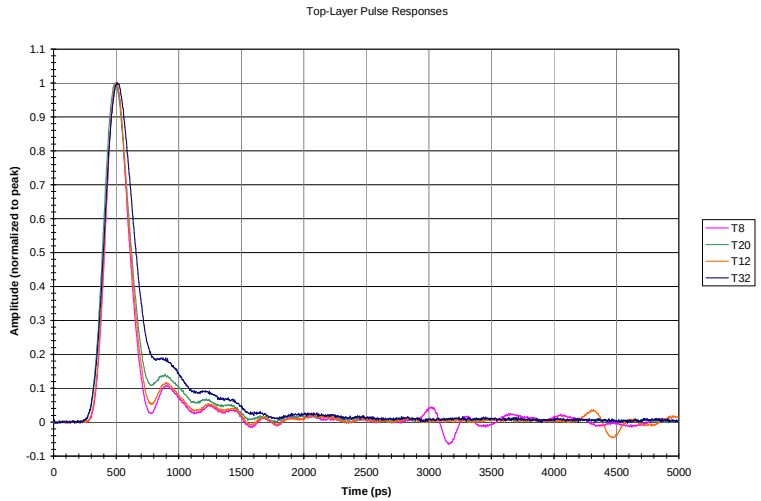
Pulse Response – Test configuration

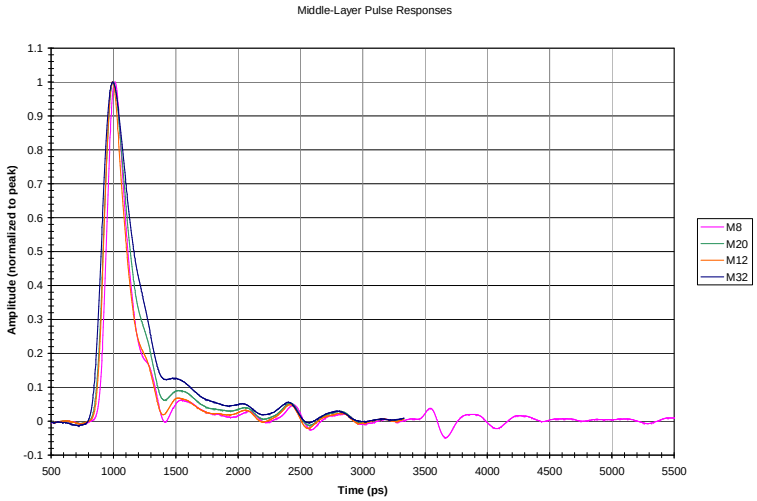
- The block diagram below illustrates the test configuration for the pulse response tests.
- For 0 dB pre-emphasis, the PE (pre-emphasis) board was removed.
- The repeating pattern consisted of a single “one” pulse followed by 512 “zero” pulses.

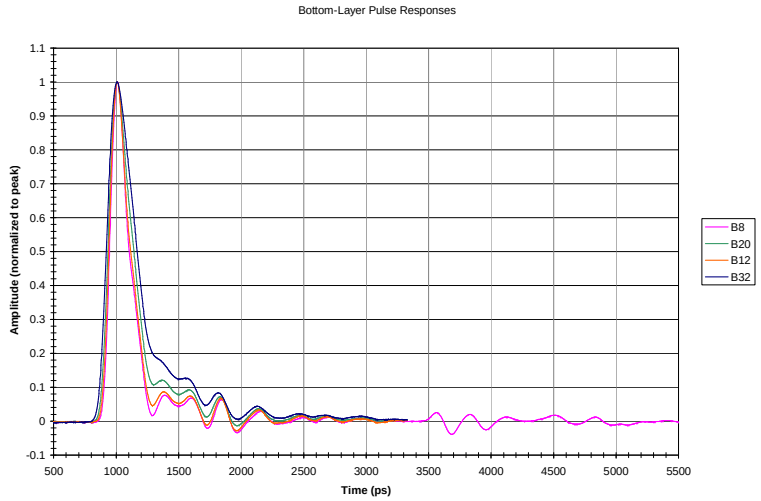


Pulse Response – Measured Results

- Measured pulse responses for all channels without pre-emphasis are shown on the three graphs on this slide.

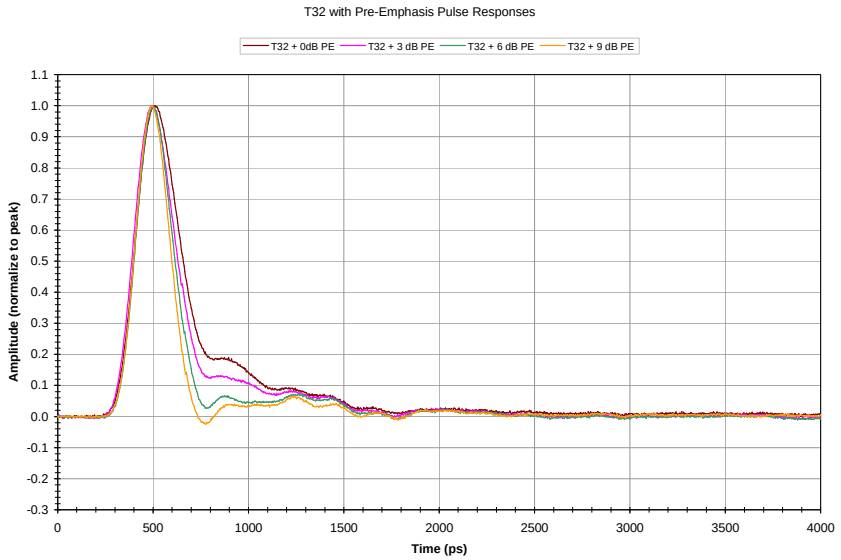






Pulse Response – Measured Results, T32 + Pre-Emphasis

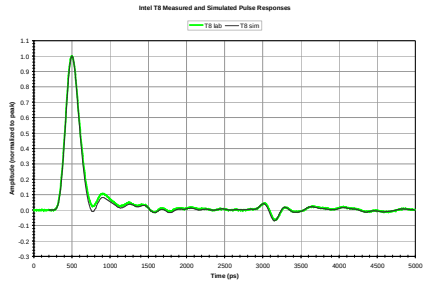
- The effect of pre-emphasis on the channel T32 pulse response is shown in the slide below.
- Note that the “friendliest” pulse response occurs with 9 dB pre-emphasis.



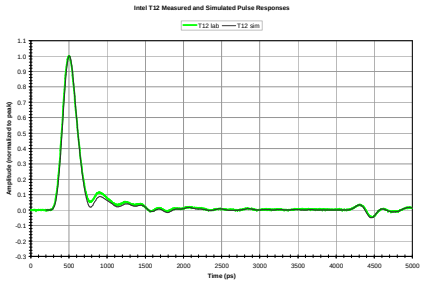
Pulse Response – Comparison with Simulated Pulses

- The following slide below compares the measured pulse response of each channel with the simulated pulse response derived from the measured s-parameters.
- The simulation model:
  - Tx: square pulse, 100 ps, 9.0 GHz BT LPF
  - Channel: s-parameter file (peters_01_0904_<channel>_thru.s4p)
  - Rx: 7.5 GHz BT LPF

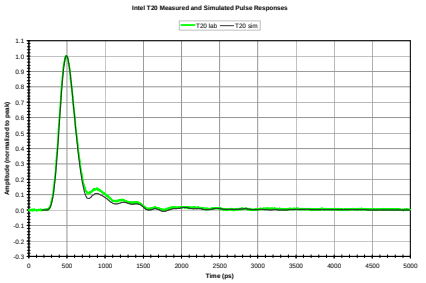
Pulse Response – Comparison with Simulated Pulses Plots NEW



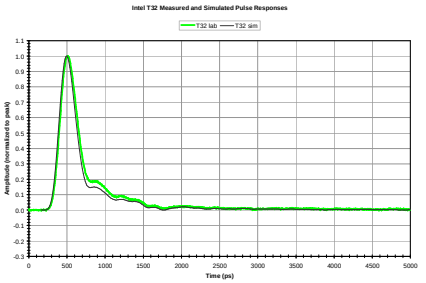
T8



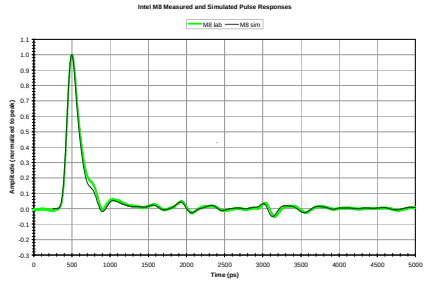
T12



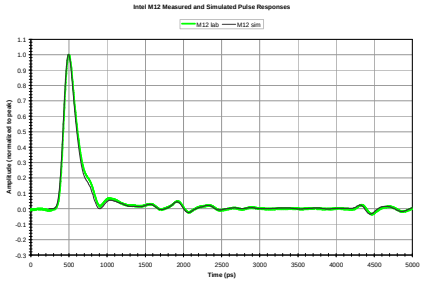
T20



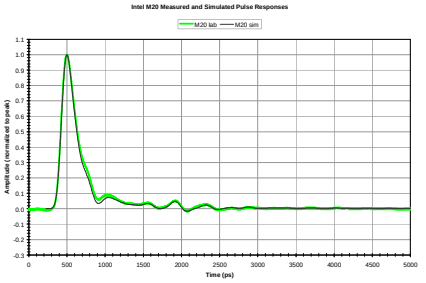
T32



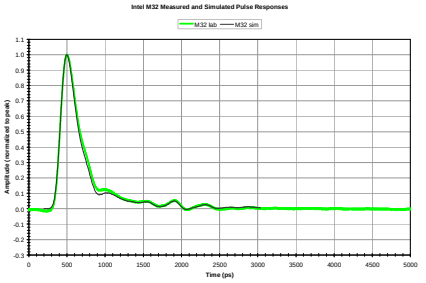
M8



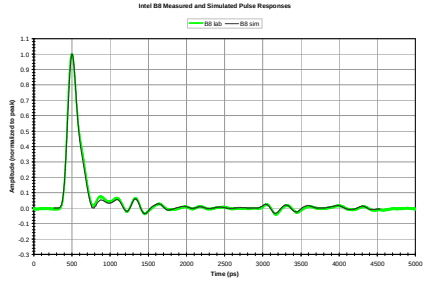
M12



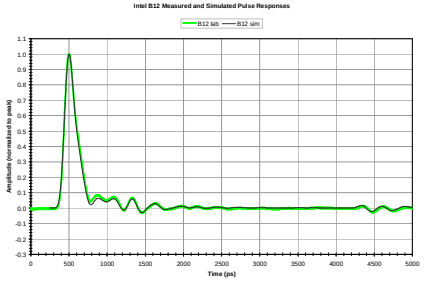
M20



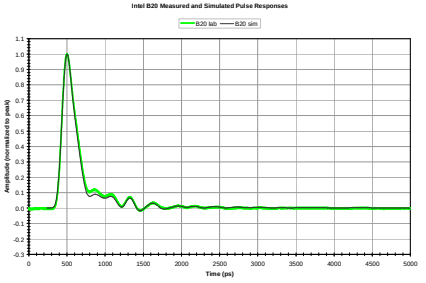
M32



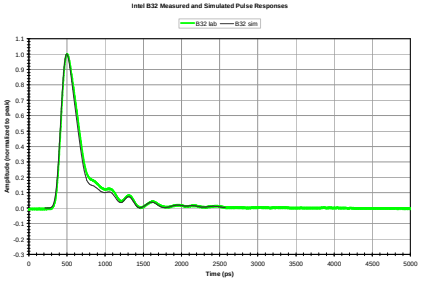
B8



B12



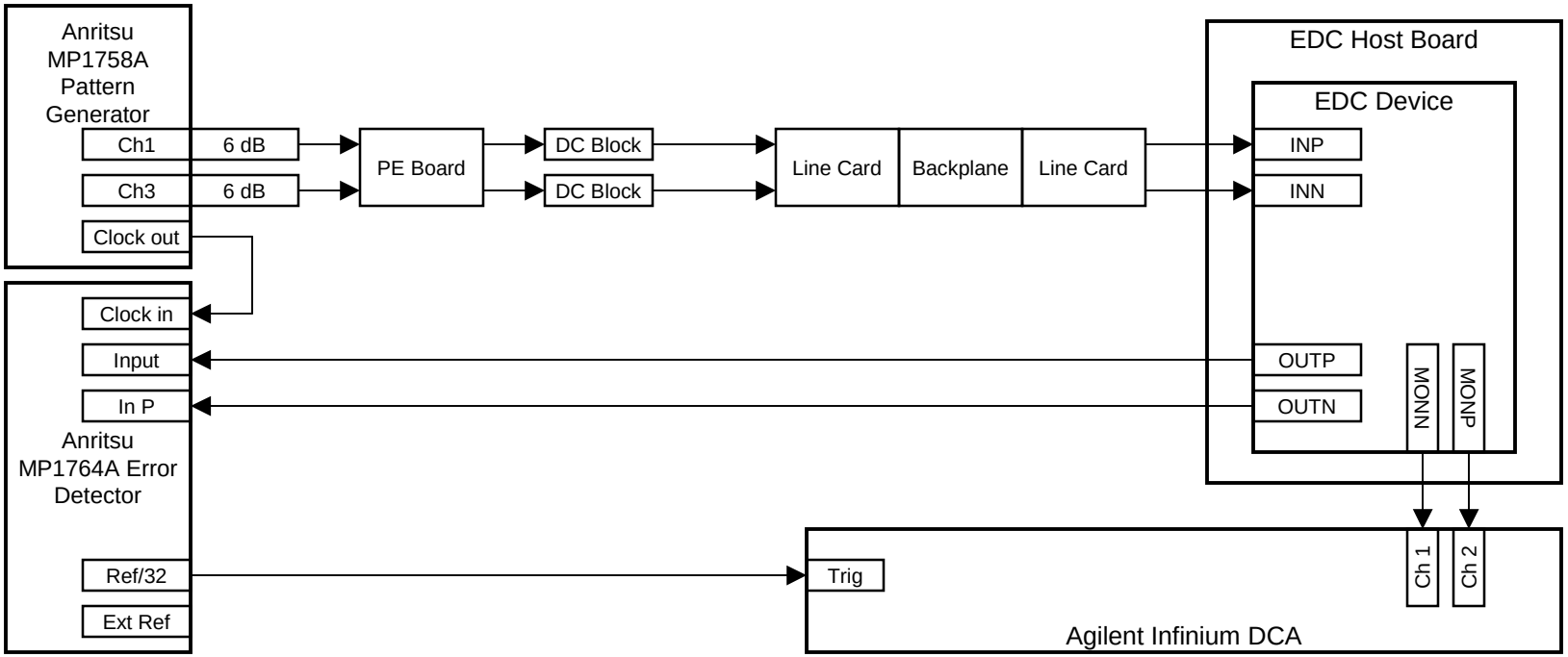
B20



B32

EDC/Backplane Integration – Test Configuration

- The block diagram below illustrates the test configuration for the EDC/backplane integration tests (for tests involving PRBS31 later an Anritsu MP1763B Pattern Generator was substituted).
- For 0 dB pre-emphasis, the PE board was removed.



EDC/Backplane Integration – Error Performance

- For each channel/PE combination the errors were counted on the recovered data.
- For all channels except T32, error-free data was recovered without pre-emphasis.
- T32 was error-free with 6 dB of pre-emphasis.
- Error-free is defined as no errors counted in 5 minutes or more.
- Test conditions: baud rate = 10.3125 Gbps, pattern = PRBS7

EDC/Backplane Integration – Eye Opening

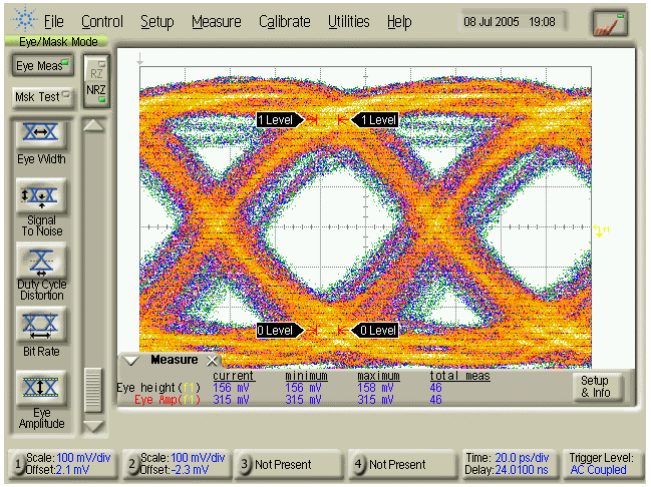
- “Best” eye opening (summarized for each channel on the following slide) was achieved with pre-emphasis ranging from 0 to 9 dB.
- Eye opening was measured as a ratio of default DCA parameters Eye Amplitude and Eye Height. Eye amplitude is the difference between the mean 1 and mean 0 values. Eye height defined as the eye amplitude minus 3 times the standard deviation of one and zero. Amplitude and standard deviation were measured over 10% of the eye width.
- Test conditions: baud rate = 10.3125 Gbps, pattern = PRBS7

EDC/Backplane Integration – Results Summary

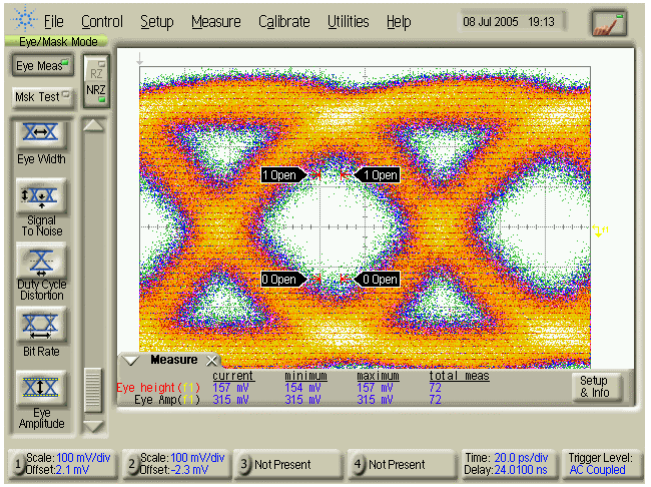
- The table below summarizes the pre-emphasis required for error-free operation and "best" eye.

Channel	*PE required to achieve error-free performance (dB)*	*PE required to achieve best eye opening (dB)*
B8	0	0
B12	0	0
B20	0	6
B32	0	9
M8	0	0
M12	0	0
M20	0	9
M32	0	9
T8	0	6
T12	0	6
T20	0	9
T32	6	9

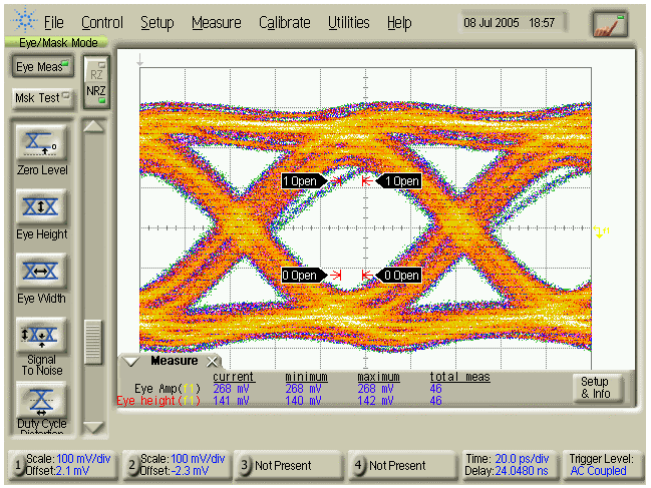
EDC/Backplane Integration – Equalized eye diagrams for Channel T12



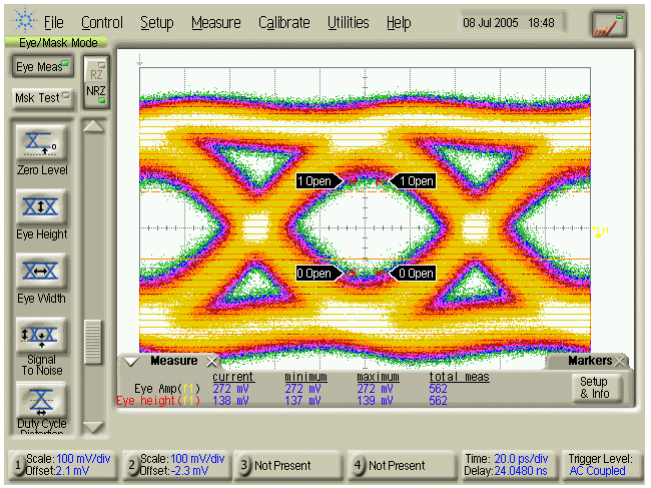
Channel: T12
Pattern: PRBS7
Mode: Full auto



Channel: T12
Pattern: PRBS31
Mode: Full auto



Channel: T12
Pattern: PRBS7
Mode: DFE only



Channel: T12
Pattern: PRBS31
Mode: DFE only

Test Results Summary

- Observations based upon the tests completed so far
  - The EDC operates error free on all channels of length {8”, 12”, 20”, 32”} and layers {B, M, T}.
  - To operate error-free pre-emphasis was required only on T32.
  - “Best” eye opening required anywhere from 0 dB to 9 dB of pre-emphasis.
  - “Best” eye opening is achievable using only the DFE at the receiver.
  - The measured pulse responses match well with the simulated pulse responses derived from measured s-parameters.

Conclusions

- Equalization of backplane channels is possible with realizable equalizers.
- Equalization of backplane channels is possible with architectures implied in the draft and assumed in related simulations.
- Simulated pulse response based on measured s-parameters is accurate.