

### Signaling Method Performance Results

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### **Presentation Flow**

- Assumptions
- Algorithm approach
- Eye maps
- Conclusions



# Purpose

- Find Equalization For Duobinary and CENRZ For 24 Representative IEEE Channels
- Generate Eye Diagrams
  - Measure Vertical and Horizontal Eye Opening
  - Set Limits and Determine Which Channels Served by Each Method
- Show perspectives on the relative performance of signaling methods
- Determine Which Signaling Method Covers Larger Number of Channels



# Included in Model

- Channel
  - 0.4 pf added at each port (package), not IEEE model
  - 7.5 GHz single pole (Tx shaping)
- Equalization
  - 3-tap FFE least squares fit
  - Up to 5-tap DFE
- Crosstalk
  - NEXT assumed worse case than FEXT
  - 2 Aggressors, randomly phased
    - Choose Worst (Highest SDD21 Magnitude) for Molex, Intel
    - Match Case by Case For Tyco Channels
- Clock Recovery



# Included in Model

- Wideband Noise
  - Added at Receiver
  - Value = 1.46 mV RMS (per IEEE)
- Quantization
  - FFE
    - Duobinary Uses 8 Levels, Range Based on All Channels
    - NRZ Uses 8 Levels, Range Based on All Channels
    - Range for Duobinary is different from range for NRZ
  - DFE
    - 16 Levels Based on Post-Cursor Range For Current Channel
- Jitter
  - DJ of 0.4 UI-pp Added (intent was to compensate for inability to sim RJ)
  - Phase Modulation at 1.1 GHz

### Limitations

- Only 1000 Bits
  - RJ not included
  - Worst case events may not appear
    - Wideband noise
    - Crosstalk
- Iterative Adjustment of FFE and Sample Point Would make results
  more optimistic & typical in actual implementation
- Quantization effects may be larger in actual implementation
- Belief:
  - We feel this evaluation is realistic, balanced and valuable, when viewed in total, given the limitations, assumptions and impairments.



# Math Progression

- Chapter 1 -- Determine Impulse Response of Through Channel.
- Chapter 2 -- Read in Bit Stream, Do Clock Recovery
- Chapter 3 -- Find FFE.
- Chapter 4 -- Find Tx Signal and FFE DC Gain.
- Chapter 5 -- Show FFE-Equalized Bit Streams, Eyes, by Assembling Equalized Impulses.
- Chapter 6 -- Find Quantized Tx FFE Tap Values.
- Chapter 7 -- Repeat (Chap 5) For Comparison.
- Chapter 8 -- Calculate DFE Taps.
- Chapter 9 -- Add DFE to Result of Chap 7, No Jitter.
- Chapter 10 -- Add DFE to Result of Chap 7, With Jitter.
- Chapter 11 -- Generate the Crosstalk.
- Chapter 12 -- Add Wideband Noise.
- Chapter 13 -- Generate the DFE Quantization.
- Chapter 14 -- Repeat Chap 7 With Xtalk, DFE Quantization, Jitter, and Noise.

NOTE: This is not a StatEye simulator



# **Comparison Approach**

- Receiver performance is viewed from a *similar complexity* basis...assuming:
  - 5-tap NRZ DFE is a reasonable complexity bound
  - 3-tap DB DFE and 5-tap NRZ DFE are reasonably similar in complexity



#### **Duobinary 3FFE / 3DFE**



Case1FM13SI20TD13SIL10.s4p
 Case2FM13SI20TD13L10.s4p
 Case3FM13SI20TD6L10.s4p

× Case4FM13Sl20TD13L6.s4p

\* Case5DS1310TD13L6.s4p

• Case6DS1310TD13L6.s4p

+ Case7FM13SI1TD13SIL6.s4p

- FR408\_25in\_sj3k3g3h3\_SPARS\_BD.s4p

- FR408\_25in\_sj3k3g3h3\_SPARS.s4p

1m\_INBOUND/sj3k3g3h3\_SPARS.s4p

peters\_01\_0904\_B1\_thru.s4p

peters\_01\_0904\_B20\_thru.s4p

× peters\_01\_0904\_B32\_thru.s4p

x peters\_01\_0904\_M1\_thru.s4p

peters\_01\_0904\_M20\_thru.s4p

+ peters\_01\_0904\_M32\_thru.s4p

- peters\_01\_0904\_T1\_thru.s4p

- peters\_01\_0904\_T20\_thru.s4p

peters\_01\_0904\_T32\_thru.s4p

T1\_Synth\_Causal

peters\_01\_0904\_B12\_thru.s4p

× peters\_01\_0904\_M12\_thru.s4p

x peters\_01\_0904\_T12\_thru.s4p

XILINX

• 0

+ 0

SPEC BOUNDS

#### NRZ 3FFE / 5DFE



 Case1FM13SI20TD13SIL10.s4p Case2FM13SI20TD13L10.s4p Case3FM13SI20TD6L10.s4p × Case4FM13Sl20TD13L6.s4p \* Case5DS1310TD13L6.s4p Case6DS1310TD13L6.s4p + Case7FM13SI1TD13SIL6.s4p - FR408 25in sj3k3g3h3 SPARS BD.s4p - FR408 25in sj3k3g3h3 SPARS.s4p 1m INBOUND/sj3k3g3h3 SPARS.s4p peters 01 0904 B1 thru.s4p peters 01 0904 B20 thru.s4p × peters\_01\_0904\_B32\_thru.s4p x peters 01 0904 M1 thru.s4p peters 01 0904 M20 thru.s4p + peters 01 0904 M32 thru.s4p - peters 01 0904 T1 thru.s4p - peters\_01\_0904\_T20\_thru.s4p • peters\_01\_0904\_T32\_thru.s4p T1 Synth Causal ▲ peters 01 0904 B12 thru.s4p × peters 01 0904 M12 thru.s4p x peters\_01\_0904\_T12\_thru.s4p • 0 +0

S. XILI

- SPEC BOUNDS





Case1FM13SI20TD13SIL10.s4p

# General Eye Shapes vs. Trajectory

• Diagram of d-horiz / d-vert for an eye



### **DB3 to NRZ5 Trajectories**





#### **DB3 to NRZ5 Trajectory Deltas**



Case2FM13SI20TD13L10.s4p Case3FM13SI20TD6L10.s4p Case4FM13SI20TD13L6.s4p Case6DS1310TD13L6.s4p - FR408 25in sj3k3g3h3 SPARS BD.s4p FR408 25in sj3k3g3h3 SPARS.s4p 1m INBOUND/sj3k3g3h3 SPARS.s4p peters 01 0904 B1 thru.s4p peters 01 0904 B20 thru.s4p peters 01 0904 B32 thru.s4p ----- peters 01 0904 M20 thru.s4p peters 01 0904 M32 thru.s4p ---- peters 01 0904 T1 thru.s4p peters\_01\_0904\_T20\_thru.s4p — peters\_01\_0904\_T32\_thru.s4p \_\_\_\_ peters 01 0904 B12 thru.s4p **——0** -+-00

XILIN









#### NRZ5 Degradation due to Jitter, Xtalk





![](_page_20_Figure_0.jpeg)

![](_page_21_Figure_0.jpeg)

### Conclusions

- Long stubs are an obstacle
- NRZ serves more channels than Duobinary
  - The unsolved channels are important market applications
  - Some channel improvements are possible that are compatible with High Volume Manufacturing techniques
  - Further improvements should be considered for both signaling and channel in order to solve these important channels
- IEEE 802.3ap should be moved forward based on this and other data

![](_page_22_Picture_7.jpeg)

![](_page_23_Picture_0.jpeg)

### **Appendix Slides**

### **Channel List**

Case1FM13SI20TD13SIL10.s4p
Case2FM13SI20TD13L10.s4p
Case3FM13SI20TD6L10.s4p
Case4FM13SI20TD13L6.s4p
Case5DS1310TD13L6.s4p
Case6DS1310TD13L6.s4p
Case7FM13SI1TD13SIL6.s4p
FR408_25in_sj3k3g3h3_SPARS_BD.s4p
FR408_25in_sj3k3g3h3_SPARS.s4p
1m_INBOUND/sj3k3g3h3_SPARS.s4p
peters_01_0904_B1_thru.s4p
peters_01_0904_B20_thru.s4p
peters_01_0904_B32_thru.s4p
peters_01_0904_M1_thru.s4p
peters_01_0904_M20_thru.s4p
peters_01_0904_M32_thru.s4p
peters_01_0904_T1_thru.s4p
peters_01_0904_T20_thru.s4p
peters_01_0904_T32_thru.s4p
T1_Synth_Causal
peters_01_0904_B12_thru.s4p
peters_01_0904_M12_thru.s4p
peters 01 0904 T12 thru.s4p

![](_page_24_Picture_2.jpeg)