IEEE 802.3ap Codes Comparison for 10G Backplane System

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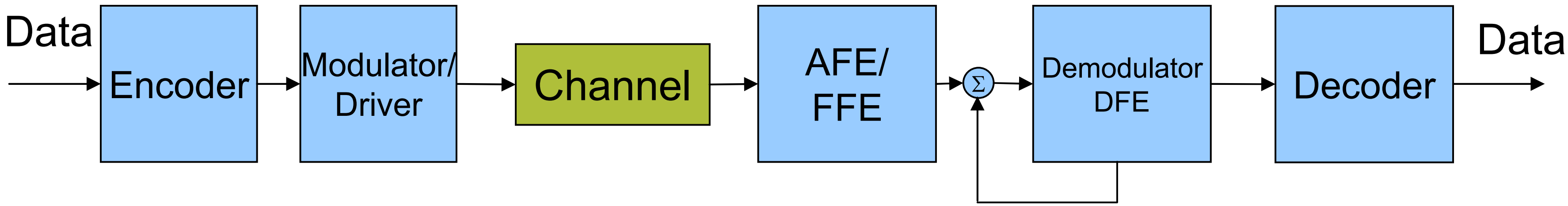
Presentation goal

- The goal of this presentation is to compare Forward Error Correction (FEC) codes performance for 10G serial system.
- Contents:
  - System considerations
  - Comparison table and graphs
  - BCH and RS code introduction
  - Convolution code introduction

System considerations

- Vast assortment of error correcting codes exists
- Focus on proper codes according to system requirements
- System considerations
  - Required BER 10^{-12} - 10^{-15}
  - Simple line codes - NRZ, duobinary, PR4
  - Do not increase baud rate significantly
  - The decoder input BER assumed order of 10^{-4} - 10^{-8}
    - Shall be defined
    - Impacts code selection
  - Noise – discussed in the next slide
  - Latency, complexity – code dependent – comparison parameters
- **Comparing following Error Correction Codes**
  - Binary BCH or other cyclic codes
  - Reed Solomon (RS) Code
  - Punctured Convolution Code

Transmitter/Receiver block scheme



- System performance limited by
  - jitter
  - analog part non-linearity
  - ISI
  - arithmetic precision errors
  - DFE error propagation
- Not classical AWGN channel
- The noise may not be white

Code characteristics summary (1)

10.3125 GHz Data rate	Code rate	Symbol rate [GHz]	Latency[1]	Complexity	Input BER for 10^{-15}	Receiver Eb/No[2] For 10^{-15}
BCH	(1023,893)	11.81	1023 bits 86.6ns	Order of 30Kgates	$7 * 10^{-4}$	7.7dB
RS	(160,140)	11.79	160 Bytes 108.6ns	Order of 30Kgates	$2 * 10^{-4}$	8.4dB
BCH	(255,223)	11.79	255 bits 31ns	Order of 10Kgates	$2 * 10^{-5}$	9.8dB
Conv.	7/8	11.79	100 Bits 8.48ns	Order of 30Kgates	$2 * 10^{-6}$	10.8dB
BCH	(1023,923)	11.43	1023 bits 89.5ns	Order of 30Kgates	$3 * 10^{-4}$	8.1dB
RS	(200,180)	11.46	200 Bytes 139.6 ns	Order of 40Kgates	$2 * 10^{-4}$	8.5dB
RS	(100,90)	11.46	100 Bytes 69.8ns	Order of 25Kgates	$2 * 10^{-5}$	9.7dB
BCH	(255,231)	11.38	255 bits 32ns	Order of 10Kgates	$4 * 10^{-6}$	10.5dB
Conv.	9/10	11.46	140 bits 12.2ns	Order of 35Kgates	$1.5 * 10^{-6}$	10.8dB

Code characteristics summary(2)

10.3125 GHz Data rate	Code rate	Symbol rate [GHz]	Latency[1]	Complexity	Input BER for 10^{-15}	Receiver Eb/No[2] For 10^{-15}
BCH	(1023,943)	11.19	1023 bits 91.4ns	Order of 30Kgates	$1.5 * 10^{-4}$	8.5dB
RS	(255,235)	11.19	255 Bytes 182.3ns	Order of 40Kgates	$1.5 * 10^{-4}$	8.5dB
RS	(130,120)	11.17	130 Bytes 93.1ns	Order of 30Kgates	$1.5 * 10^{-5}$	9.7dB
Conv.	12/13	11.17	160 bits 14.3ns	Order of 40Kgates	10^{-6}	10.8dB
BCH	(255,239)	11.0	255 bits 33ns	Order of 10Kgates	$3 * 10^{-7}$	11.25dB

Note (1) – Decoder processing latency should be added for RS and BCH.
The decoder processing latency is implementation specific
and may vary from tens to hundreds bits.

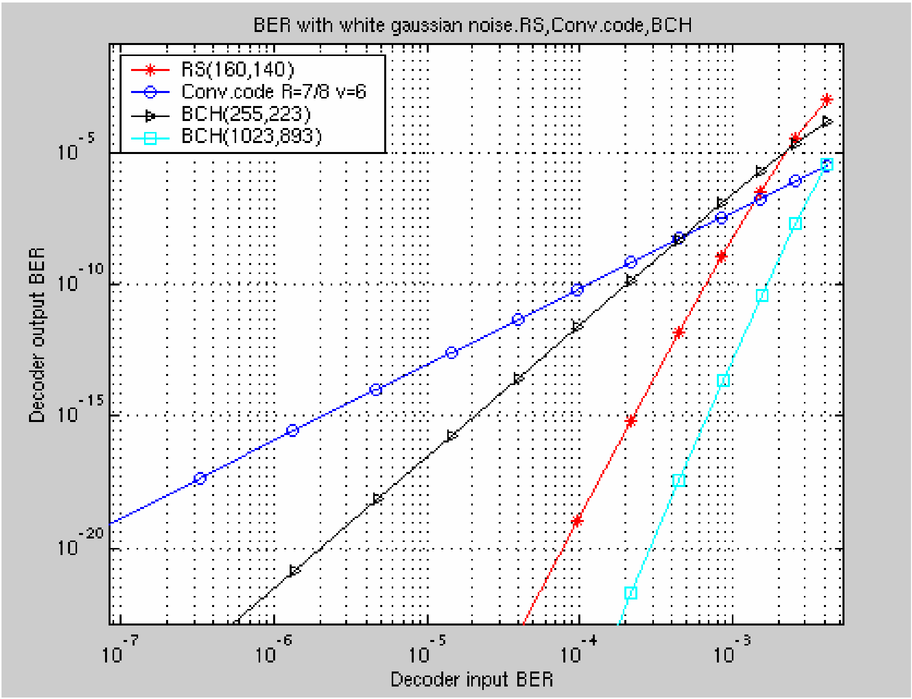
Note (2) – BER is calculated for NRZ and AWGN channel. Uncoded Eb/No presented.

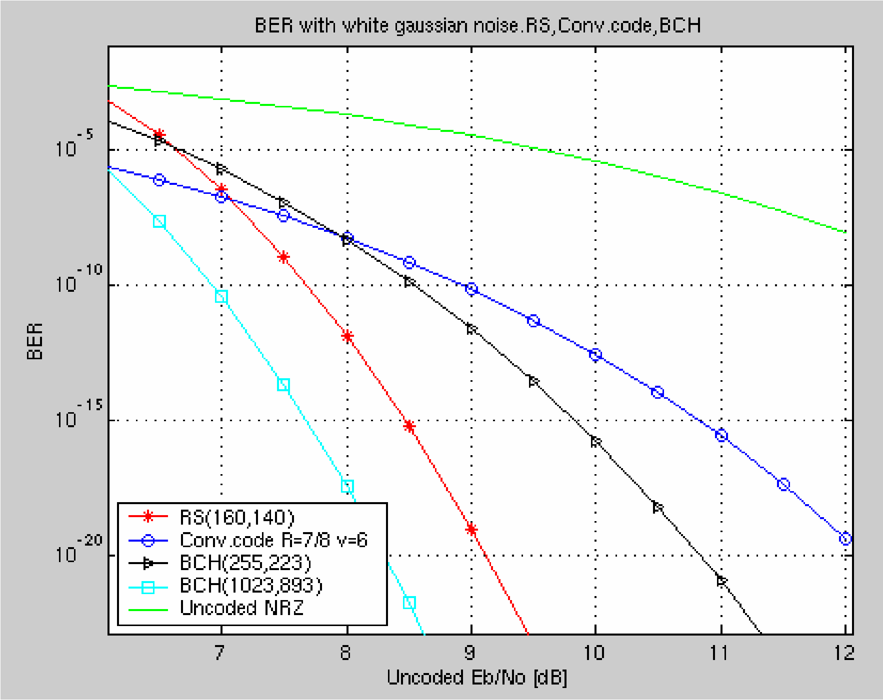
Additional code properties

RS, BCH	Convolutional code
Hard Decision	Soft Decision
RS corrects error bursts up to the (n-k)/2 bytes. BCH corrects bursts up to the 2-13 bits depending on code	Viterbi decoder degrades for error bursts
RS and BCH are not sensitive to the noise distribution as long the number of errors less than threshold.	Viterbi decoder optimized for AWGN

Code performance graphs (1)

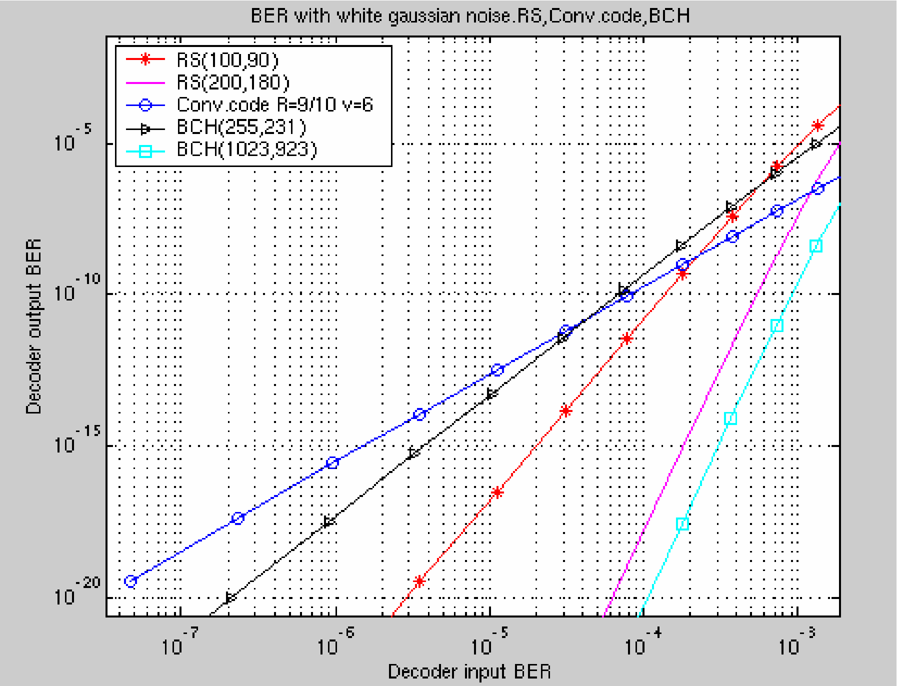
BCH(255,223), BCH(1023,893)
RS (160,140),
Convolution code R=7/8, ν=6

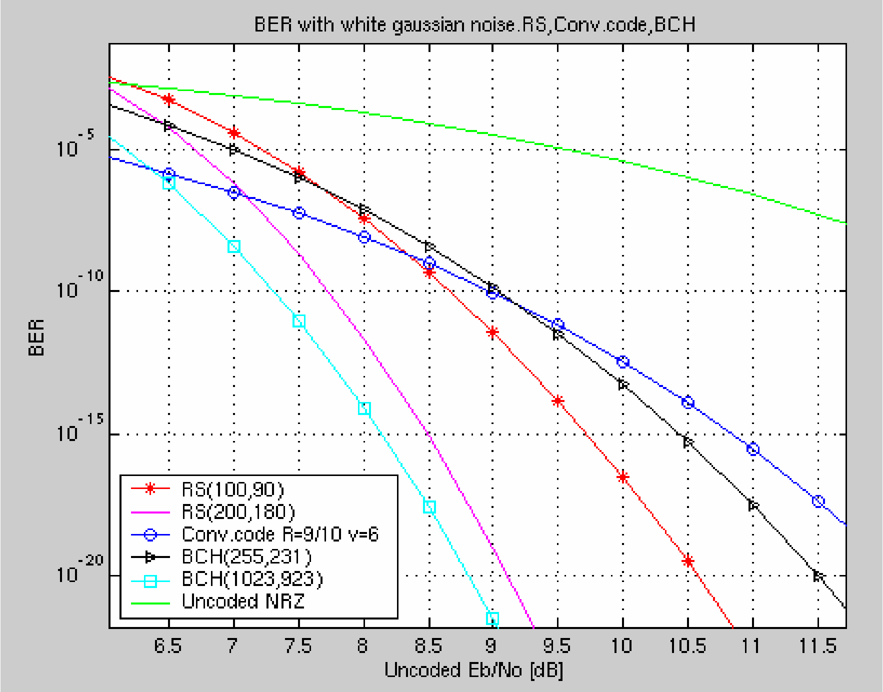




Code performance graphs (2)

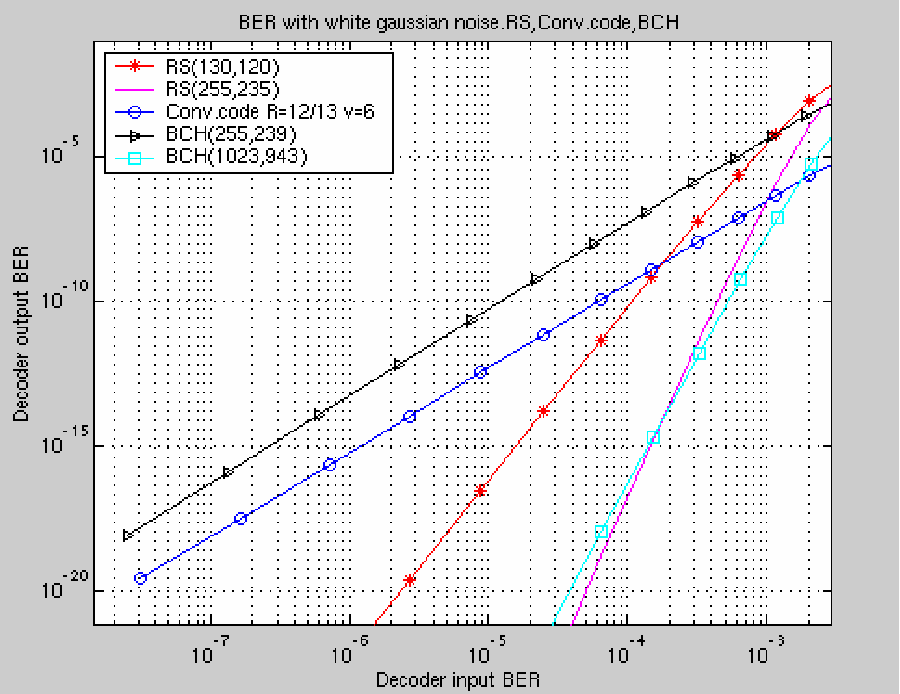
BCH(255,231),BCH(1023,923)
RS (100,90), RS (200,180),
Convolution code R=9/10, ν=6

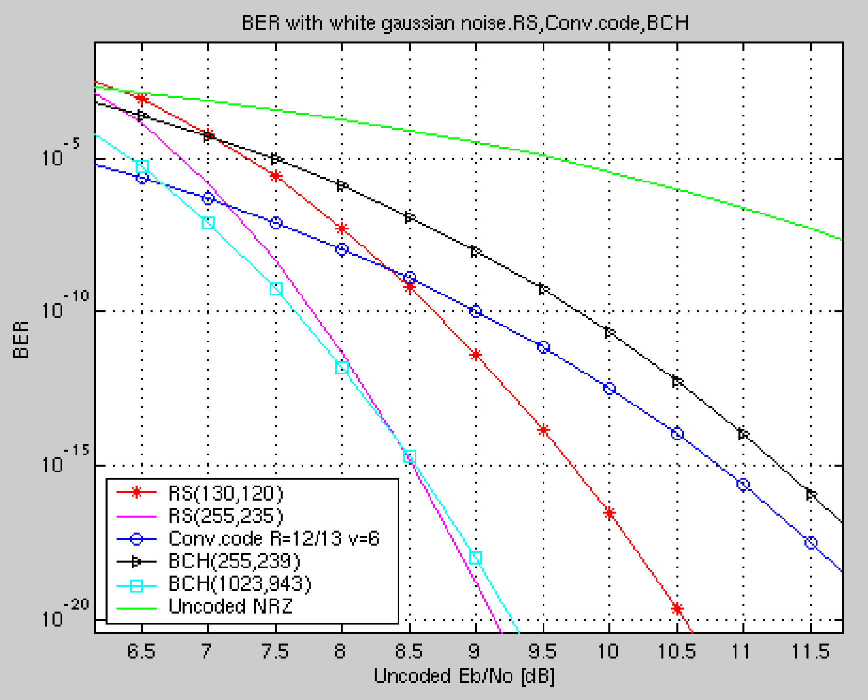




Code performance graphs (3)

BCH(255,239), BCH(1023,943)
RS (130,120), RS (255,235),
Convolution code R=12/13, ν=6





Summary

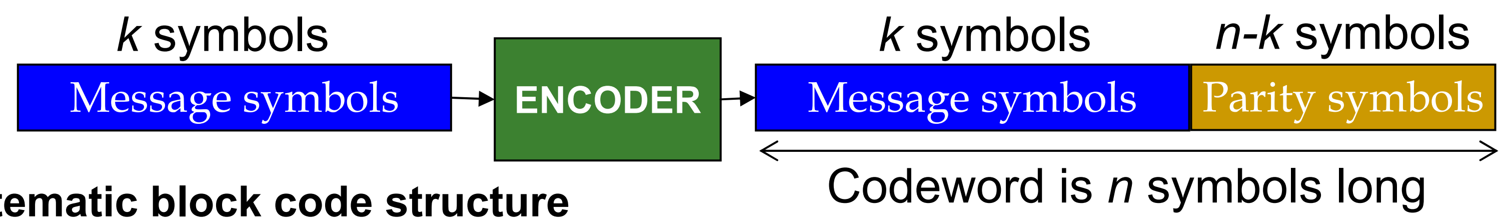
- Code selection dependent on system parameters
  - Latency
  - Complexity
  - Decoder input BER
- RS or BCH codes seems to be best candidates.
- Convolutional code requires high resolution ADC and means to deal with bursts (interleaving)

Input BER of 10^{-4}	→	RS(255,235) BCH(1023,943)
Input BER of 10^{-6}	→	BCH(255,231)
Latency limit of 200ns	→	RS(255,235) BCH(1023,943)
Latency limit of 50ns	→	BCH(255,223) BCH(255,231)

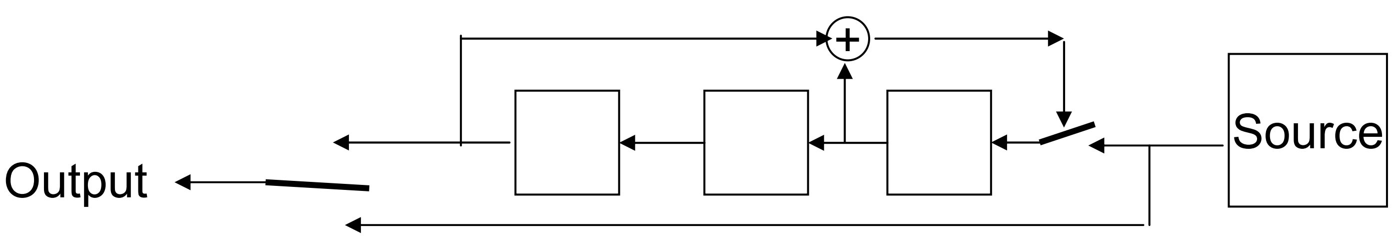
Brief codes introduction

BCH codes including Reed Solomon

- Systematic cyclic linear block code
  - Binary codes or non binary codes like Reed-Solomon
- Consists of data bits (bytes) and parity bits (bytes)
  - n – number of codeword symbols
  - k – number of data symbols
- The code generated using shift register XORed output
- No Latency in the encoder
- Inherent latency of one block in the decoder



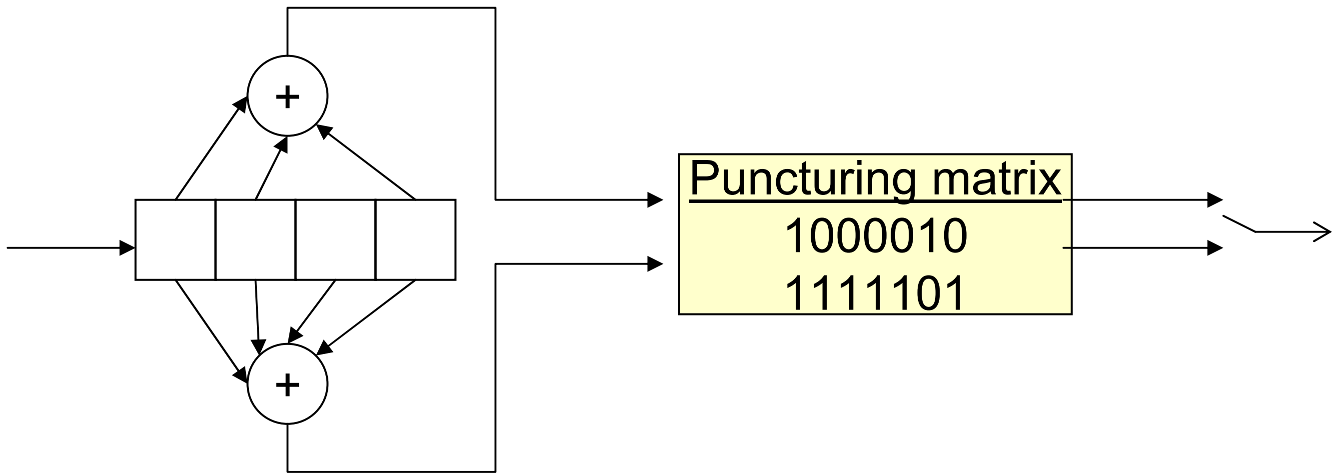
Systematic block code structure



BCH shift register encoder example

Punctured convolution code

- Based on R=1/2 convolution code
- Some of encoder output bit deleted creating R=(n-1)/n code.
- Practical encoder shift register may have length $\nu+1$ between $\nu=2$ to $\nu=6$
- Decoded using Viterbi algorithm
- Punctured code truncation path length **L** longer than for the original R=1/2 code



R=7/8 Convolution encoder, based on R=1/2 ν=3, (15,17) code

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