

Comparison of Signaling and Equalization Schemes NRZ, Duobinary, and PR4

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High Speed Interface Systems Architecture

LSI Logic



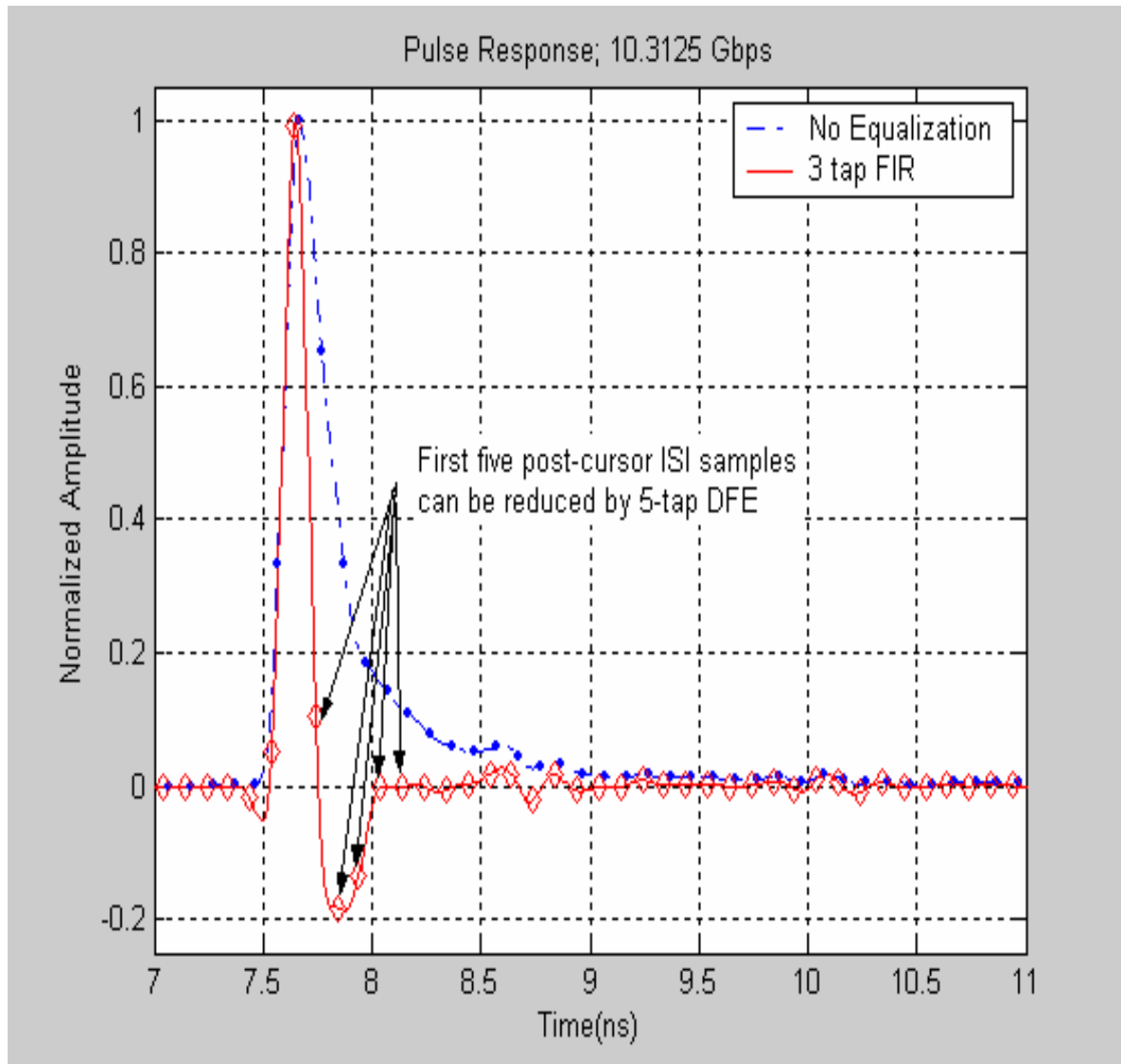
Introduction

- Overview of signaling schemes
 - NRZ, Duobinary, and PR4
- Review of simulator and parameters
- Presentation of results

NRZ, Duobinary, and PR4 Overview

NRZ Signaling

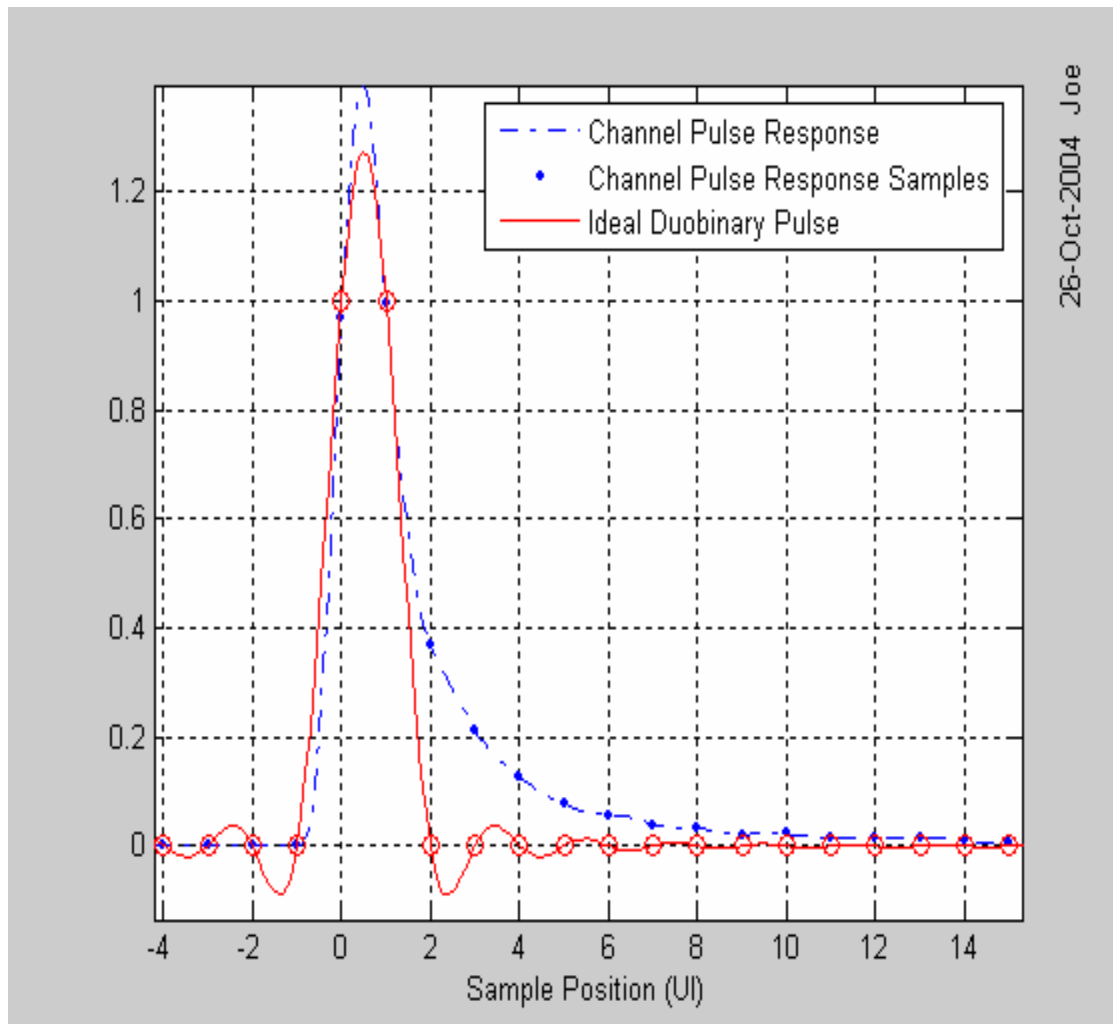
Trying to Removing All ISI Through Equalization



- Our primary equalization goal has been to eliminate intersymbol interference (ISI).
- A combination of a TX FIR filter and a DFE in the Rx are used to mitigate the ISI.
- The goal of removing ISI is to make detection possible with a reasonable complexity.

Duobinary

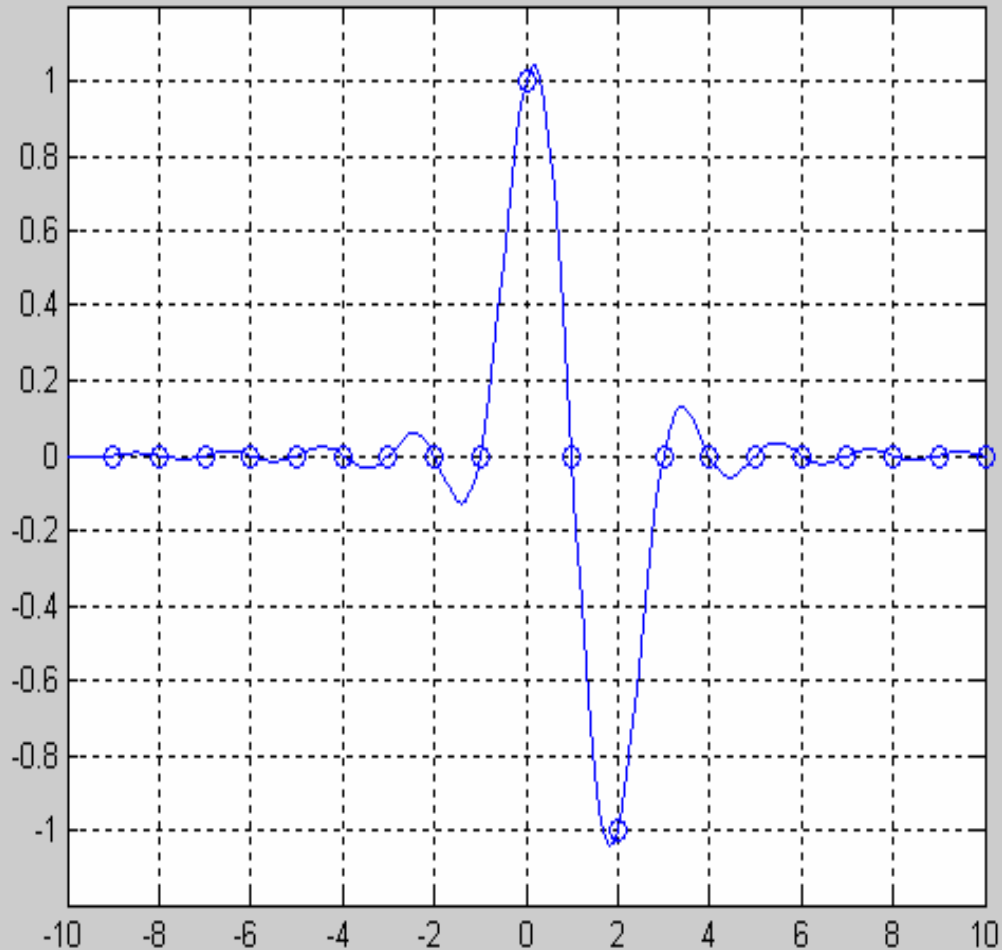
Ideal versus Channel Pulse Response



- 1+D Channel
 - Samples at
 - time 0 and 1 are 1
 - 0 everywhere else.
- Appears to be a reasonable fit for channels at this data rate.

Partial Response – Class IV

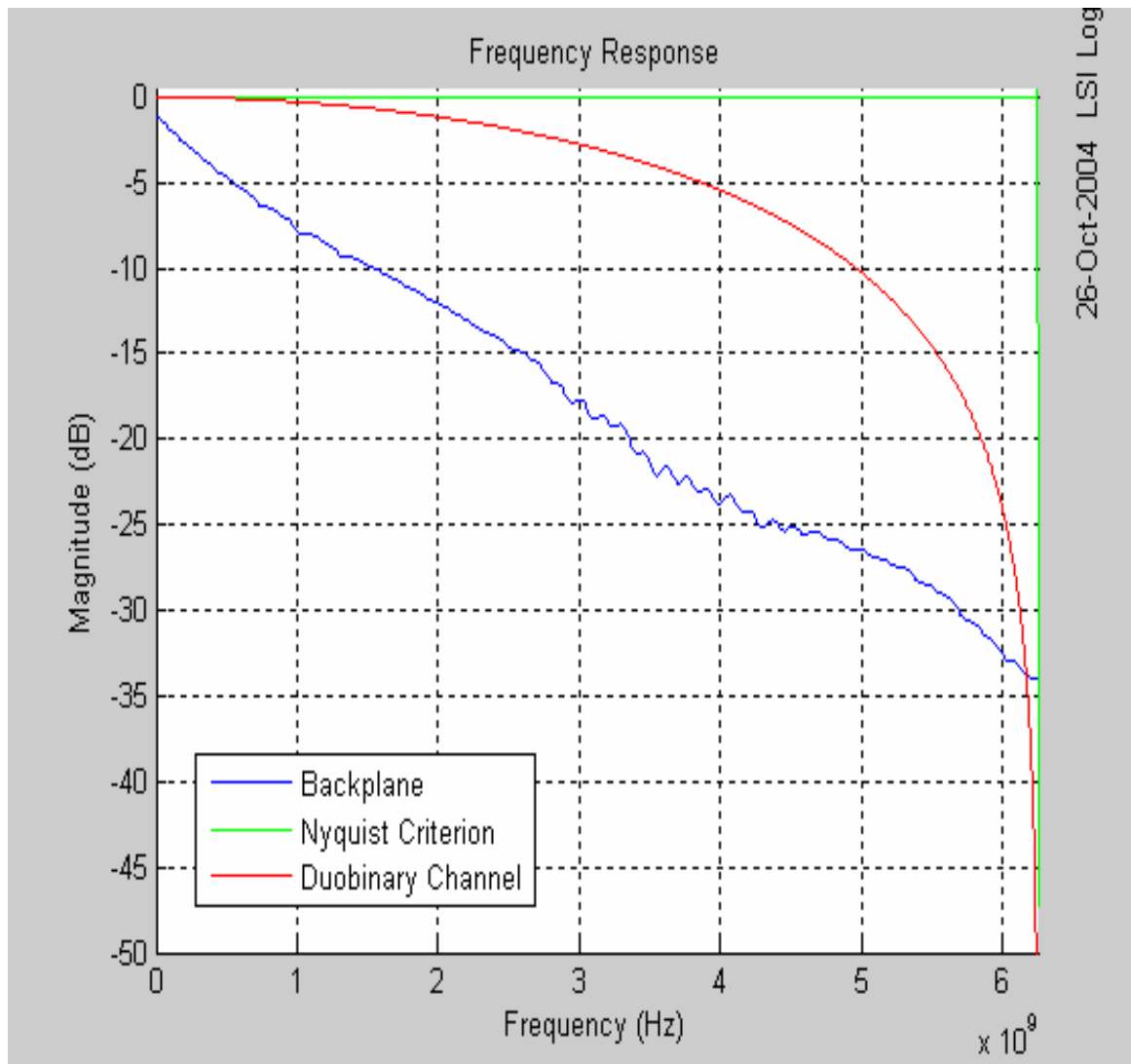
Pulse Response



- Does not resemble our channel pulse response.

Frequency Response Comparison

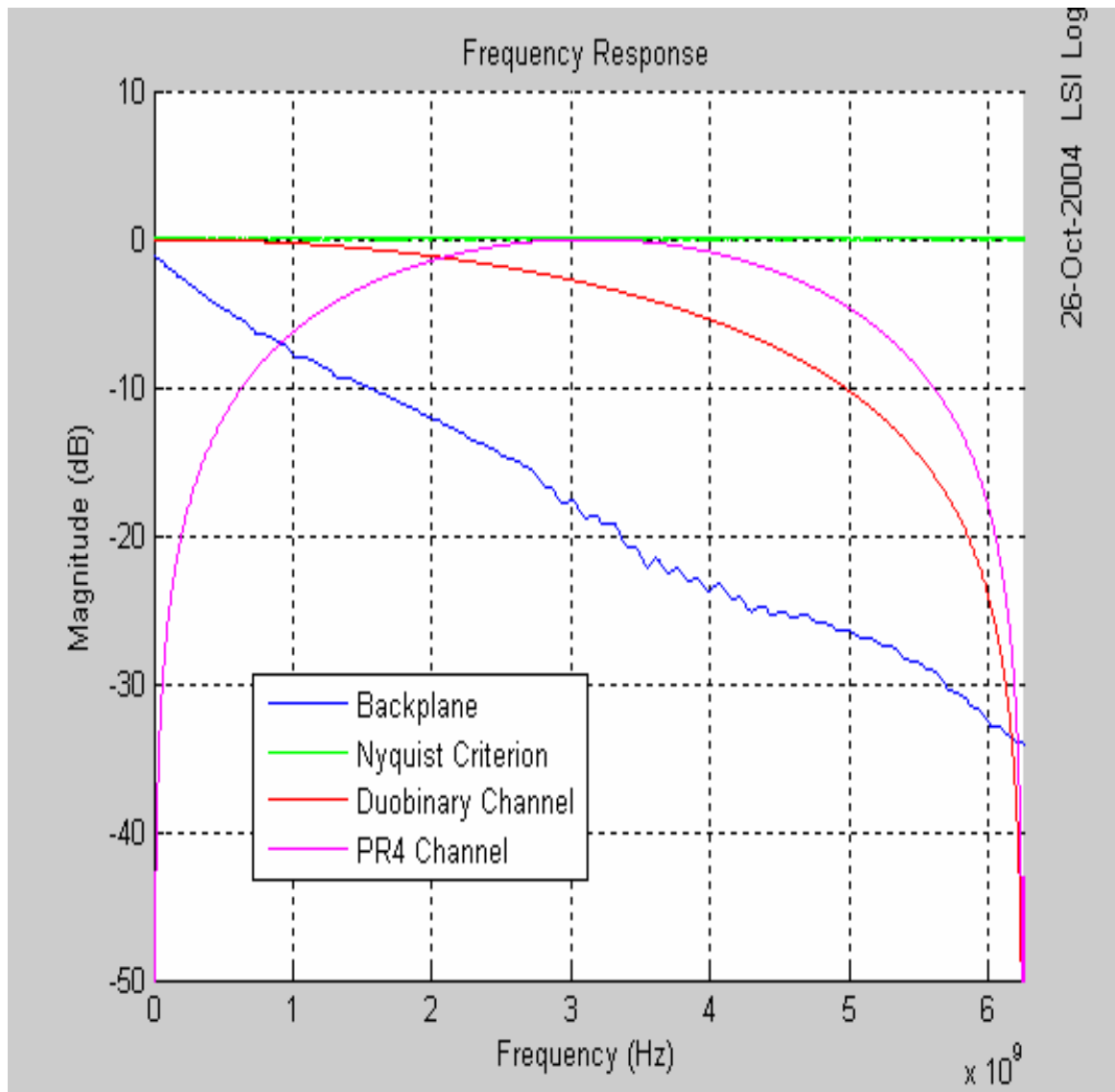
NRZ and Duobinary



- Ideal NRZ equalization target is flat spectrum.
- NRZ requires a lot of high frequency boost.
- Duobinary's 1+D equalization target has a null at the Nyquist frequency. It is a better match to the channel at high frequencies and consequently requires less high frequency boost.

Frequency Response Comparison

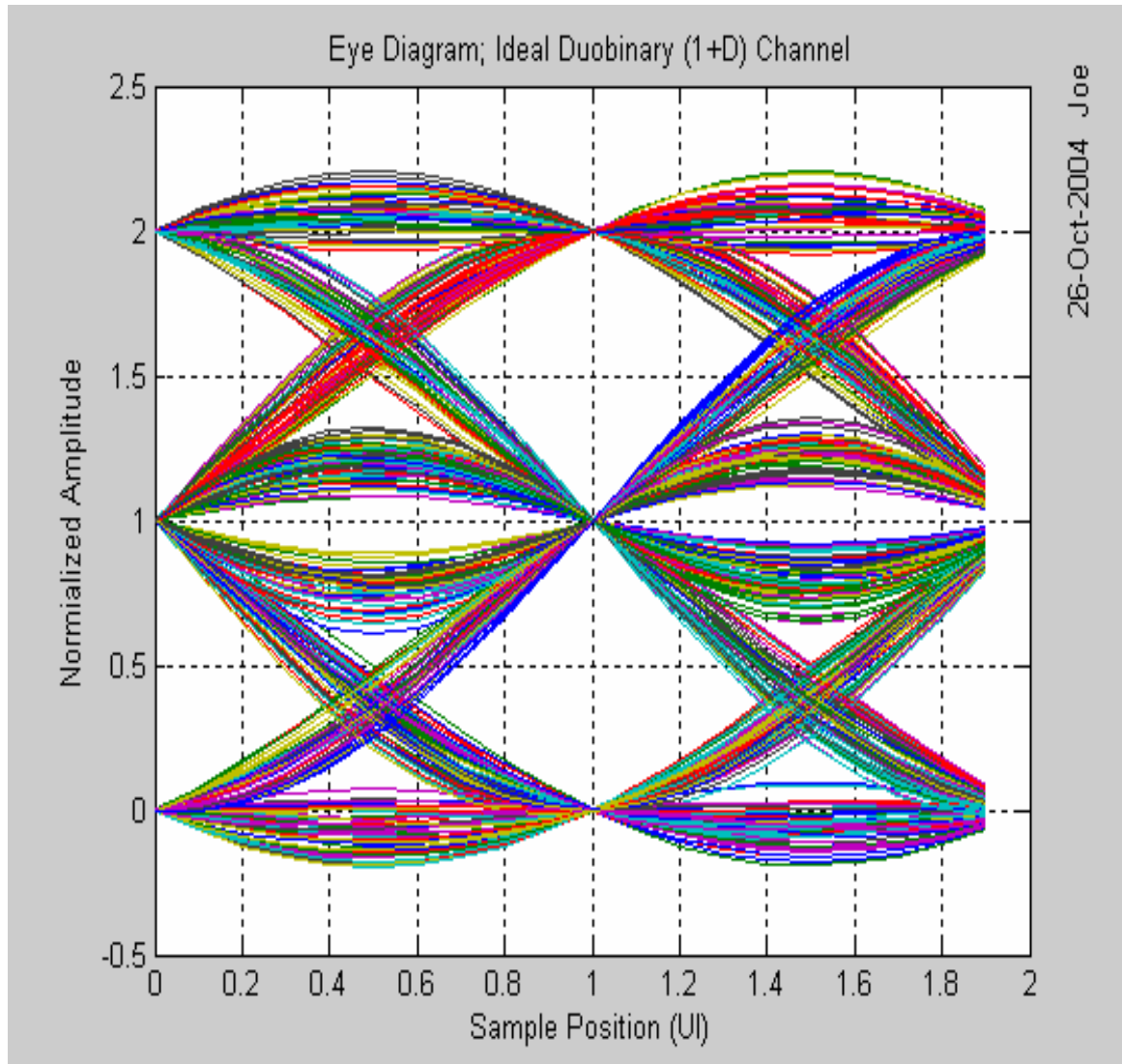
NRZ, Duobinary, and PR4



- Has nulls at both DC and Nyquist
- Null at DC may match DC-null in AC coupled systems, but PR-4's DC null is much deeper.
- Equalizing to PR4 results in throwing away the signal in the low frequency range where the SNR is strongest.

Duobinary

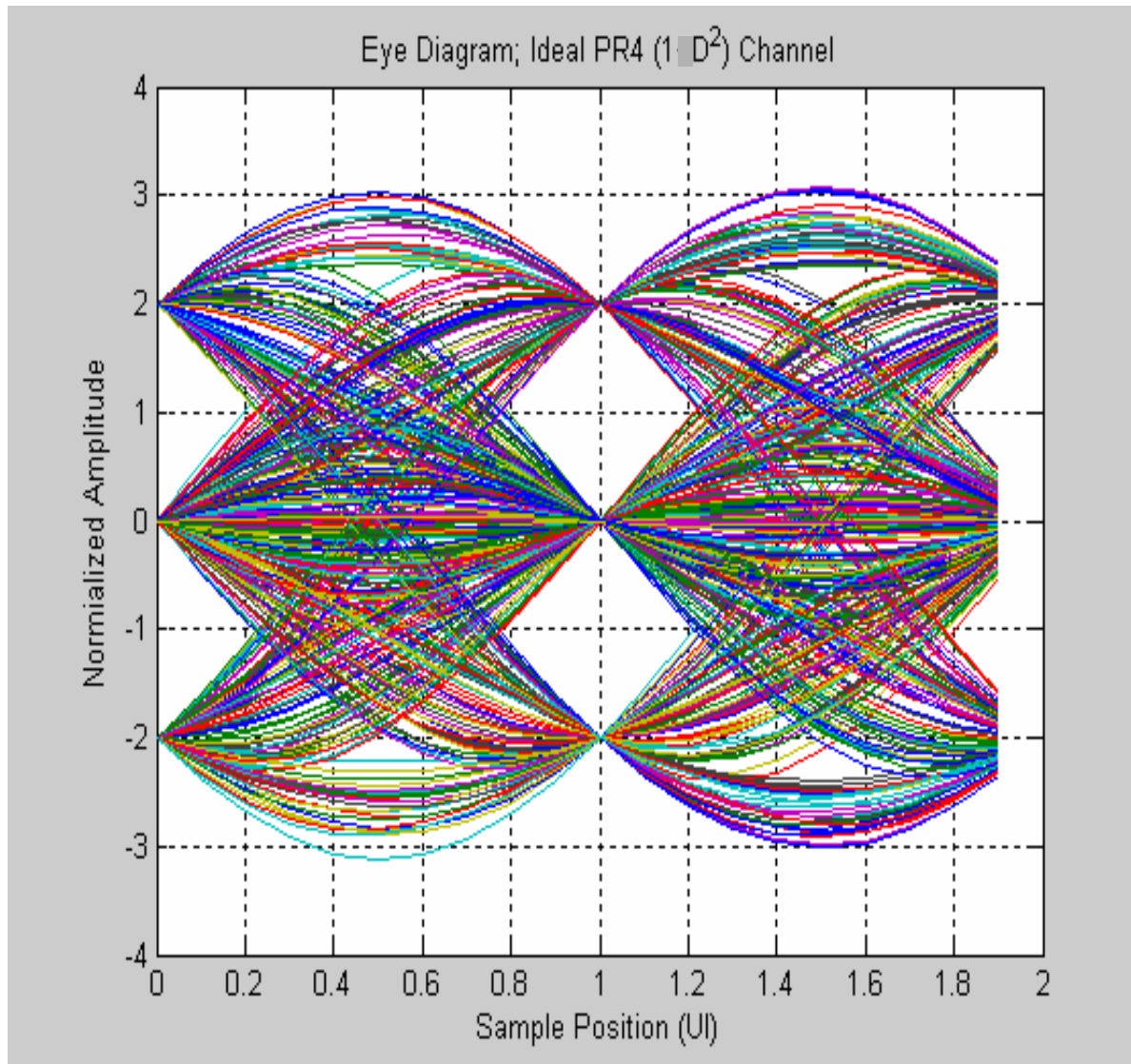
Ideal Eye Diagram



- No transitions from highest to lowest signal levels in adjacent bits.
- Notice that slicer value that results in highest jitter tolerance is not the slicer level that results in best noise tolerance.

PR4

Eye Diagram

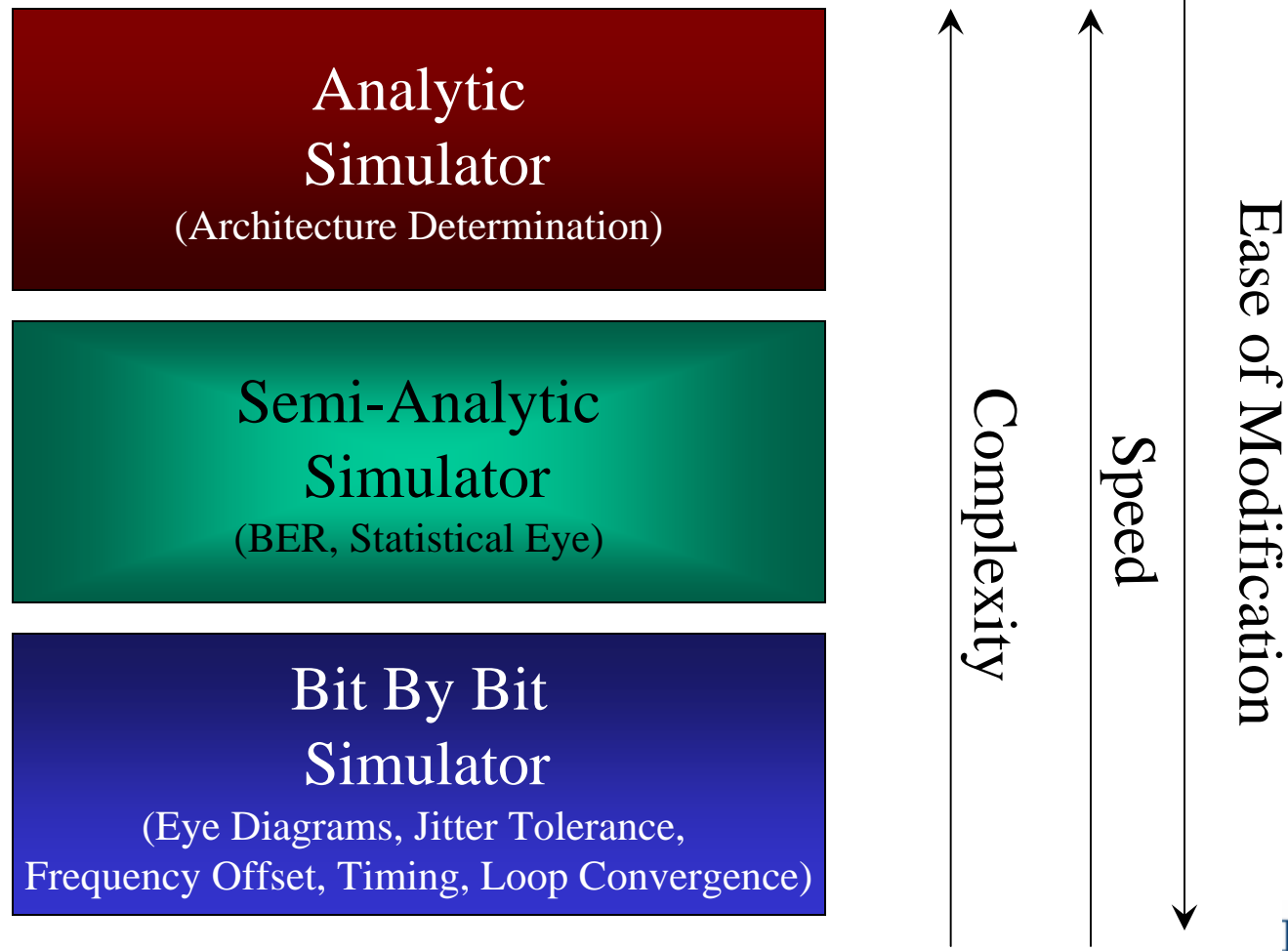


- Horizontal eye opening in ideal eye diagram is reduced compared to $1+D$ target.
- Any signal level can transition to any other signal level in adjacent bit.
- Even in ideal case, without MLSD, eye exhibits very little tolerance to jitter.

Simulator Review

Three System Modeling Approach

Three System Model Approach



Analytic Model

- Includes
 - Intersymbol Interference
 - Tx Jitter
 - Electronics (White) Noise
 - Crosstalk
- Does Not Include
 - Receiver Sensitivity
 - Duty Cycle Distortion
 - Other Sources of DJ

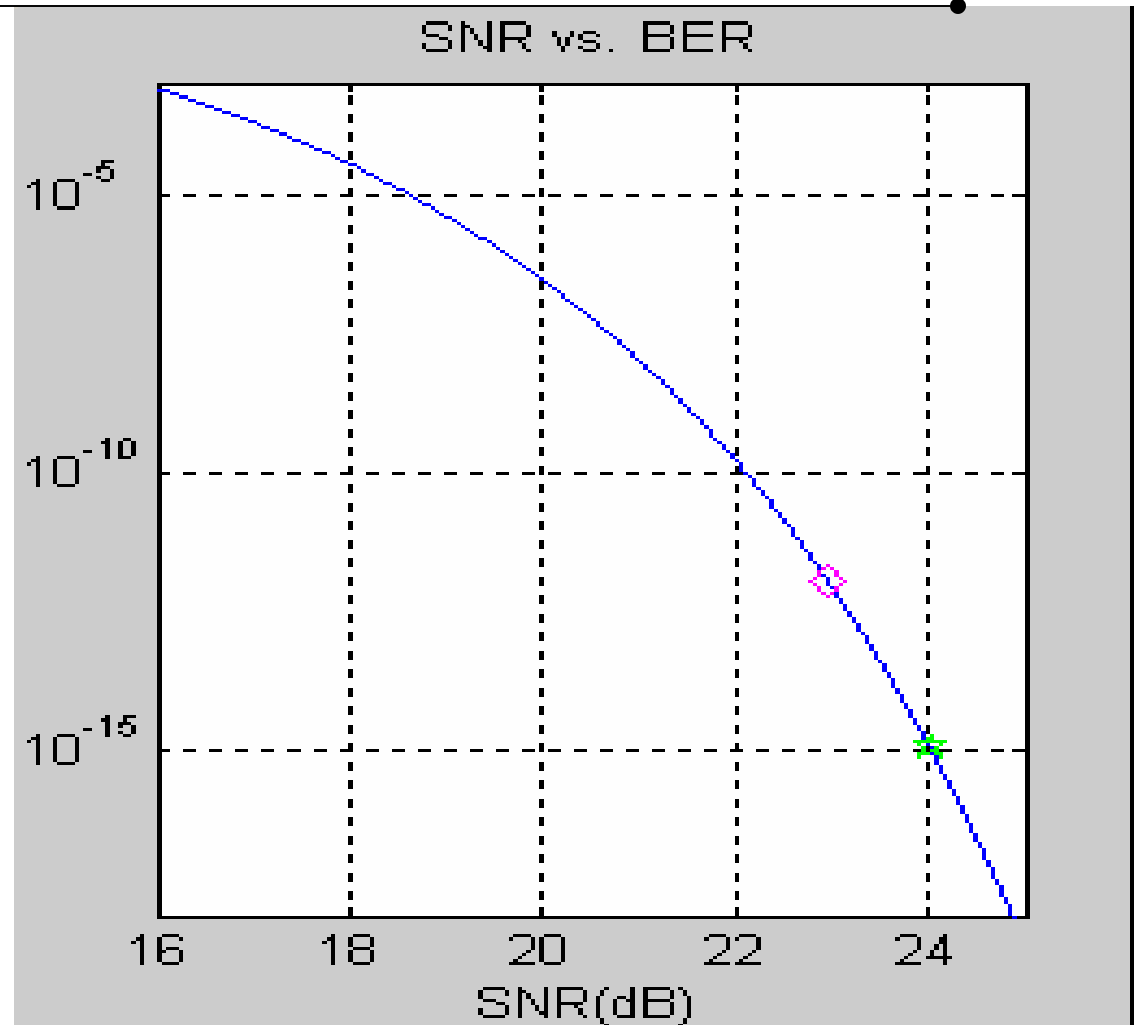
Required SNR

SNR Required at Slicer for 10^{-15} BER

$$SNR = \frac{d_{\min}^2}{\sigma^2}$$

$$Pr_{err} \approx \frac{1}{2} \operatorname{erfc} \left(\frac{\sqrt{SNR}}{2\sqrt{2}} \right)$$

- Approximately 24dB is required for an error rate of 10^{-15}



Overview of Simualtions

- Equalization architectures with a linear FIR feedforward (FF) filter in the TX, and a decision feedback (FB) equalizer in the Rx are compared.
- The number of taps in the feedforward and feedback equalizers are varied.
- The effect of one near-end crosstalk aggressor is considered.
 - With Tyco and Intel data sets, worst case NEXT corresponding to that data set is used.
 - With Molex and Xilinx data sets, modeled NEXT from Anderson is used.
- A simple RC model with pole at $0.75 \times \text{baud rate}$ is used for the transmitter.
- Mellitz capacitor-like package model included on both transmitter and receiver.

Parameters Used

- Only DJ is from ISI
 - No DCD, PJ included
- $0.010UI \sigma$ RJ added
 - Not more than 13.4ps peak-to-peak RJ at 8.5Gbps data rate with probability $1-10^{-12}$
 - Not more than 15.6ps peak-to-peak RJ max at 8.5Gbps data rate with probability $1-10^{-15}$
- Signal-To-Electronics Noise Ratio 45dB
- Crosstalk added as noted
- Ideal receiver sensitivity assumed

Description of Results

- SNR at optimal sampling point is shown. No measurement of horizontal eye opening is presented.
- x-axis shows number of feedback taps used
- Each line represents a different number of feed-forward (FF) equalizer taps used in the TX
- Each color represents a different signaling scheme.
- Crosstalk is assumed to occur at the same frequency as the signal. The worst case crosstalk phase at the ideal sampling point is selected.
- All tap values are ideal.

Summary of Results

SNR Comparison

Intel Backplanes

BP	NRZ 3FF+5DFE	DB 3FF+3DFE	DB 3FF+5DFE	DB 4FF+3DFE	DB 4FF+5DFE	PR4 3FF+3DFE	PR4 3FF+5DFE	PR4 5FF+3DFE	PR4 5FF+5DFE
Intel B1	25.75	23.7428	24.7189	23.8904	24.7194	10.02	10.5355	21.9916	22.148
Intel B12	25.4387	20.6647	24.2936	24.0673	25.5312	11.8722	12.9072	22.9701	23.5763
Intel B20	24.421	17.9337	21.4678	24.1036	24.7867	12.5534	13.6077	22.137	22.9709
Intel M1	24.2043	21.3843	21.8428	21.3882	22.1214	13.6615	14.3548	19.2269	20.565
Intel M20	24.2586	18.8378	20.1773	21.8866	22.3897	16.7028	17.1796	21.0436	21.0448
Intel T1	21.862	19.6715	20.0462	19.685	20.1262	11.684	11.8187	17.7951	19.4143
Intel T12	21.3521	17.8295	20.2168	18.696	20.4783	13.8084	15.0696	18.1711	18.9188
Intel T20	20.4595	16.3257	19.0451	18.4427	19.7304	14.0649	15.2461	17.3062	18.2698



SNR Comparison

Tyco Backplanes

BP	NRZ 3FF+5DFE	DB 3FF+3DFE	DB 3FF+5DFE	DB 4FF+3DFE	DB 4FF+5DFE	PR4 3FF+3DFE	PR4 3FF+5DFE	PR4 5FF+3DFE	PR4 5FF+5DFE
Tyco 1	26.4184	15.5579	18.0878	25.3081	25.3752	13.7218	15.3615	23.1624	23.6852
Tyco 2	26.7208	15.4417	17.8542	15.4474	17.8549	13.6503	15.4245	13.6559	15.4302
Tyco 3	24.7924	14.7412	17.0261	24.4904	24.6559	13.0619	14.8896	22.4596	23.1564
Tyco 4	27.3838	16.7213	19.9583	25.8848	26.1496	14.6765	16.383	23.8066	24.8202
Tyco 5	28.8032	20.5003	23.6176	27.3431	27.896	15.9264	17.4989	25.2065	26.7141
Tyco 6	25.4634	19.9357	22.3319	23.3344	24.3991	15.6349	17.0529	21.6006	23.0806
Tyco 7	26.6822	23.394	25.8662	23.7112	26.0652	16.9793	17.5009	22.5142	24.2921

SNR Comparison

Molex and Xilinx Backplanes

BP	NRZ 3FF+5DFE	DB 3FF+3DFE	DB 3FF+5DFE	DB 4FF+3DFE	DB 4FF+5DFE	PR4 3FF+3DFE	PR4 3FF+5DFE	PR4 5FF+3DFE	PR4 5FF+5DFE
MoL ex i2	24.809	17.1815	18.9193	23.3004	23.8805	14.9248	16.8129	21.4513	22.3848
MoL ex i3	24.7216	16.4369	18.7943	23.0948	23.7304	14.0673	15.9244	21.3092	22.3042
MoL ex i4	24.635	16.8023	18.7352	23.0507	23.7563	14.504	16.5218	20.9664	22.278
MoL ex i5	24.9085	16.0529	18.9518	23.5529	23.9459	13.7286	15.6399	21.5105	22.4099
Mole x o2	25.224	17.5415	19.1214	23.9419	24.2682	15.4785	17.0011	22.3036	22.683
Mole x o3	25.0651	16.75	18.8106	23.6832	24.0728	14.586	16.1901	22.0329	22.4956
Mole x o4	25.1958	17.2071	18.9993	23.9024	24.2266	15.1239	16.7727	22.1454	22.6515
Mole x o5	25.2929	17.2958	19.1175	24.1252	24.3047	15.3704	16.9238	22.3191	22.6489
Ande rson	23.6875	15.3596	18.3673	22.8244	22.9803	13.3333	15.2358	20.2191	21.0405



Required Number of DFE Taps

To Achieve 24dB SNR

Tyco Backplanes

BP	NRZ	DB	PR4
	3 tap FF	4 tap FF	5 tap FF
Tyco 1	≤ 1	3	6
Tyco 2	≤ 1	20	100
Tyco3	3	3	10
Tyco4	≤ 1	2	4
Tyco 5	≤ 1	≤ 1	≤ 1
Tyco 6	4	4	30



Required Number of DFE Taps

To Achieve 24dB SNR

Intel Backplanes

BP	NRZ	DB	PR4
	3 tap FF	4 tap FF	5 tap FF
Intel B1	3	4	8
Intel B12	4	3	6
Intel B20	4	3	8
Intel M1	4	6	10
Intel M20	5	20	20
Intel T1	10	20	20
Intel T12	100	100	>100
Intel T20	>100	>100	>100



Required Number of DFE Taps

To Achieve 24dB SNR

Molex and Xilinx Backplanes

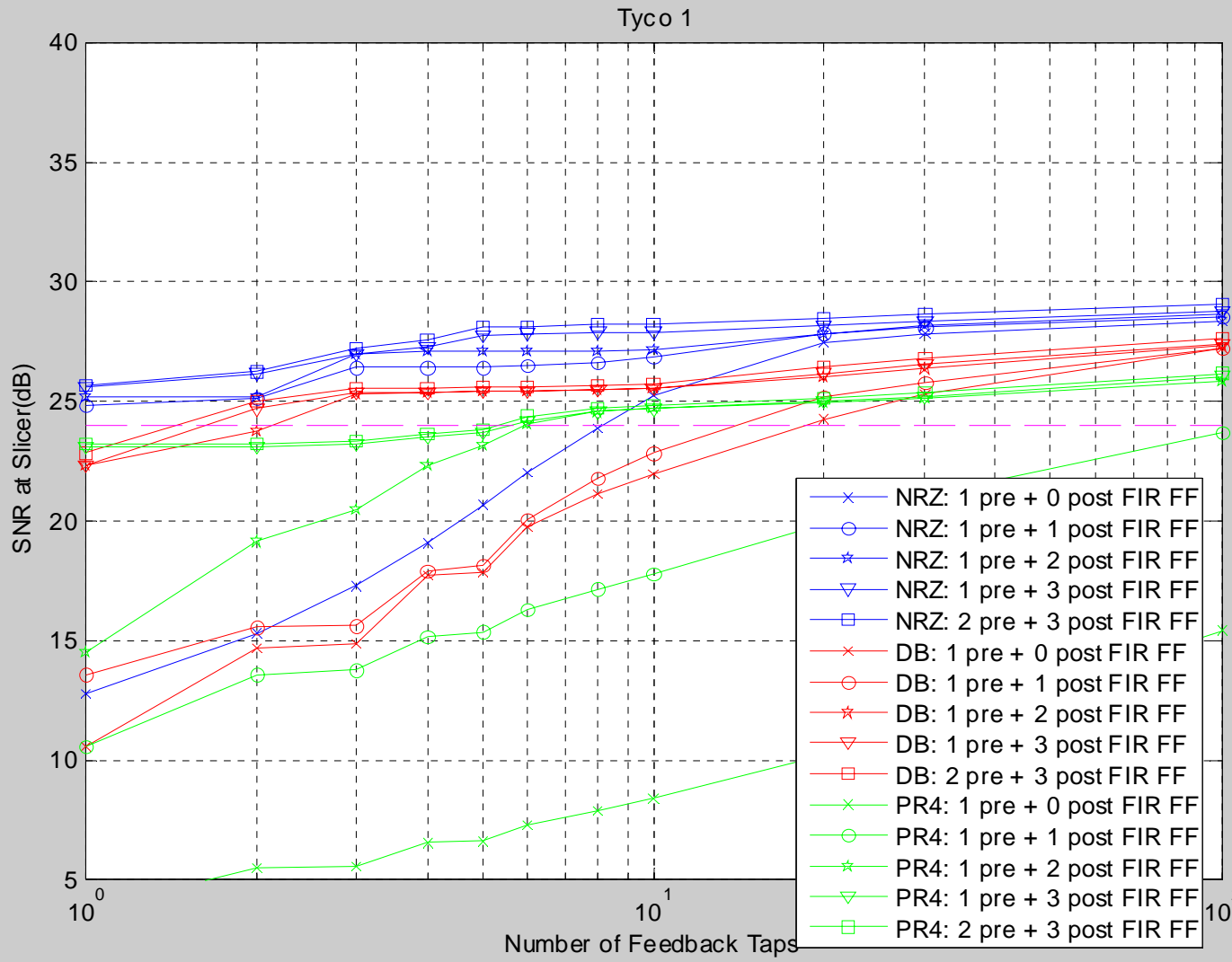
BP	NRZ	DB	PR4
	3 tap FF	4 tap FF	5 tap FF
Molex i2	2	6	100
Molex i3	2	8	100
Molex i4	2	10	100
Molex i5	2	6	100
Molex o2	<=1	4	100
Molex o3	<=1	5	100
Molex o4	<=1	4	100
Molex o5	<=1	3	100
Anderson	8	20	>100



Selected Results

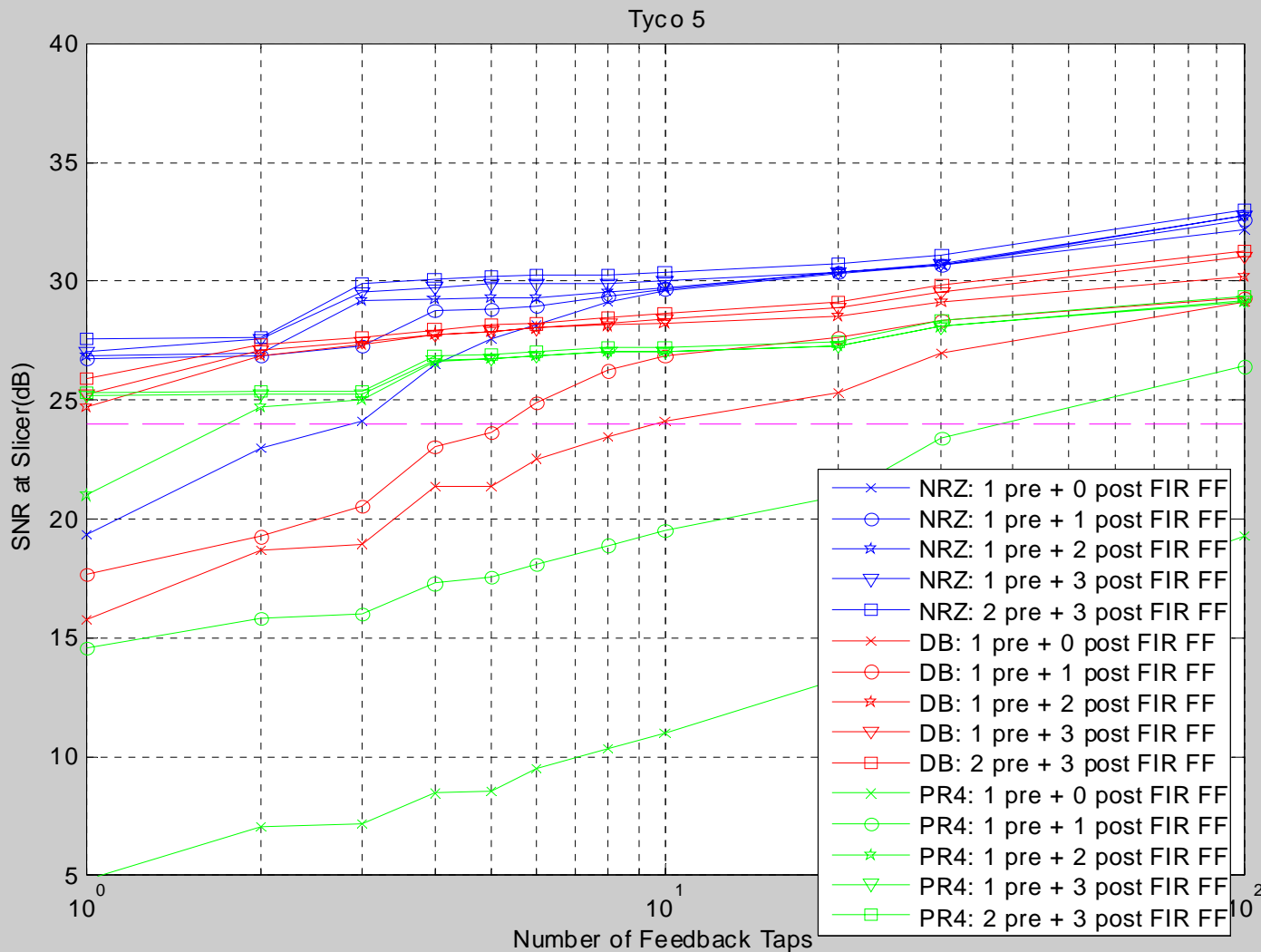
Results

Tyco 1 Backplane



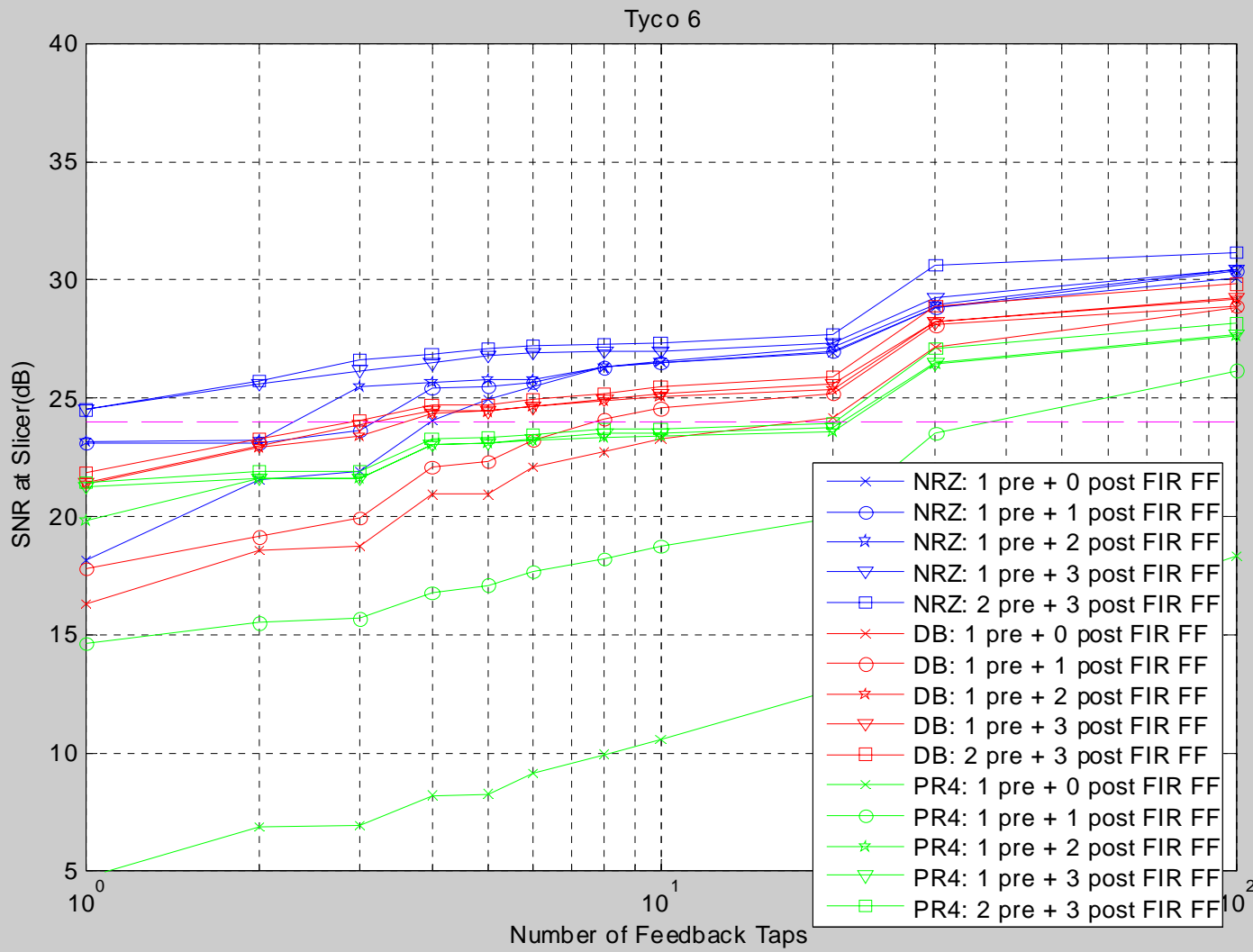
Results

Tyco 5 Backplane



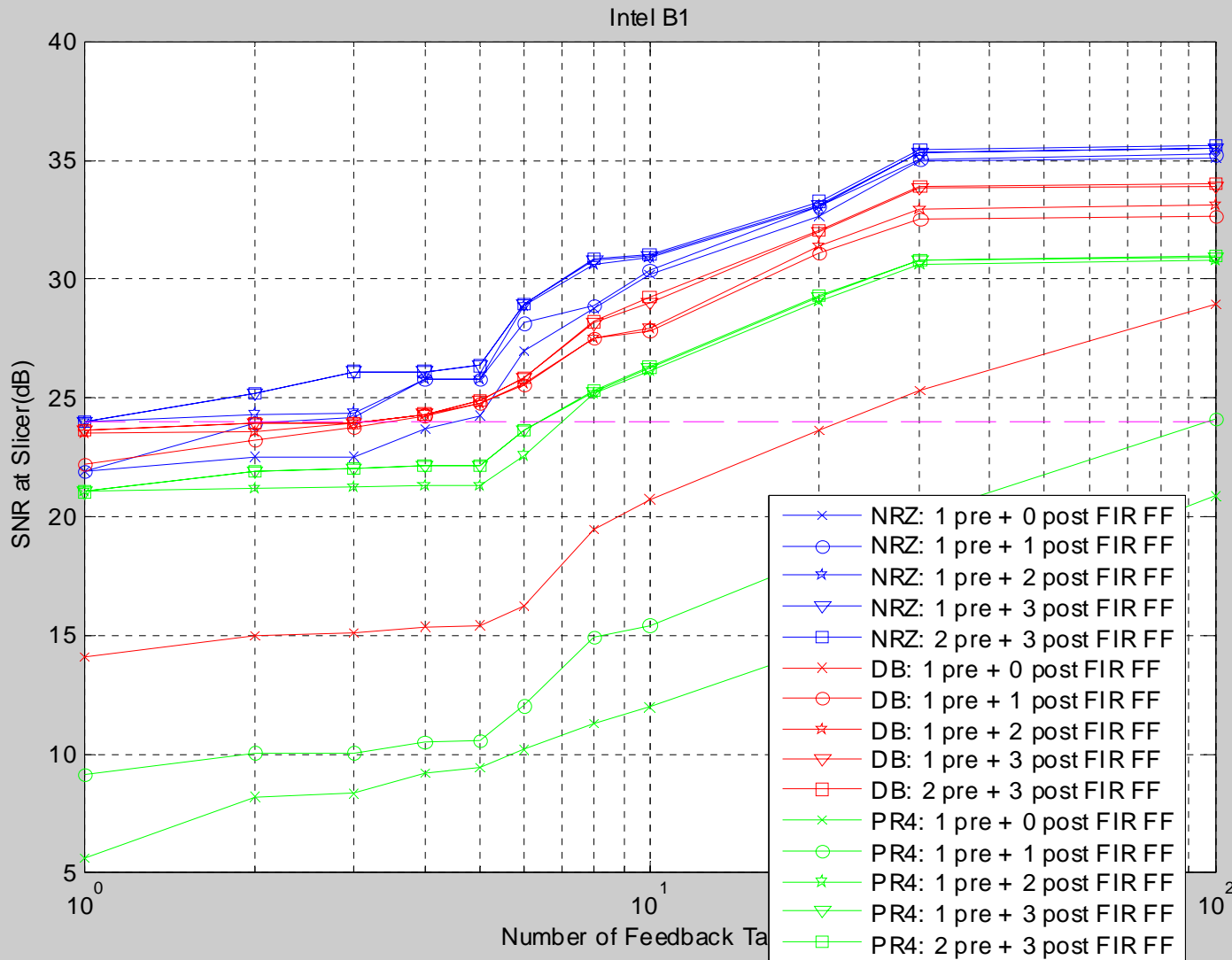
Results

Tyco 6 Backplane



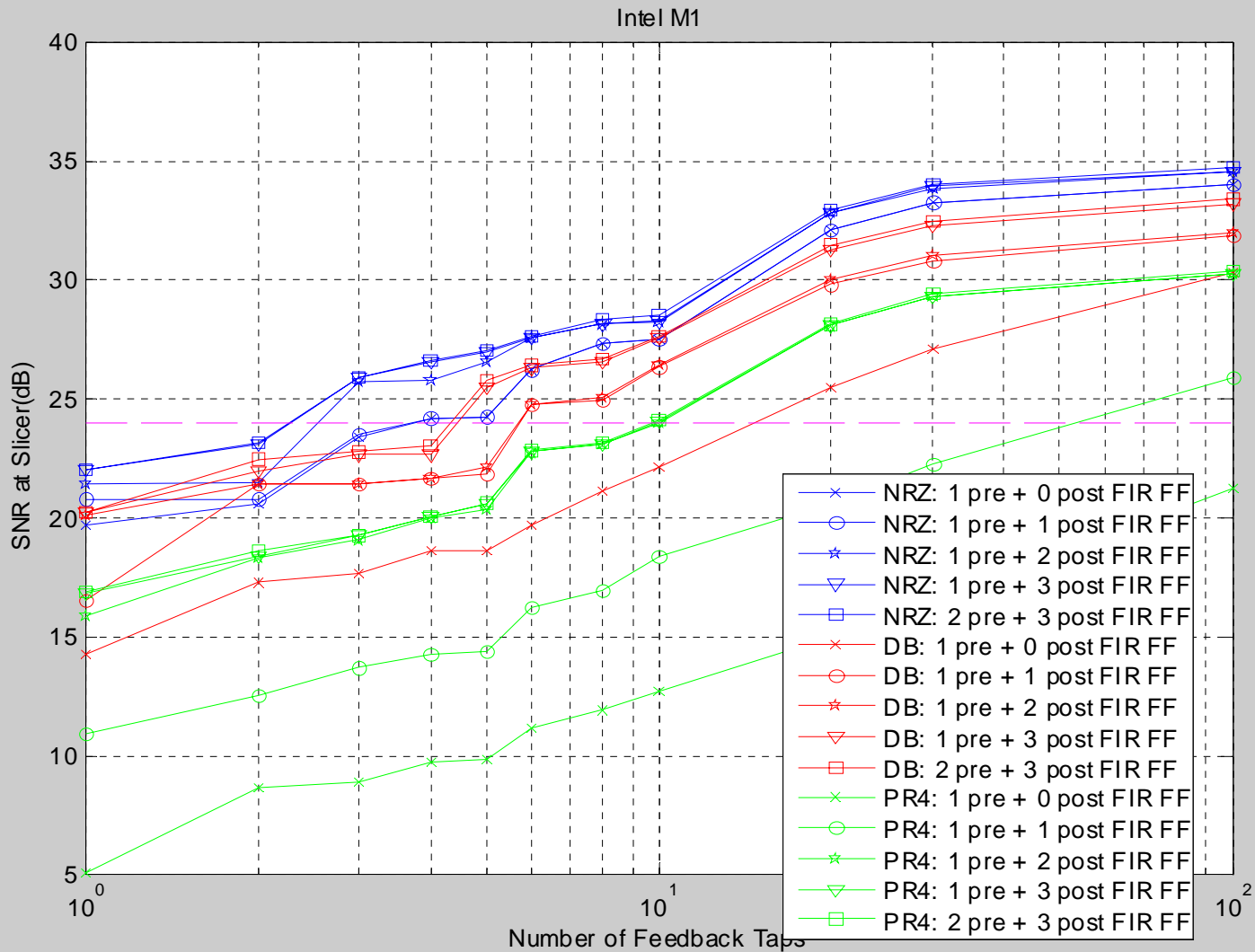
Results

Intel B1 Backplane



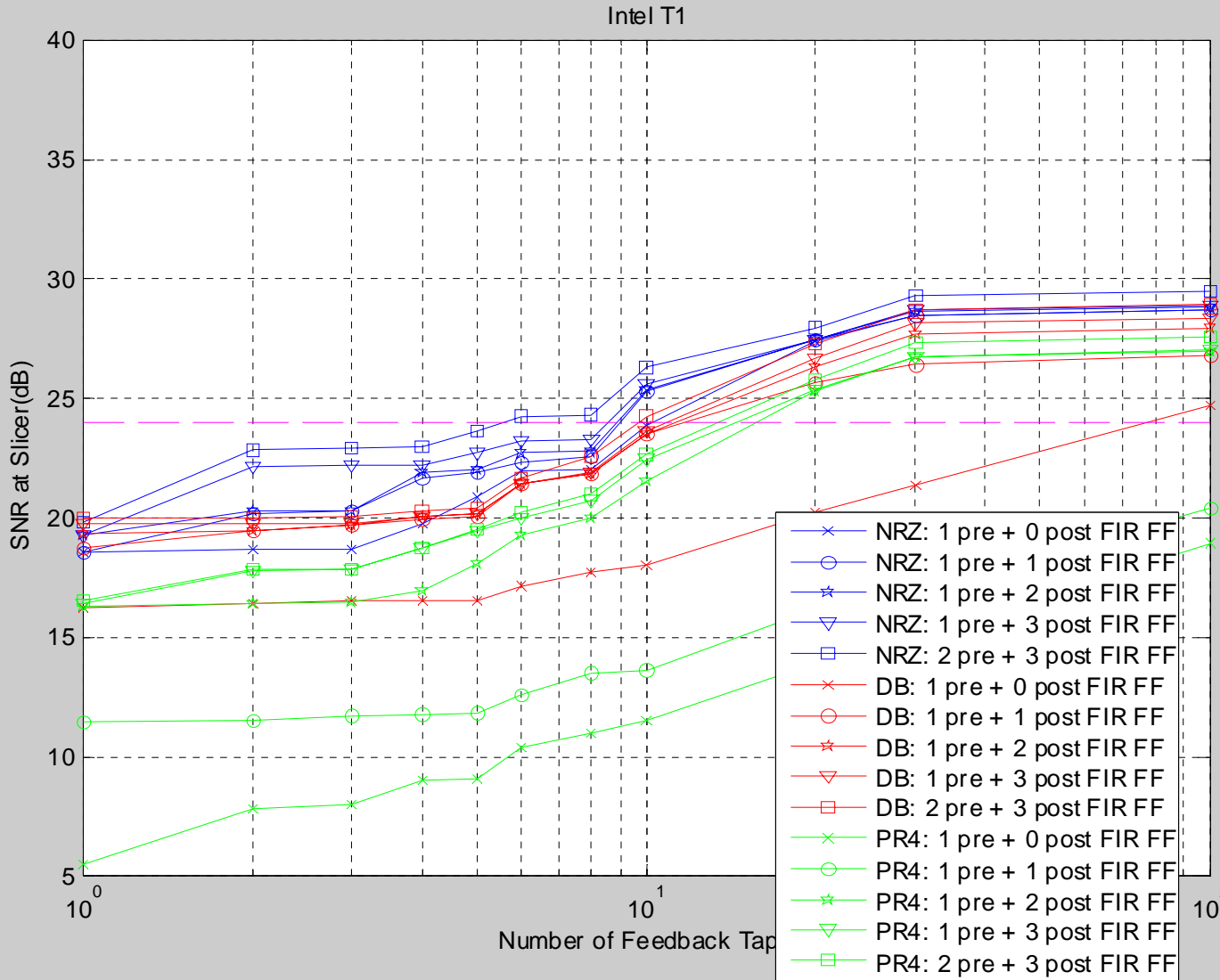
Results

Intel M1 Backplane



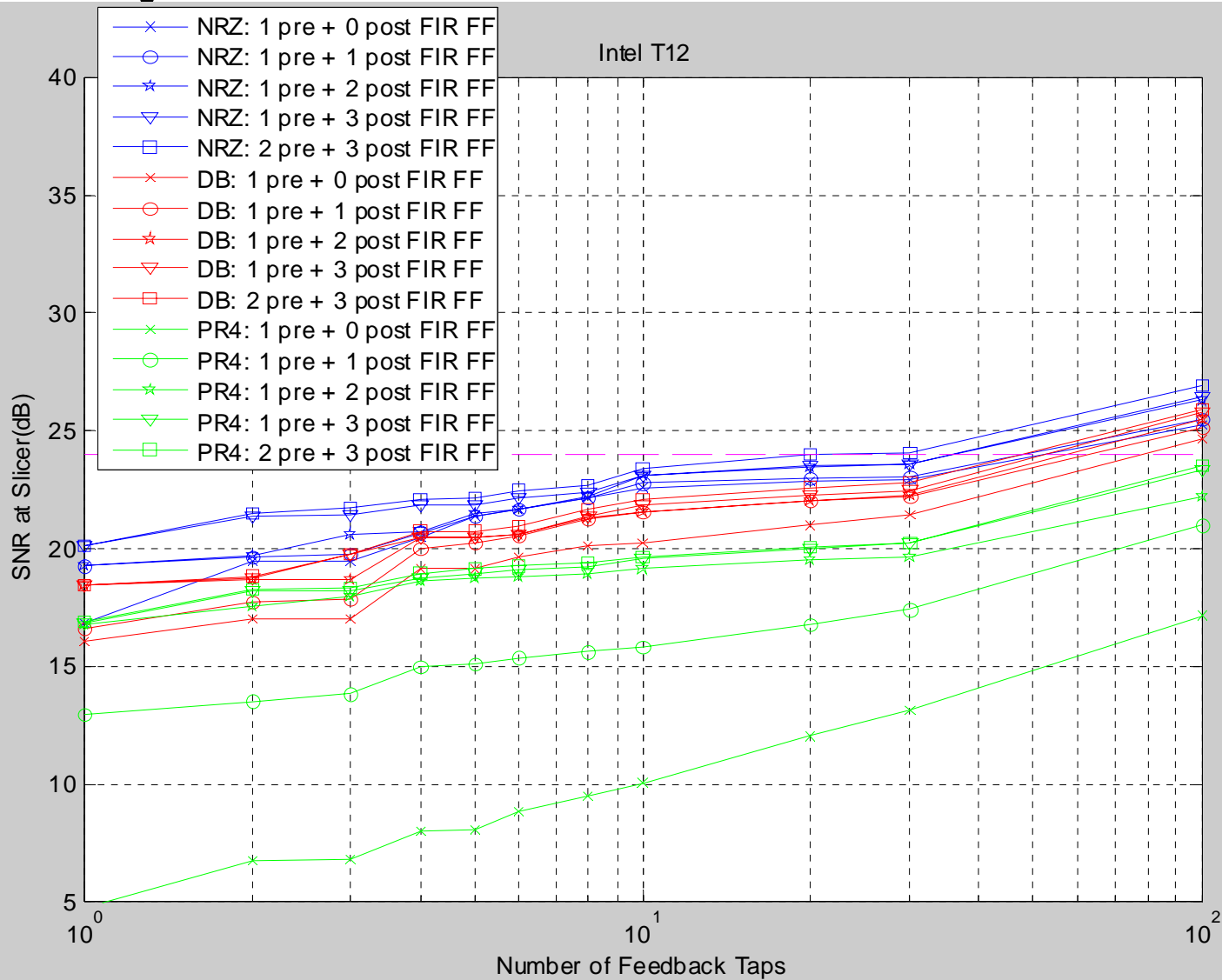
Results

Intel T1 Backplane



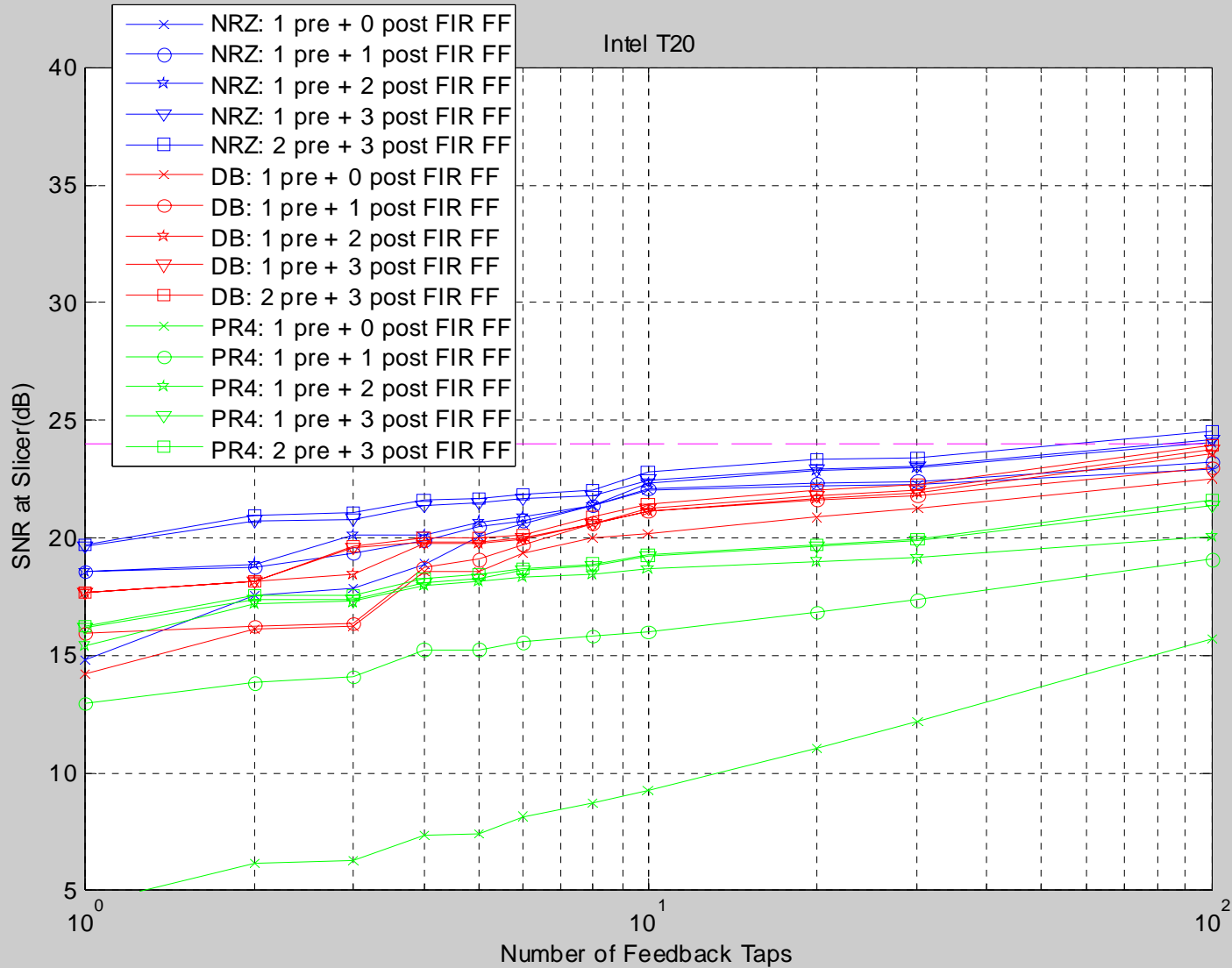
Results

Intel T12 Backplane



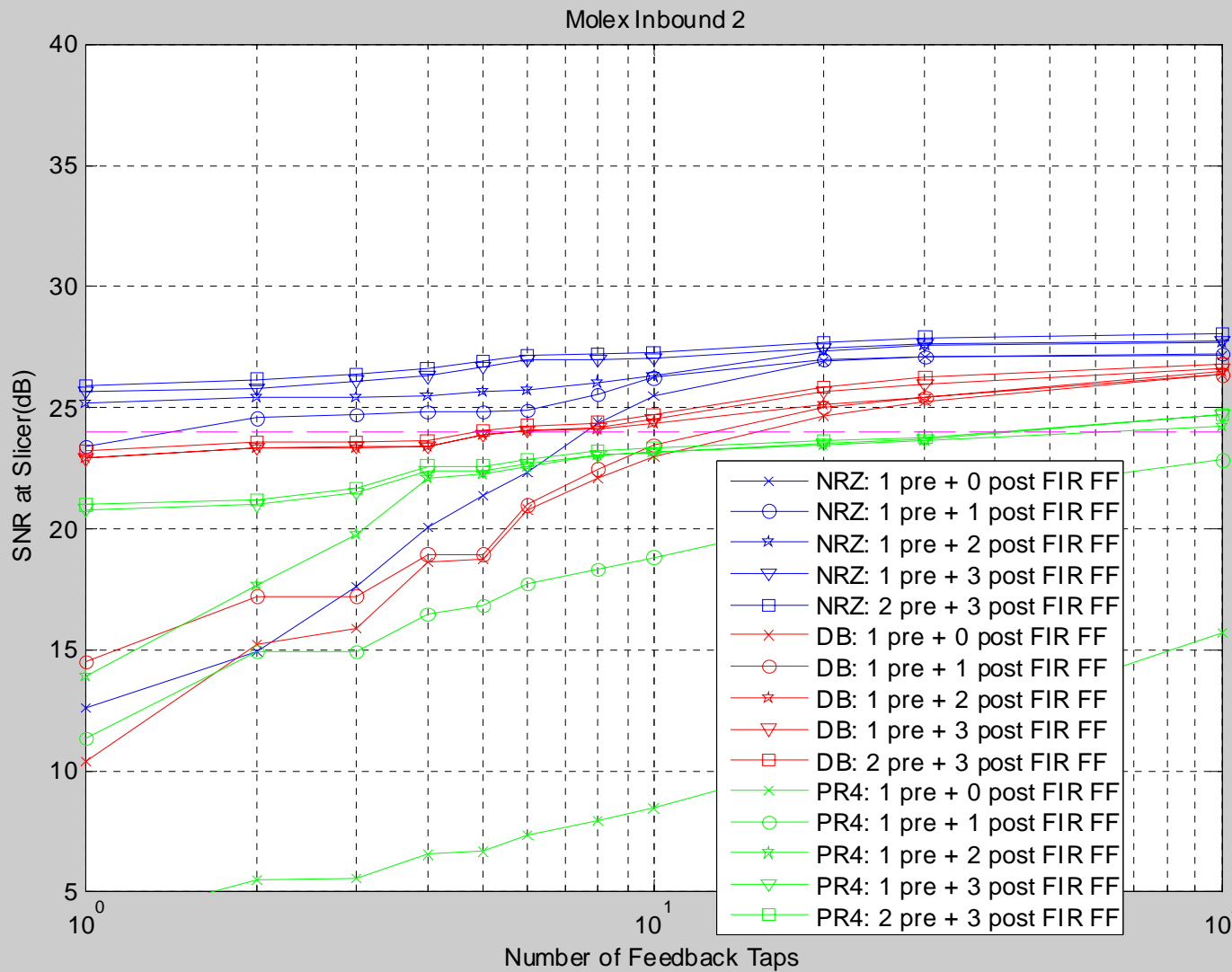
Results

Intel T20 Backplane



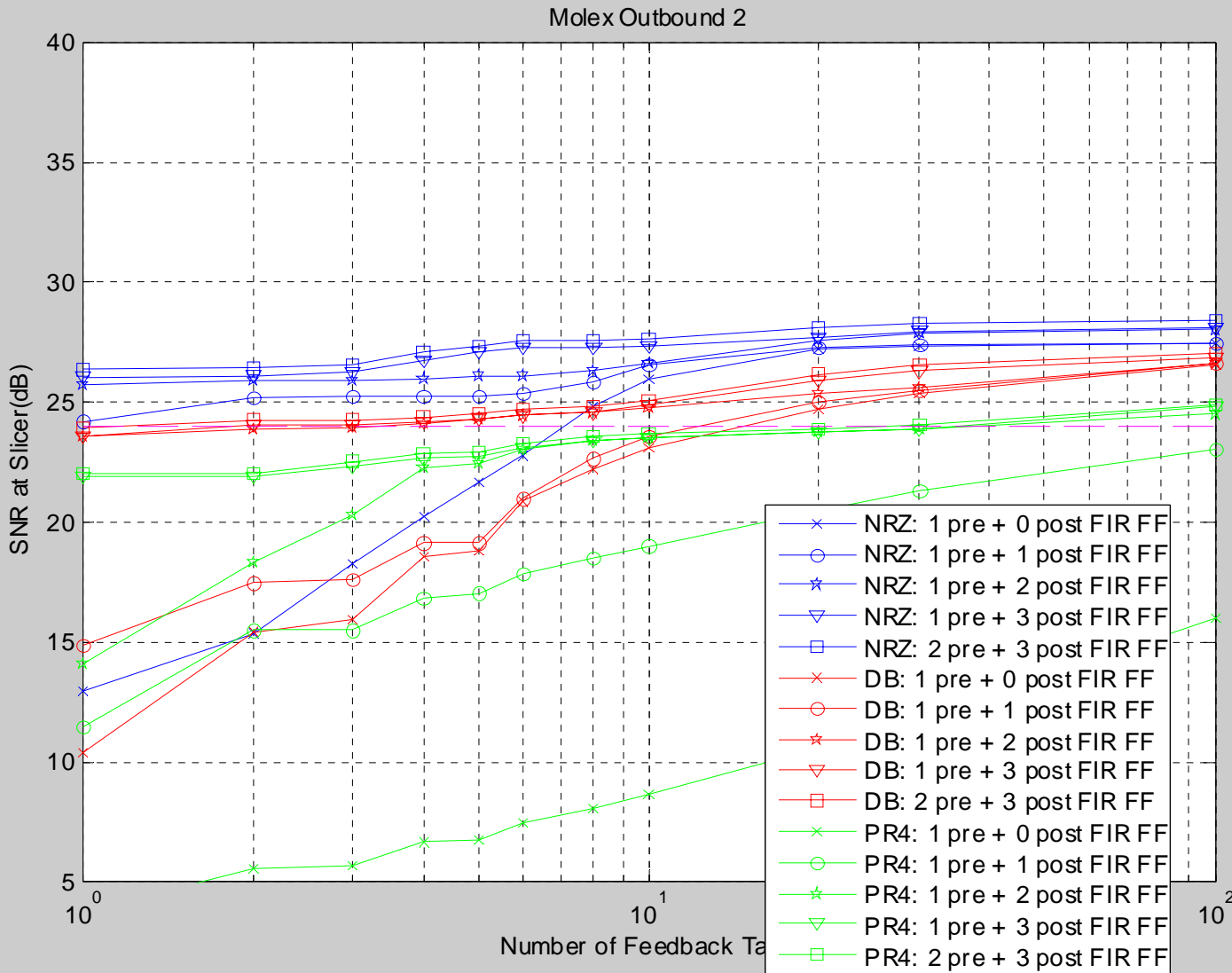
Results

Moxex Inbound 2 Backplane



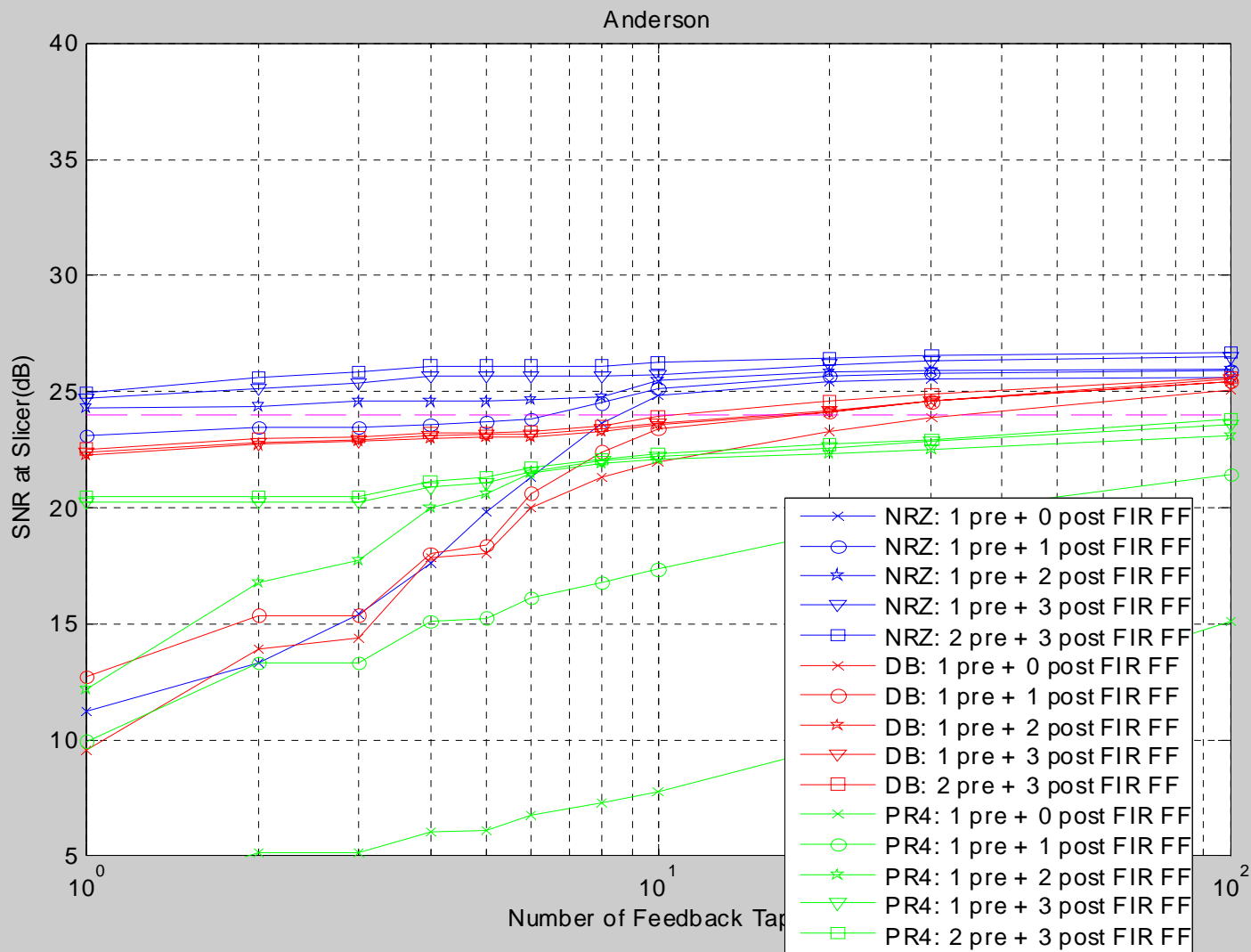
Results

Molex Outbound 2 Backplane



Results

Xilinx Backplane



Conclusions

- NRZ almost always outperformed Duobinary for similar equalization complexity.
- PR4 consistently performed worse than NRZ and Duobinary for similar complexity and does not appear to be appropriate for this application.
- Intel T1 backplanes are tremendously challenging to handle.