

# 10 Gb/s NRZ Signalling on Ethernet Backplane

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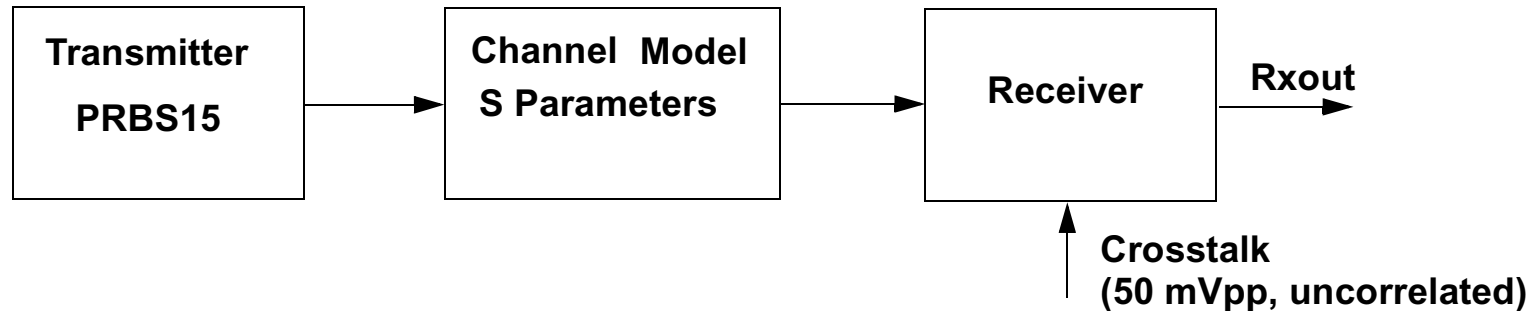
## 1. Outline

- NRZ Signalling
- Simulation Environment
- Results Evaluation Methodology
- Simulation Results

## 2. NRZ Signalling

- This contribution provides simulation results of performance across a subset of test channels using NRZ signalling.
- 10.3 Gb/s NRZ signalling for 10GBAS-KR is compatible with 1000BASE-KX and 10GBASE-KX4, and can use the same transmitter and receiver.
- NRZ signalling can be evaluated using current lab equipment and methodologies.
- NRZ signalling can use the latest developments in high speed equalization techniques and low geometry CMOS processing.
- Based on our estimates, using NRZ signalling will result in lowest power dissipation and highest density.

### 3. Simulation Environment



#### Transmitter

- 600 mVpp differential
- 0.35 UIpp total jitter
- 0.17 UIpp deterministic jitter
- 2 tap DFE capability (programmable)

#### Channel

- Tyco case 1 to 7
- Intel T1, T12, M1

#### Receiver

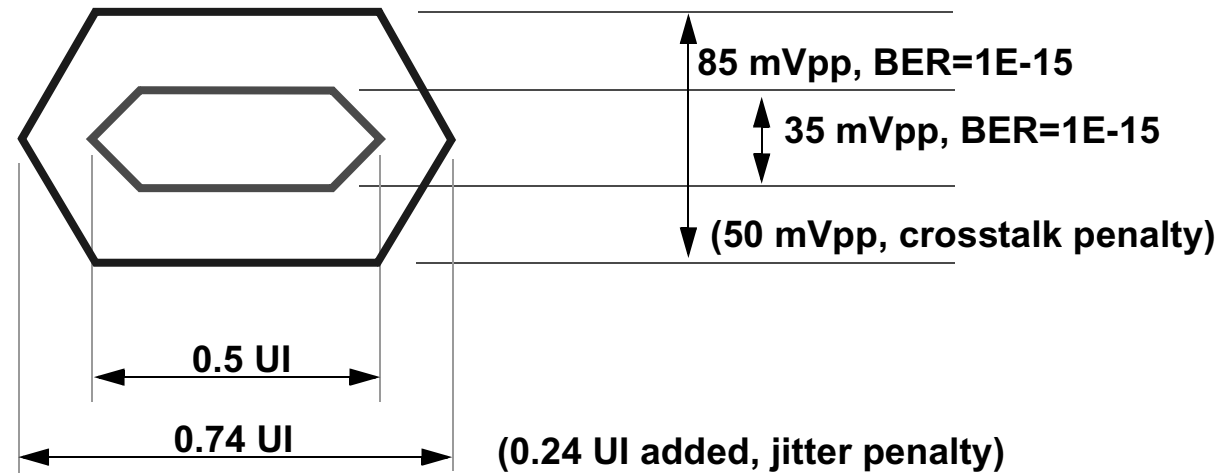
- receiver noise 2.2 mVrms
- receiver bandwidth 7.5 GHz (4th order BT)
- AGC capability
- 7 tap FFE and 5 tap DFE
- self adaptive
- CDR jitter 0.07 UIpp
- 0.5 UI, eye opening for BER=1E-15

**Note 1:** The package models are not included in these simulations.

**Note 2:** The receiver architecture was chosen based on existing circuit implementation and is not intended to be recommended as required receiver architecture.

## 4. Results evaluation methodology

Received signal (Rxout, equalizer output) eye mask for BER=1E-15



- Transmitter deterministic jitter ( $0.17 \text{ UI}$ ), will close the received eye.
- Receiver clock jitter  $0.07 \text{ UI}$  will reduce the horizontal eye opening.
- Crosstalk signal amplitude maximum  $50 \text{ mVpp}$ , uncorrelated with the incoming data.

## 5. Simulation results summary

<b>Channel</b>	<b>Transmitter DFE taps</b>	<b>Eye Mask BER 1E-15</b>
<b>Tyco Case 1</b>	<b>1</b>	<b>Pass</b>
<b>Tyco Case 2</b>	<b>1</b>	<b>Pass</b>
<b>Tyco Case 3</b>	<b>1</b>	<b>Pass</b>
<b>Tyco Case 4</b>	<b>1</b>	<b>Pass</b>
<b>Tyco Case 5</b>	<b>0</b>	<b>Pass</b>
<b>Tyco Case 6</b>	<b>0</b>	<b>Pass</b>
<b>Tyco Case 7</b>	<b>0</b>	<b>Pass</b>
<b>Intel T1</b>	<b>0</b>	<b>Pass</b>
<b>Intel T12</b>	<b>0</b>	<b>Pass</b>
<b>Intel M1</b>	<b>1</b>	<b>Pass</b>