

The VITESSE logo is rendered in a bold, blue, italicized sans-serif font. It is positioned in the upper right quadrant of the slide, above a large orange banner. The background of the slide features a blue-tinted image of hands holding a square microchip with a 'V' logo, and a grey background with a dotted pattern on the right side.

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Duobinary Transmission over ATCA Backplanes

Majid Barazande-Pour
John Khoury

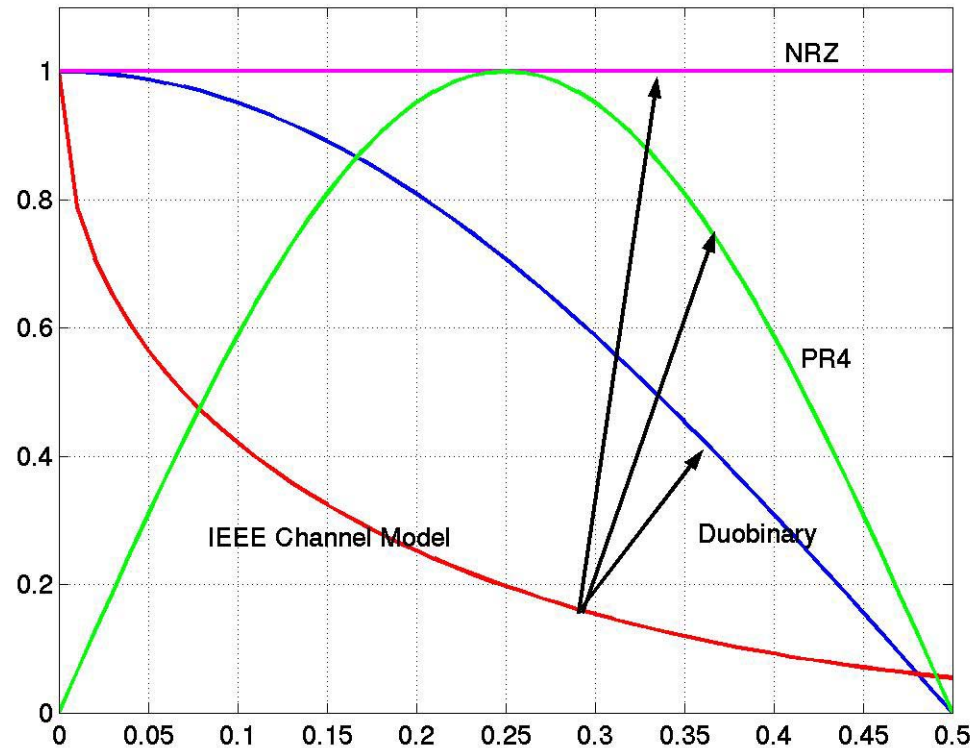
November 15-19, 2004

IEEE 802.3ap Backplane Ethernet Task Force Plenary Meeting

San Antonio Texas

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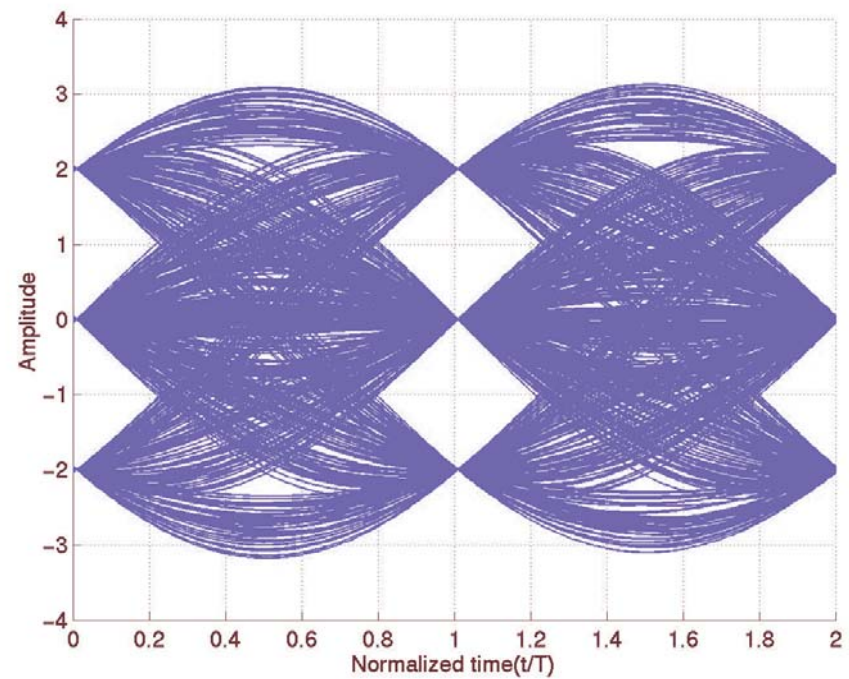
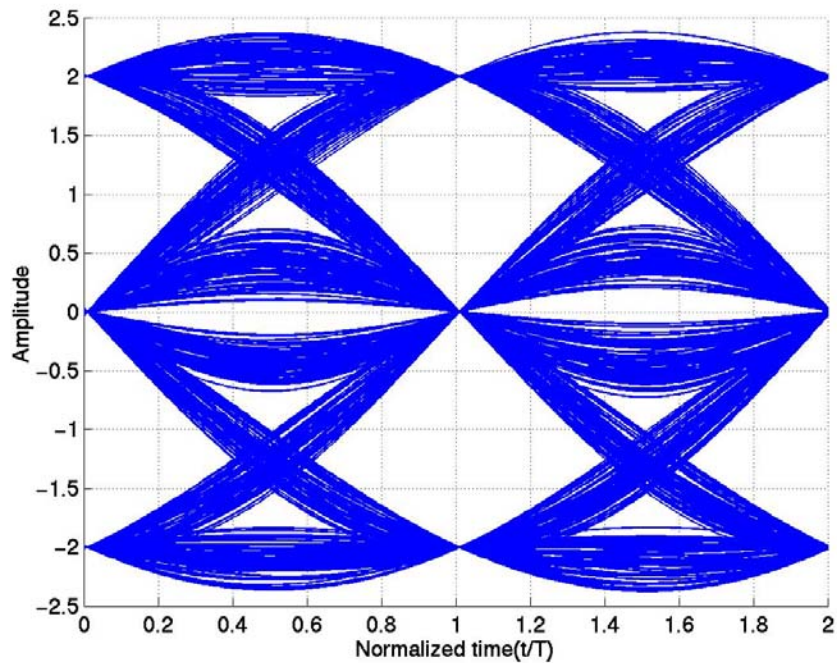
- ▶ Introduction
- ▶ Adaptive FSE + DFE for Duobinary Signaling
- ▶ ATCA Backplanes
 - ▶ Tyco
 - ▶ Intel
- ▶ Simulation Results
- ▶ Equalizer Requirements and Conclusion



- ▶ Duobinary requires the least amount of boost at higher frequencies.

Duobinary and PR2 Eye Diagrams

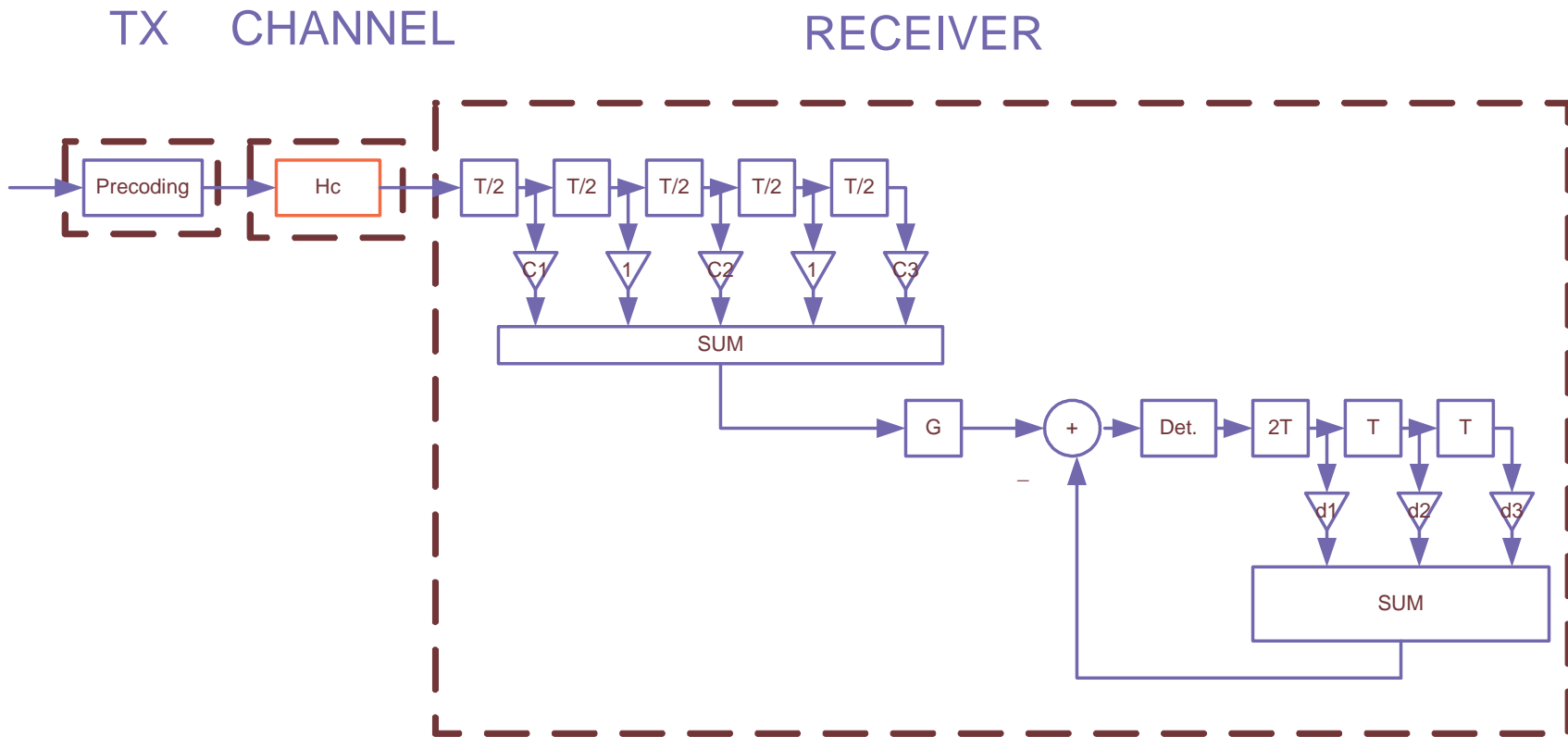
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- ▶ In duobinary, Transition from 2 to -2 and -2 to 2 over one bit period is not allowed.
 - ▶ Low horizontal Jitter

Adaptive FSE+DFE Block Diagram for Duobinary Signaling

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▶ Transmitter:

- ▶ Transmitter pre-emphasis: For Long Channels (40") one pre-emphasis tap at at most 0.4 was used at transmitter.

$$H_{\text{pre}}(z) = 1 - \alpha z^{-1}$$

- ▶ Transmit amplitude: 800 mv peak-to-peak differential

▶ Receiver Equalizer:

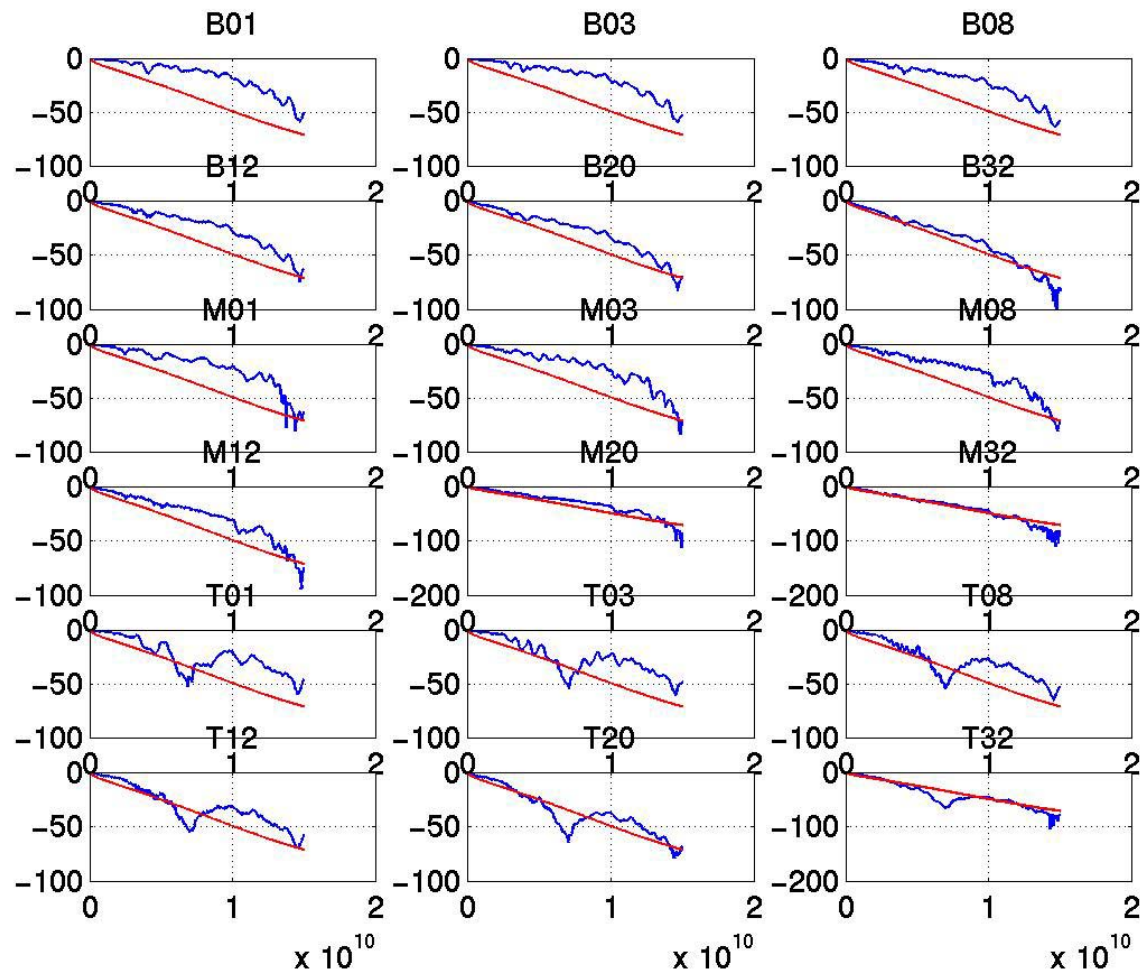
- ▶ Fractionally Spaced Equalizer, 5 Taps (3 variable)
 - Low sensitivity to sampling time.
- ▶ DFE: 3 Taps

▶ Receiver Input and Transmitter Output Models

- ▶ Differential 100 ohms resistance
- ▶ 0.5 pf of capacitance was used as a model for the effects via, package and chip capacitances.

- ▶ Optimum Coefficients are are obtained using adaptive LMS Algorithm.
- ▶ Simple Alexander timing recovery algorithm was used at the receiver.
- ▶ Floating point representation of coefficients
- ▶ No training pattern was used in the simulations.
- ▶ A wide variety of ATCA channels (provided by Intel and Tyco to IEEE 802.3 task force) were used for simulations.
- ▶ No Crosstalk.
- ▶ No TX or RX clock jitter.

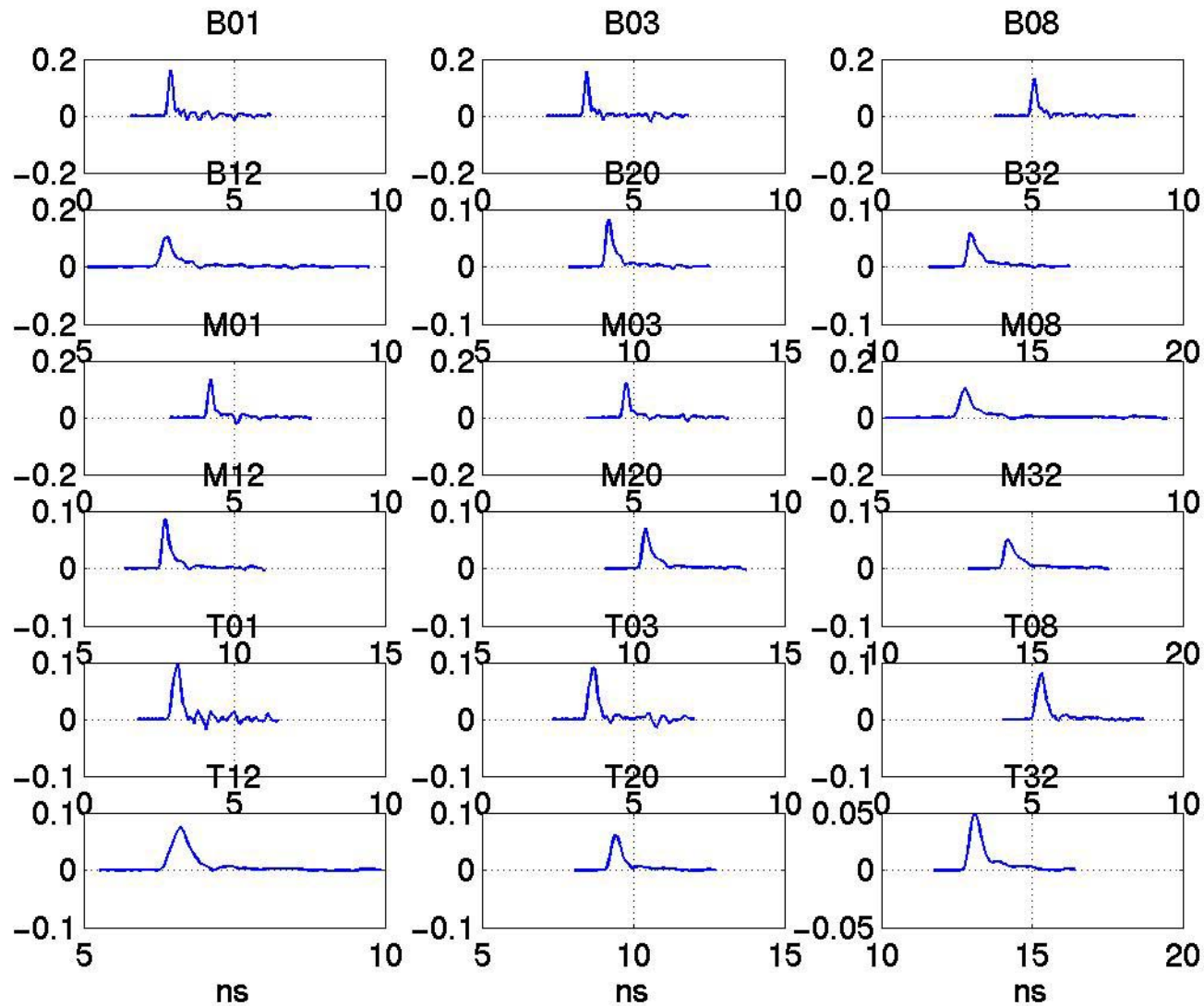
- ▶ Vertical and horizontal margins are defined to achieve BER of $1e-15$.
- ▶ Vertical Margin
 - ▶ Subtract the effect of residual ISI after equalization
 - ▶ Subtract the effect of dc offset and slicer sensitivity (total value of 10 mv is assumed)
 - ▶ Margin is defined as the maximum standard deviation of residual Gaussian noise to achieve BER of $1e-15$
- ▶ Horizontal margin
 - ▶ Subtract the effect of ISI on horizontal eye opening
 - ▶ Margin is defined as maximum standard deviation of the residual clock jitter (Gaussian assumption) to achieve BER of $1e-15$.

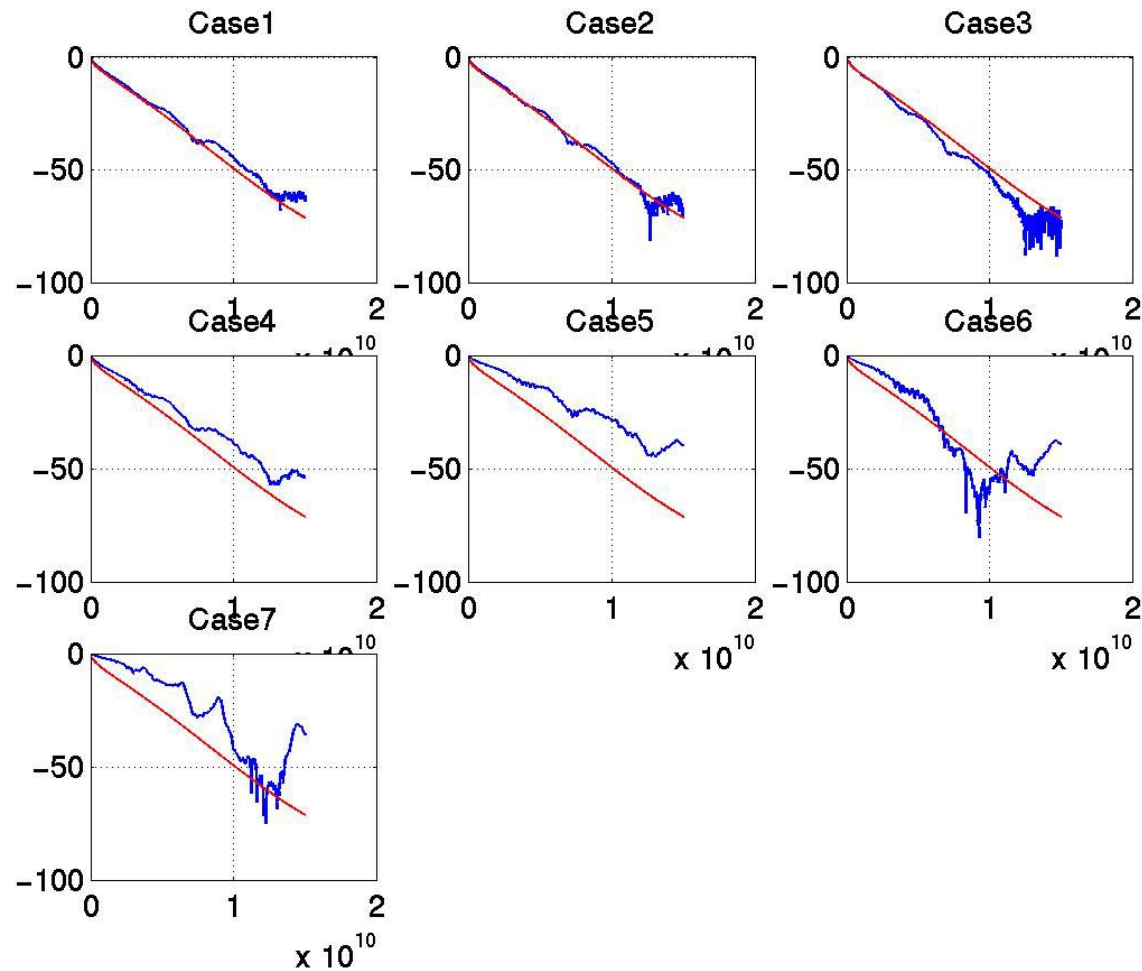


- ▶ Backplanes (B01, B03, B32, M32, T01, T20) were used in simulations.

Intel ATCA Channels Impulse Responses

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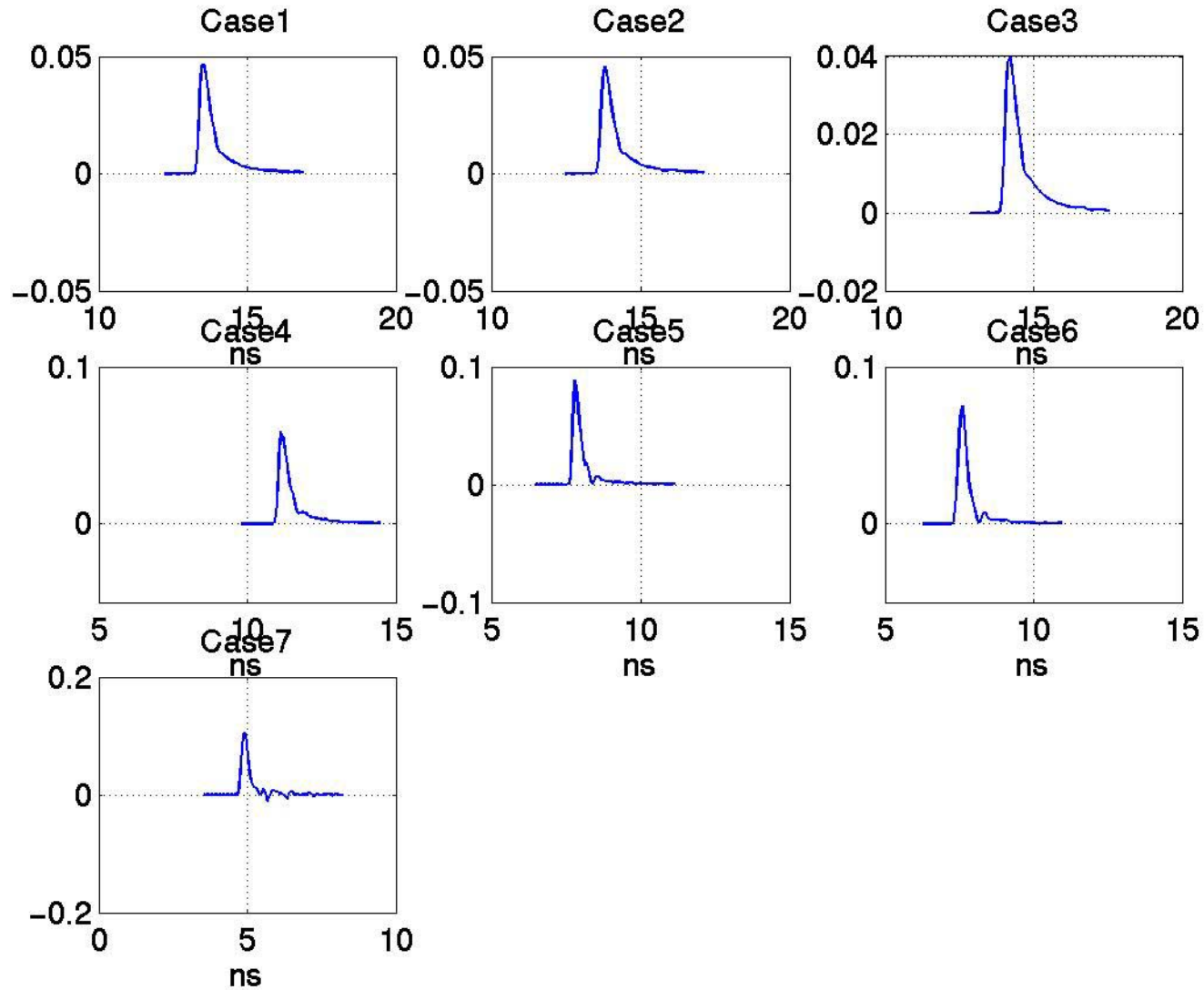




- ▶ Backplanes (Case1, Case3, Case4, Case6, Case7) were used in simulations.

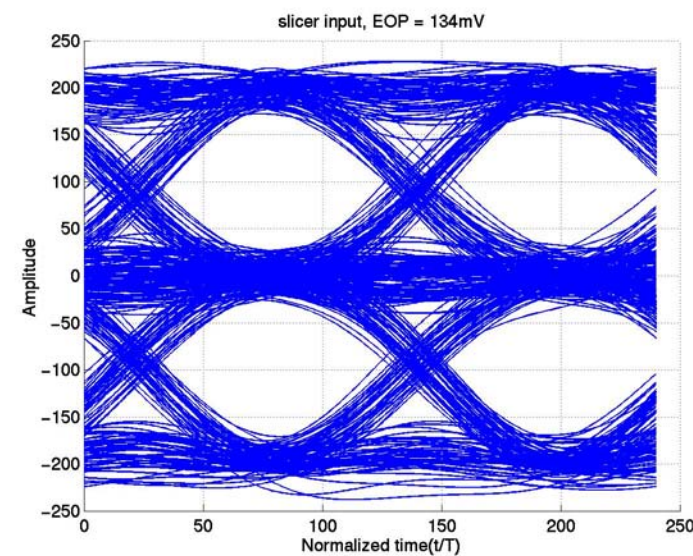
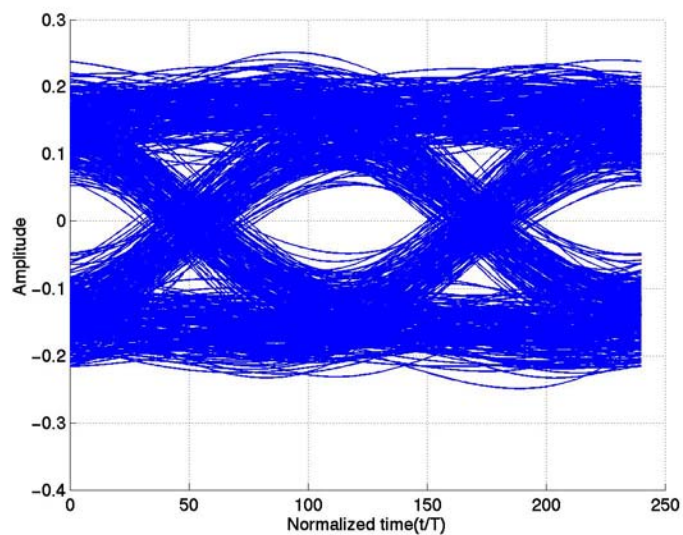
Tyco ATCA Channels Impulse Responses

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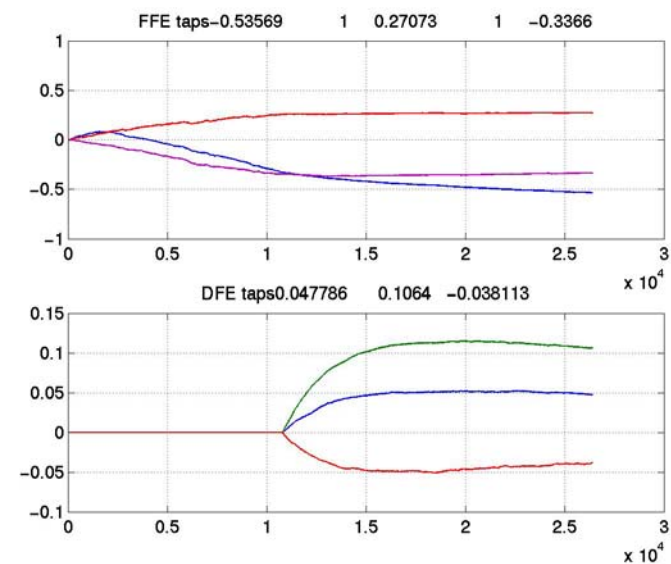


Simulation Results for Intel ATCA B1

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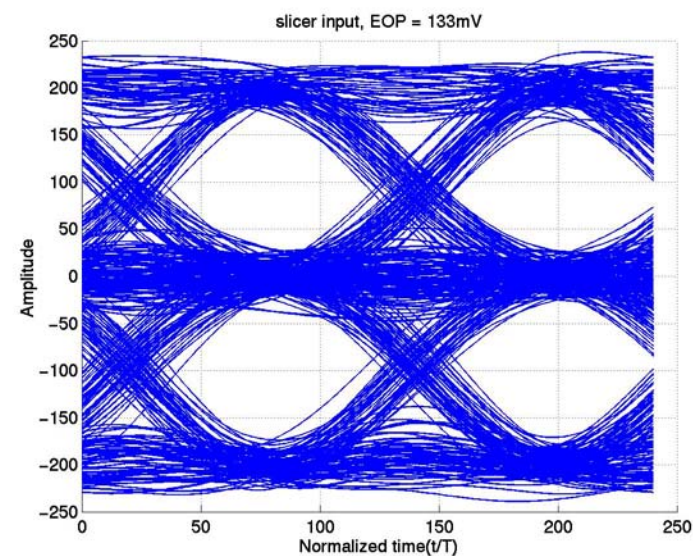
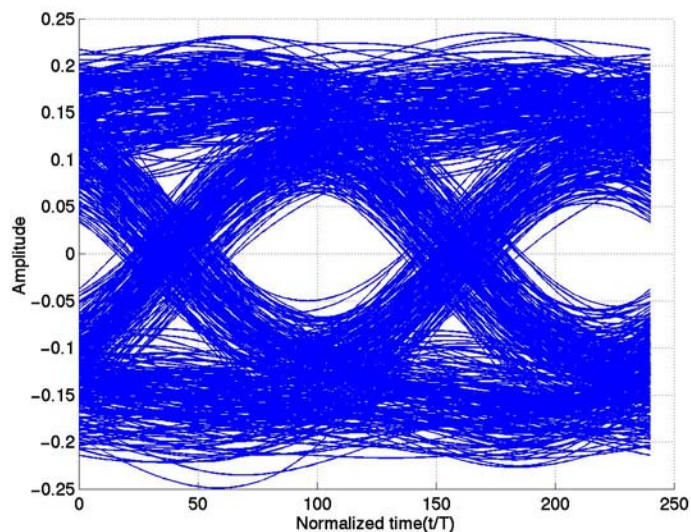


- ▶ Length: 2.25" + 1.25" + 2.97"
- ▶ Eye opening: 1
 - ▶ Vertical: 134 mv, (margin= 7.12 mv)
 - ▶ Horizontal: 85 ps (margin = 5.3 ps)
- ▶ Pre-emphasis: 0

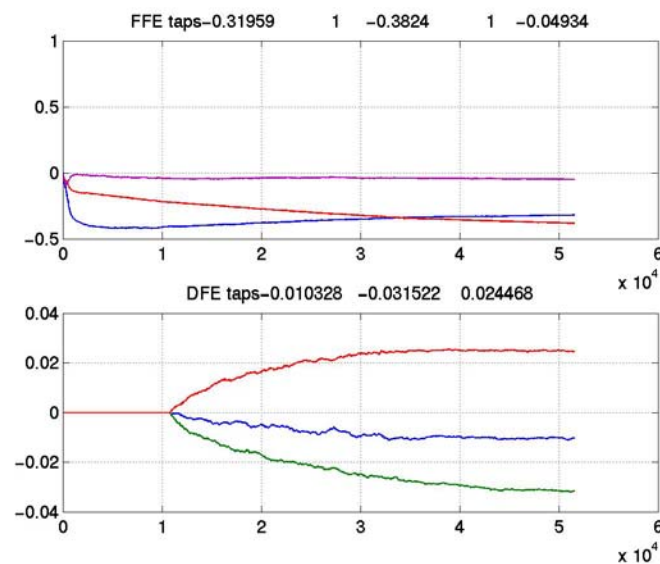


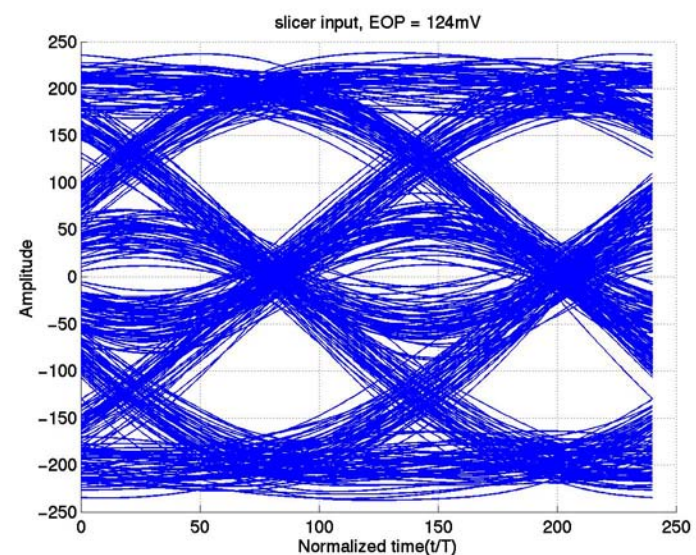
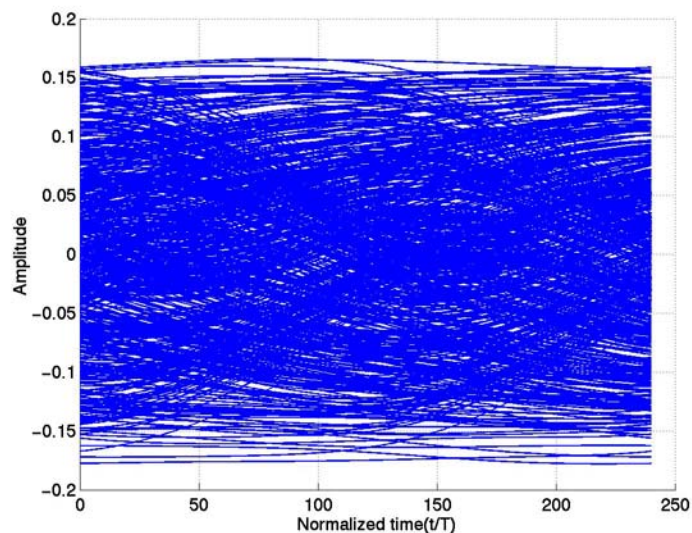
Simulation Results for Intel ATCA B3

VITESSE

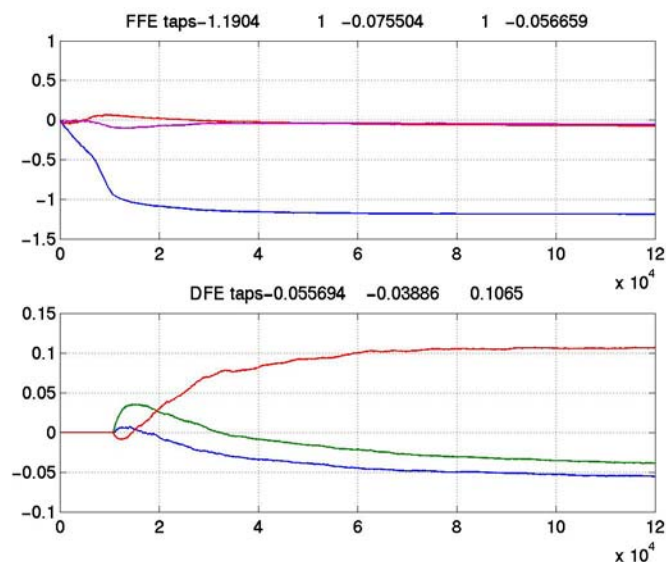


- ▶ Length: 2.25" + 3" + 2.97"
- ▶ Eye opening:
 - ▶ Vertical: 133 mv (margin = 7 mv)
 - ▶ Horizontal : 80 ps (margin = 5 ps)
- ▶ Pre-emphasis: 0



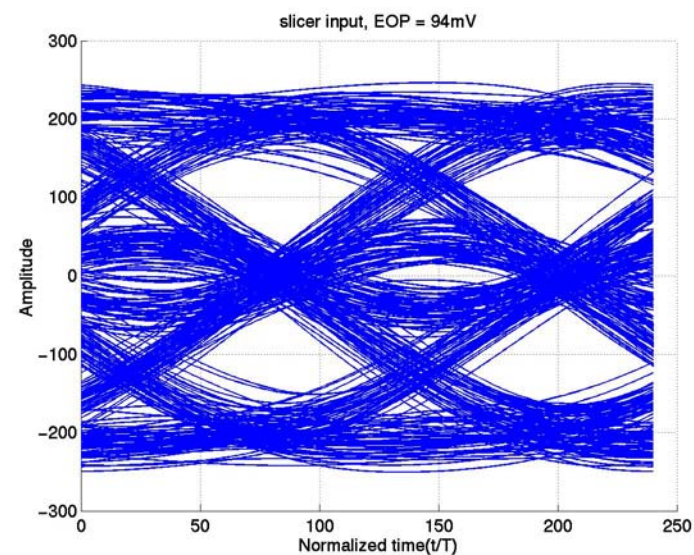
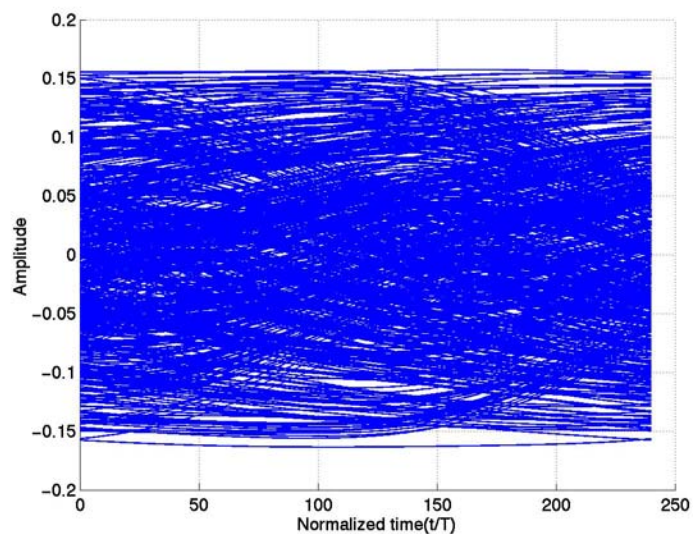


- ▶ Length: 2.25" + 32" + 2.97"
- ▶ Eye opening:
 - ▶ Vertical: 124 mv (margin= 6.5 mv)
 - ▶ Horizontal: 71 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0

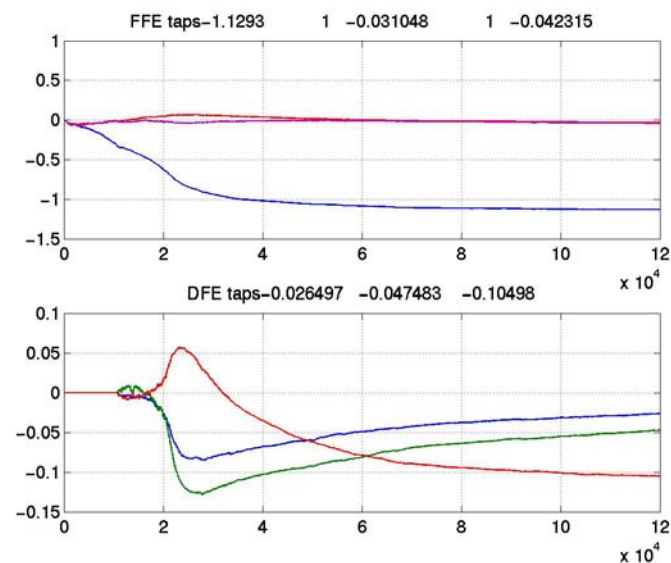


Simulation Results for Intel ATCA M32

VITESSE

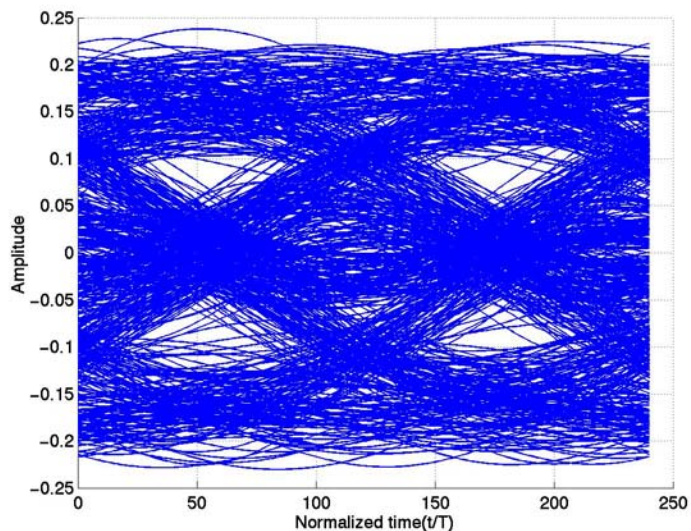


- ▶ Length: 4.75" + 32" + 3.79"
- ▶ Eye opening:
 - ▶ Vertical: 94 mv (margin = 4.6 mv)
 - ▶ Horizontal: 71 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0

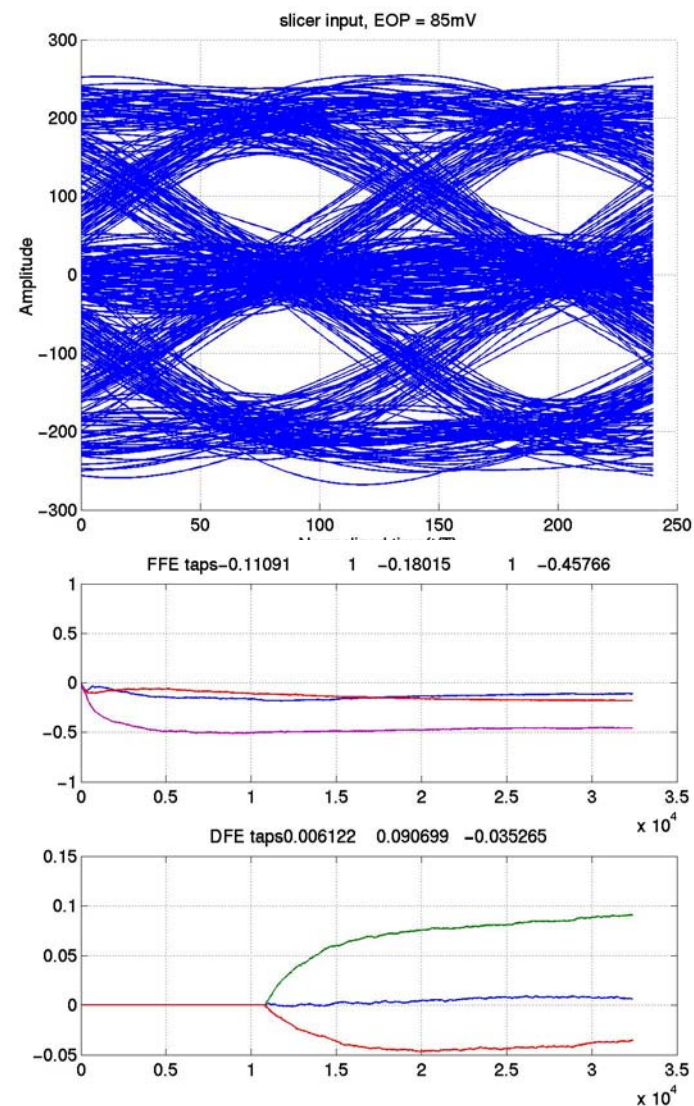


Simulation Results for Intel ATCA T1

VITESSE

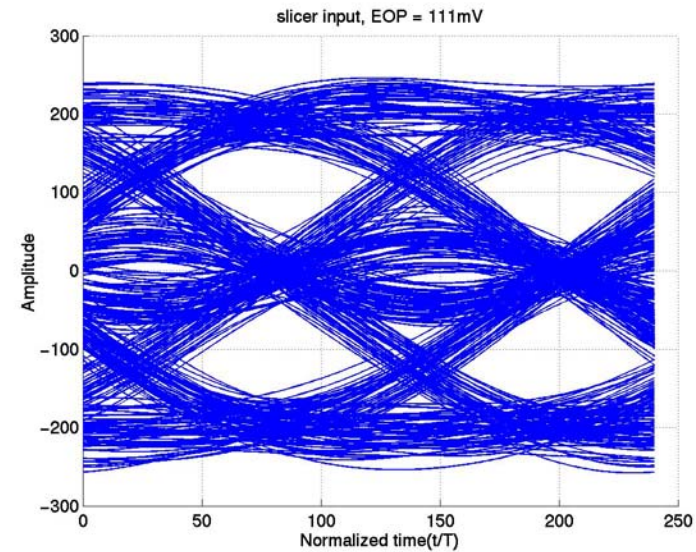
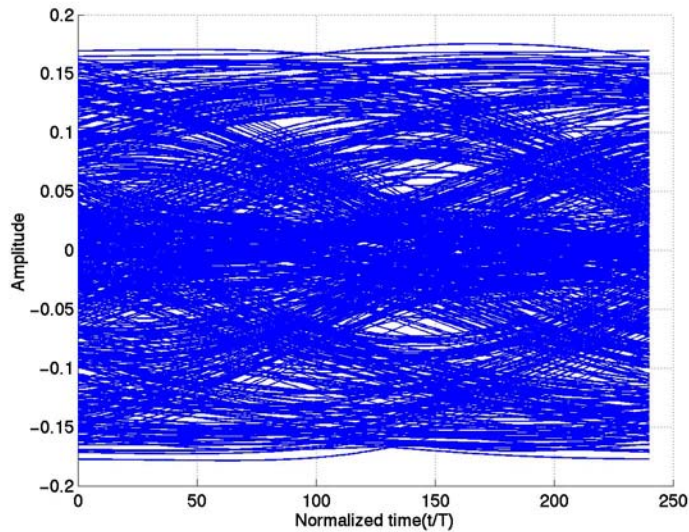


- ▶ Length: 2.73" + 1.25" + 3.18"
- ▶ Eye opening:
 - ▶ Vertical 85 mv (margin = 4 mv)
 - ▶ Horizontal: 71 (margin = 4.4 ps)
- ▶ Pre-emphasis: 0

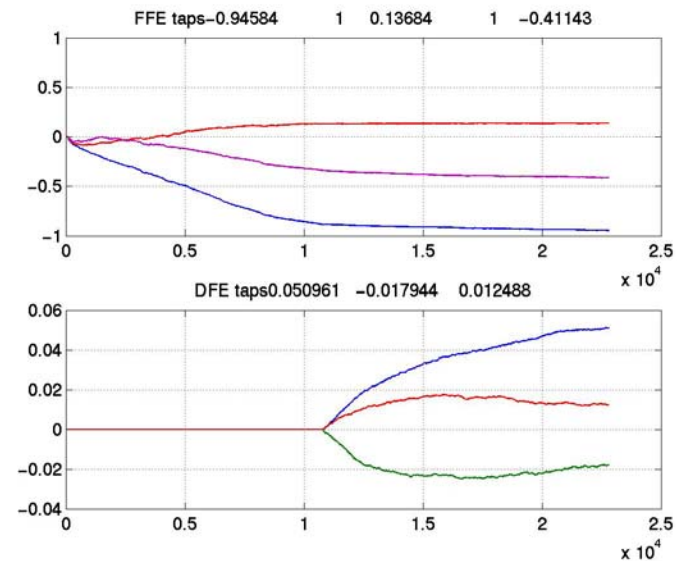


Simulation Results for Intel ATCA T20

VITESSE

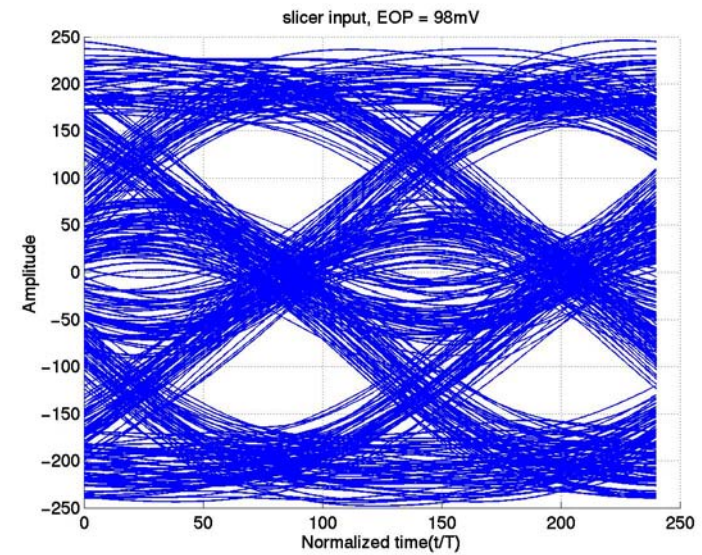
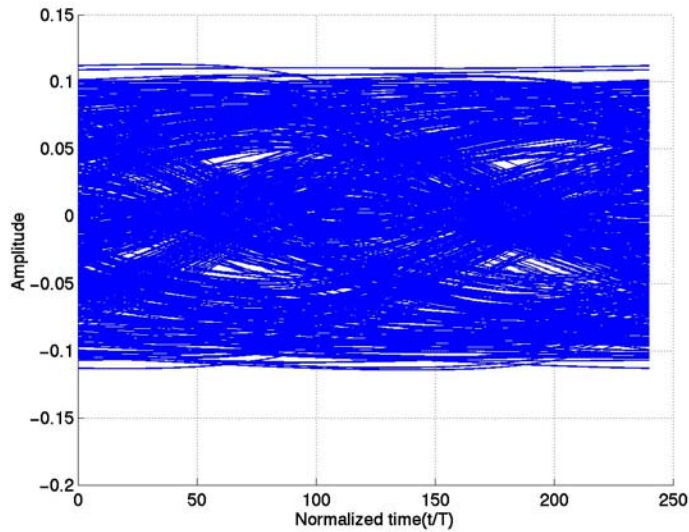


- ▶ Length: 2.73" + 12" + 3.18"
- ▶ Eye opening:
 - ▶ Vertical 111 mv (margin = 5.7 mv)
 - ▶ Horizontal: 70 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0

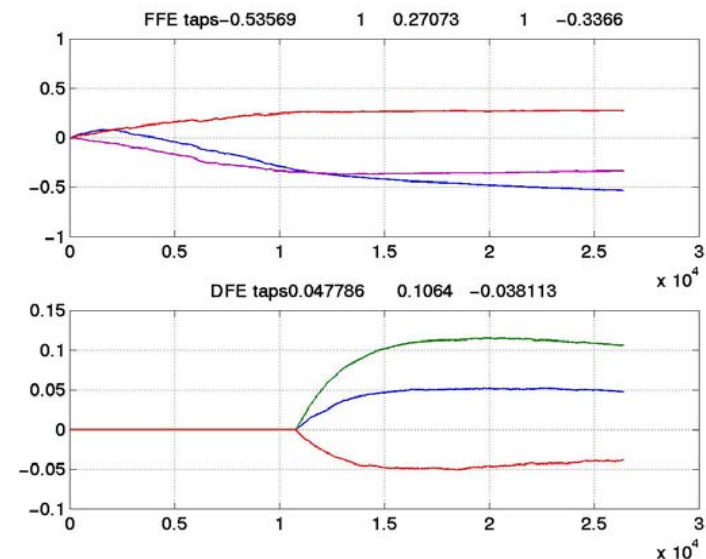


Simulation Results for Tyco ATCA Case1

VITESSE

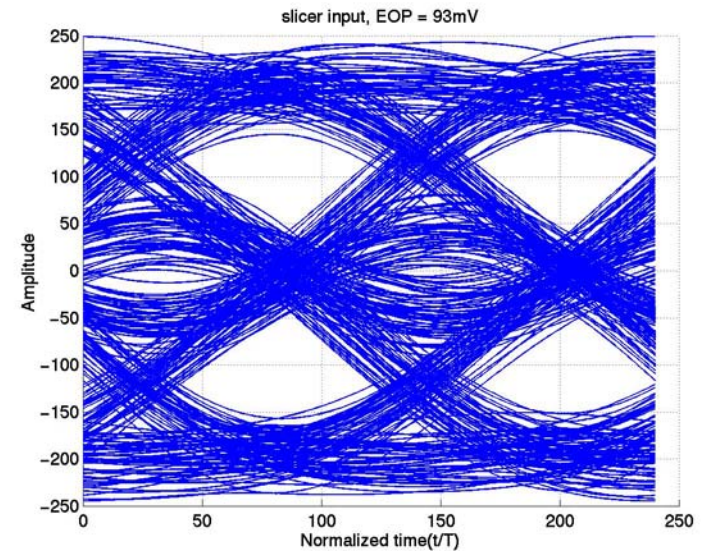
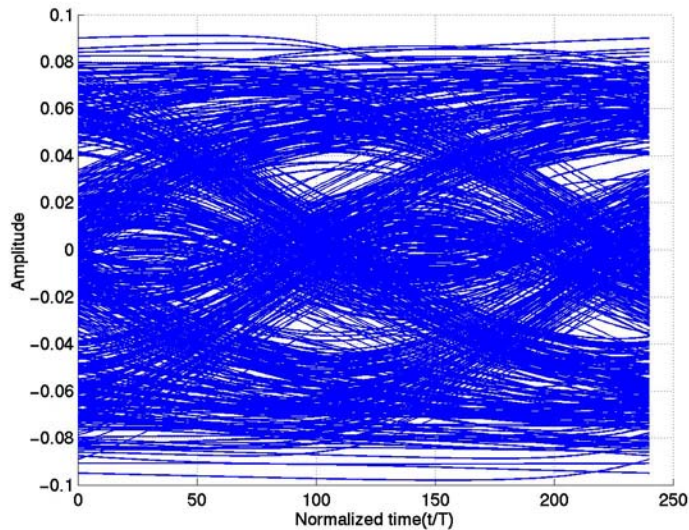


- ▶ Length: 10"+20"+10"
- ▶ Stub Bottom (or counter boring)
- ▶ Eye opening:
 - ▶ Vertical: 98 mv (margin = 4.87 mv)
 - ▶ Horizontal: 70 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0.3

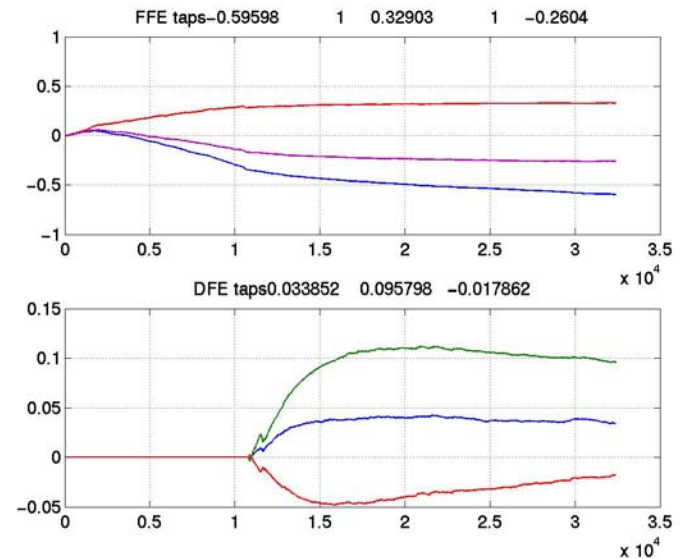


Simulation Results for Tyco ATCA Case3

VITESSE

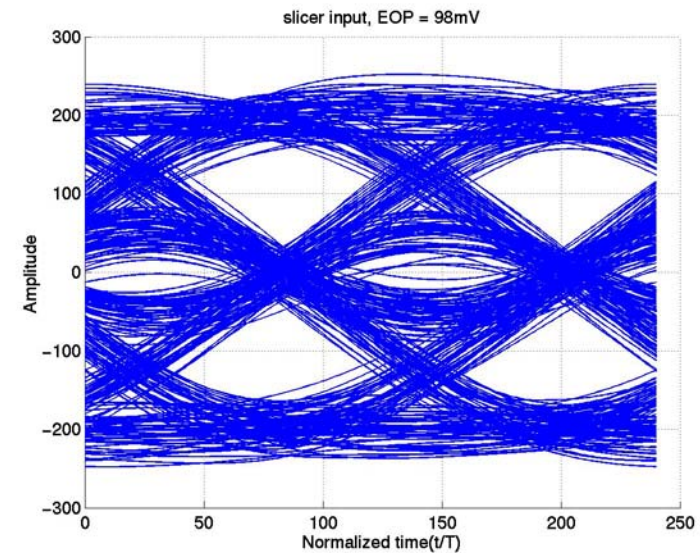
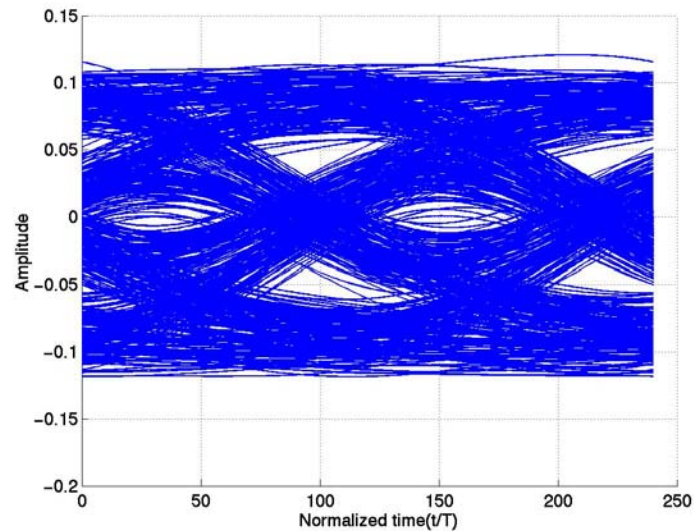


- ▶ Length: 10"+20"+10"
- ▶ Stub Bottom (or counter boring)
- ▶ Eye opening:
 - ▶ Vertical : 93 mv (margin = 4.56 mv)
 - ▶ Horizontal: 70 ps (4.4 ps)
- ▶ Pre-emphasis: 0.4

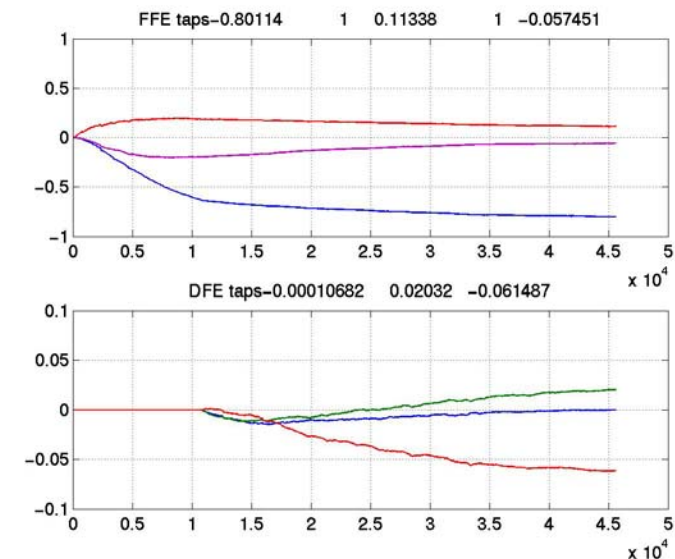


Simulation Results for Tyco ATCA Case4

VITESSE

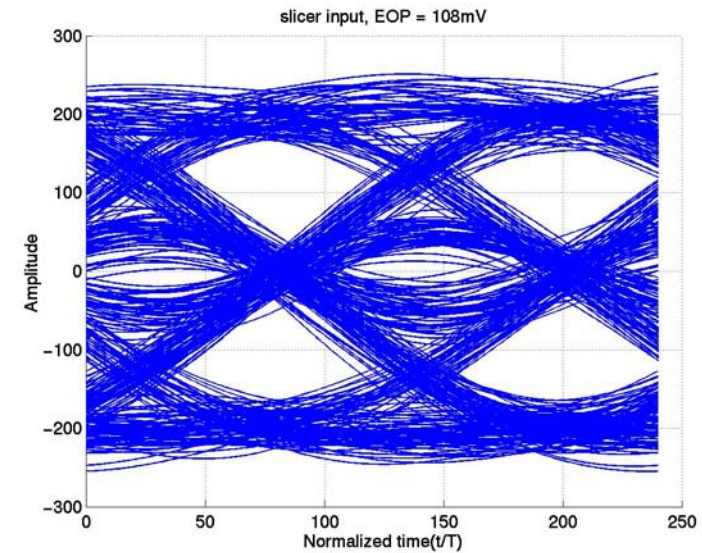
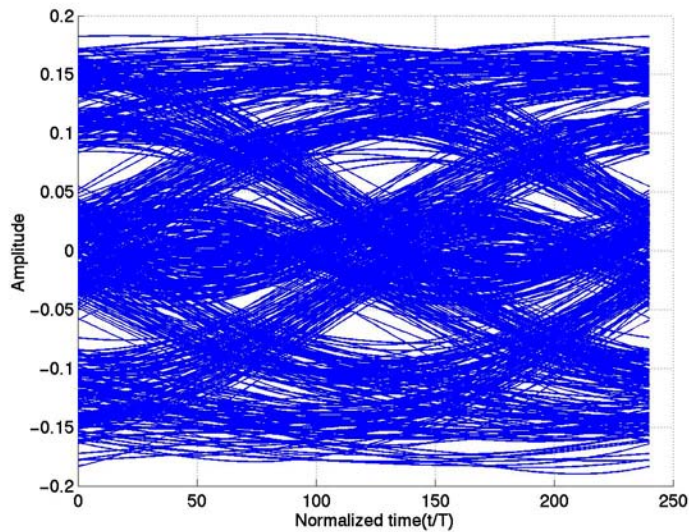


- ▶ Length: 10"+20"+10"
- ▶ Stub Bottom (or counter boring)
- ▶ Eye opening:
 - ▶ Vertical: 98 mv (margin = 4.87 mv)
 - ▶ Horizontal: 70 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0.3

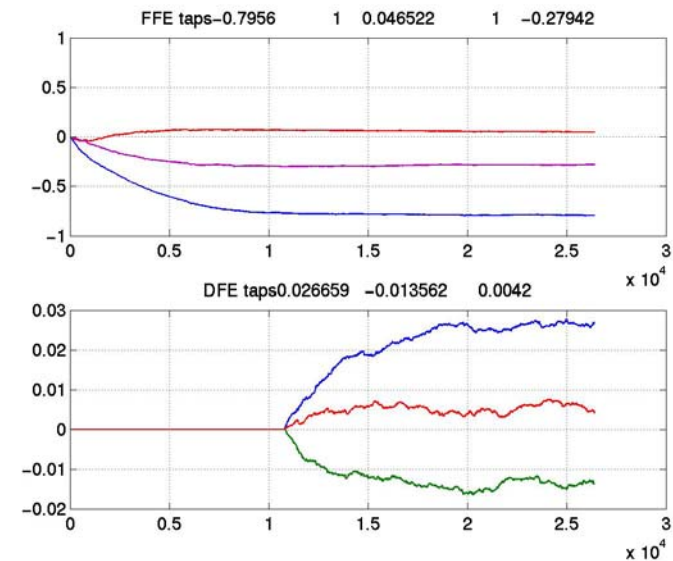


Simulation Results for Tyco ATCA case6

VITESSE

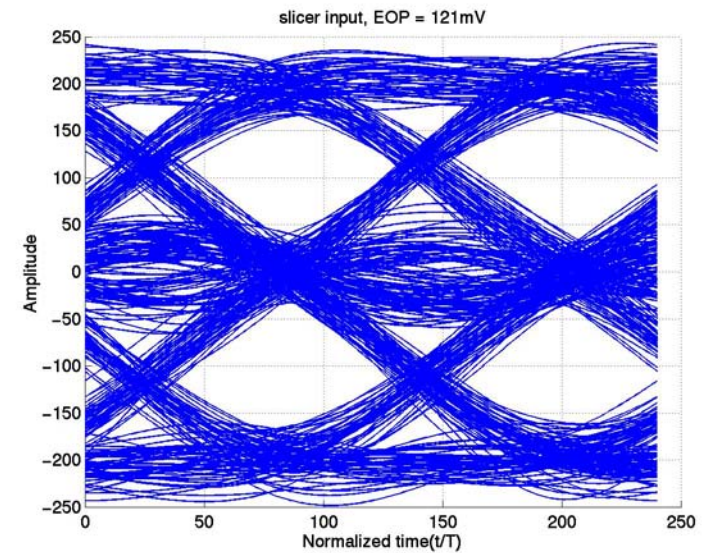
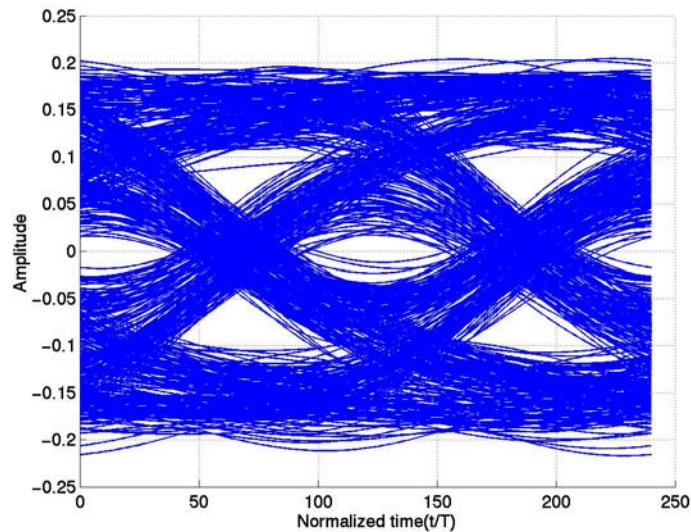


- ▶ Length: 6" + 10" + 6"
- ▶ Top Layer (with stub)
- ▶ Eye opening:
 - ▶ Vertical: 108 mv (margin = 5.5 mv)
 - ▶ Horizontal: 70 ps (margin = 4.4 ps)
- ▶ Pre-emphasis: 0

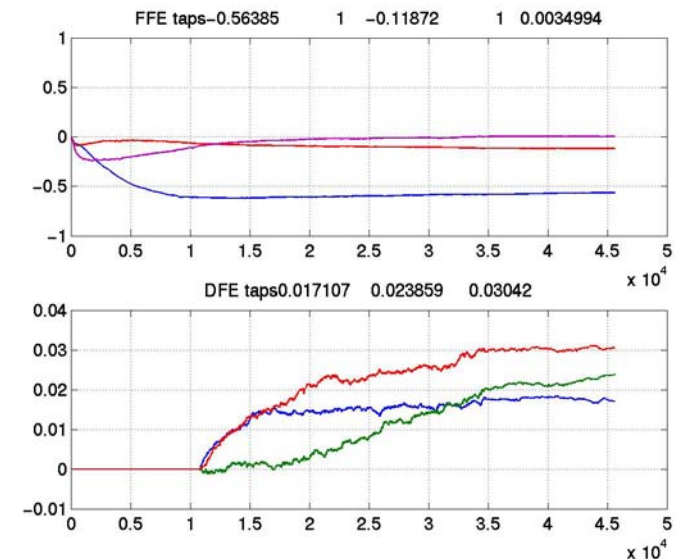


Simulation Results for Tyco ATCA case7

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- ▶ Length: 6"+1"+6"
- ▶ Near Top layer (with stub)
- ▶ Eye opening:
 - ▶ Vertical: 121 mv (margin = 6.3 mv)
 - ▶ Horizontal : 75 (margin = 4.7 ps)
- ▶ Pre-emphasis: 0



- ▶ ATCA Backplanes provided by Intel and Tyco can be equalized with reasonable complexity, using duobinary modulation to achieve BER of $1e-15$.
- ▶ A 5-tap feed-forward equalizer cascaded with 3-tap DFE can be used at the receiver to achieve good performance.
- ▶ To support long channels (40"), a simple one-tap pre-emphasis at transmitter is required.