Channel Design Parameter Impact on the SDD21 and Pulse Response

The purpose is to characterize effects of real design parameters on channel performance

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November 16, 2004

Enterprise Platforms Group

Supporters

- Pravin Patel, IBM
- John D'Amborsia, Tyco Electronics

Message

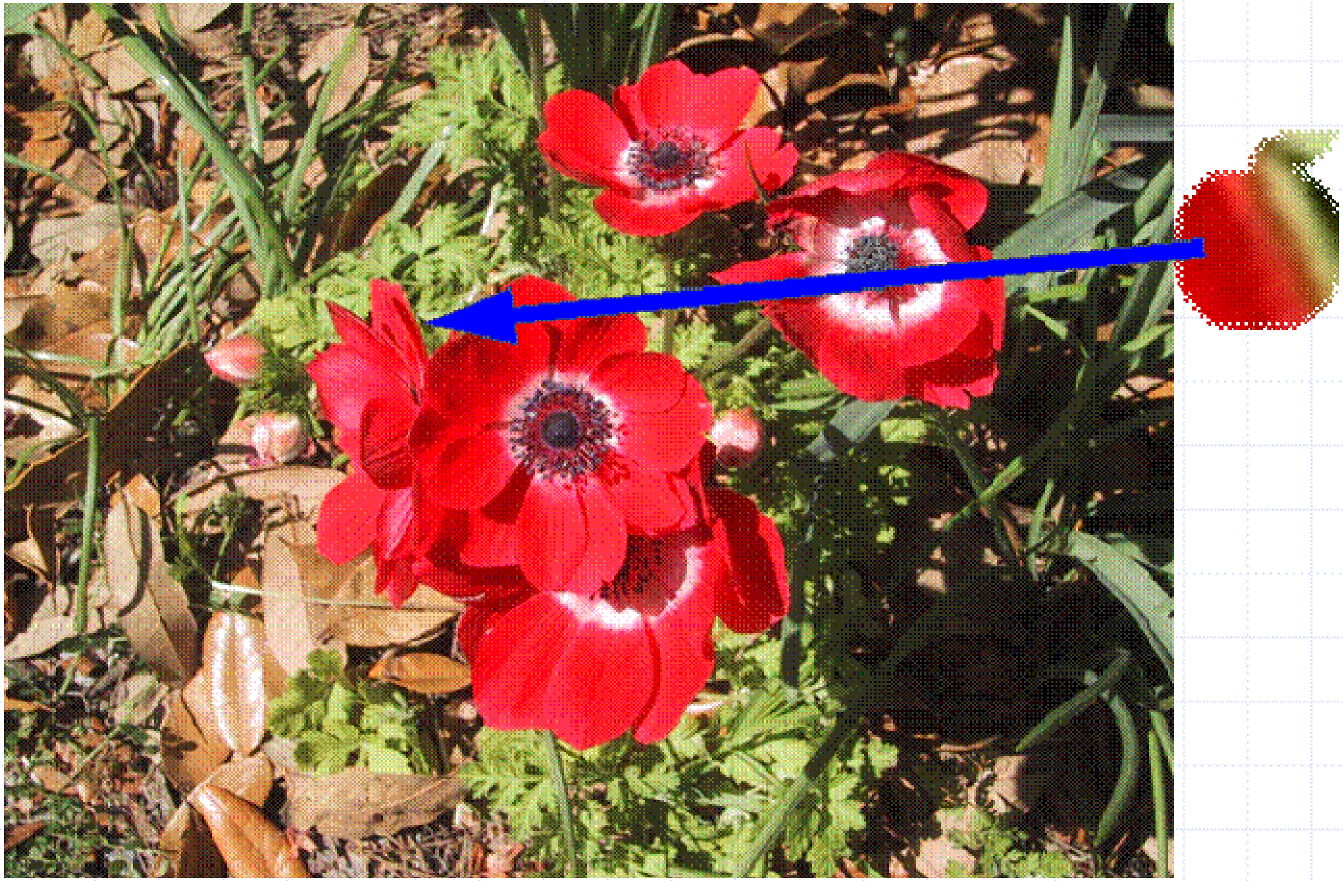
- Board material and channel length are only "part" of a design
- Via stubs and connectors have a significant impact
  - Via stubs cause issues for equalization even if we are above a loss curve.
- Impedance mismatches have a much smaller effect.
- Legacy design practices can achieve 10Gb performance if the entire physical design is managed
  - However there will be challenges for silicon too!

Goal:

- Determine relation between performance channel design parameters such as
  - differential via structures
  - impedance mismatches
- These features are expected to alter the following (and thus performance)
  - Frequency domain properties
  - Pulse response properties
- Not considered here: … YET
  - Connectors
  - AC coupling cap structure
  - Power/Reference plane anomalies
  - Crosstalk

Goal: Show trends and magnitude of design choices

Paint an impressionistic picture: not pixels



Process

- Create structure that resonate

1. For impedance
   - Adjusting impedance and lengths
   - This creates SDD21 ripple
2. For vias
   - Adjusting stub length and pad stack
   - This creates SDD21 notches

- For these pathological cases
  - correlate design features, frequency domain characteristics, and pulse response.
  - Perform analysis independently
- Caveat: These effects will interrelate
  - Not covered here
  - Job of the board designer is to manage

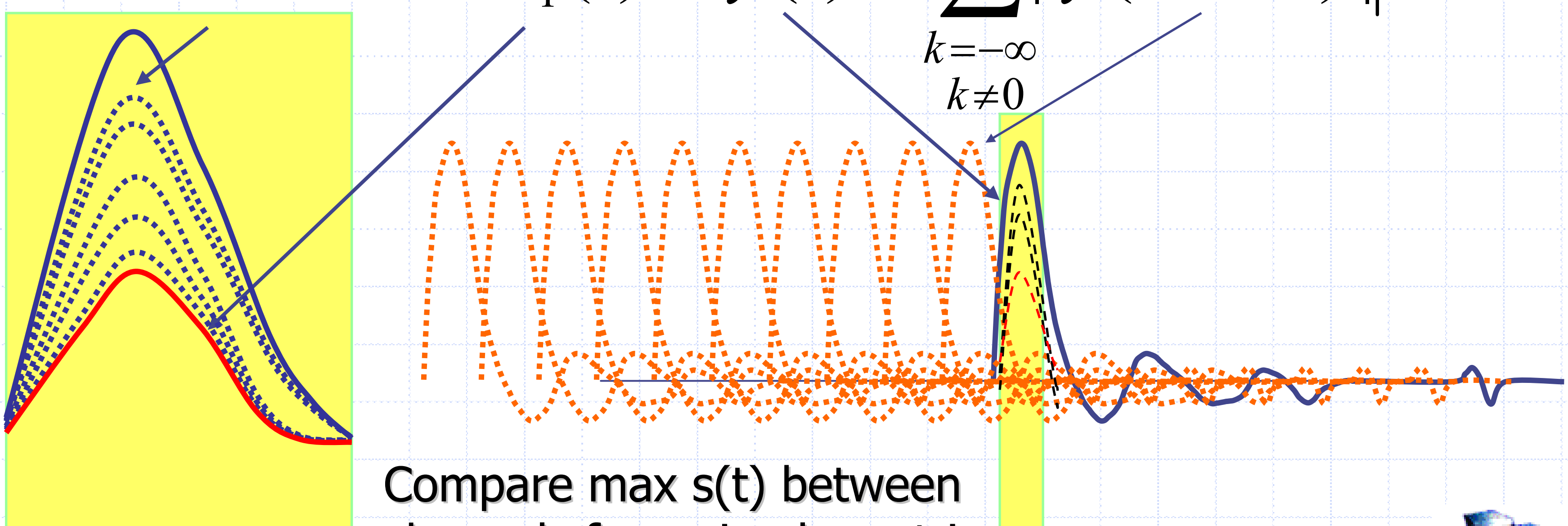
Evaluation and Design Practices

- Without getting into signaling issues, we can access the relative signaling challenges with pulse response using partial pulse convolution.
  - Pulse convolution is a worst case analysis and its expected that equalization will compensate for at least part of this. (see next slide)
- Three pulse characteristics can also be examined
  - Pulse height (Reference is 1V)
  - Near end ringing (1 UI to 2UI)
  - Settling
- For Common Place Design Practices
  - Determine what choices can be made to mitigate negative pulse response effects.

Partial Lone Pulse Response Convolution

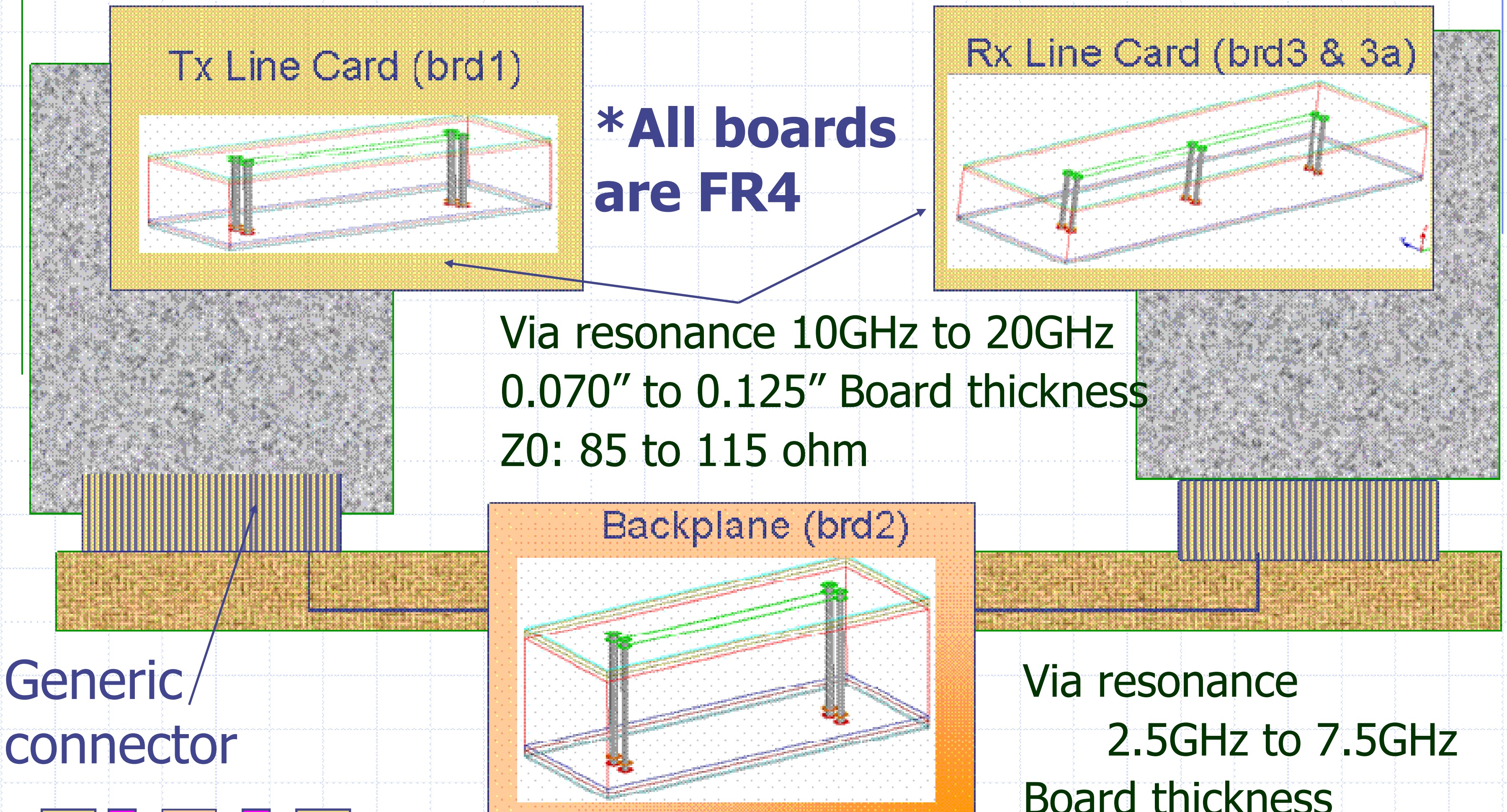
- Just a simple method to compare one channel against another
- Encompasses long ringing and losses

$$s_1(t) = y(t) - \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} | y(t-kT) |$$



Compare max s(t) between channels for a simple metric

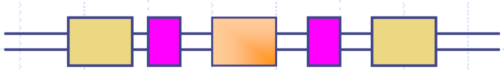
Topology



***All boards are FR4**

Via resonance 10GHz to 20GHz
0.070″ to 0.125″ Board thickness
Z0: 85 to 115 ohm

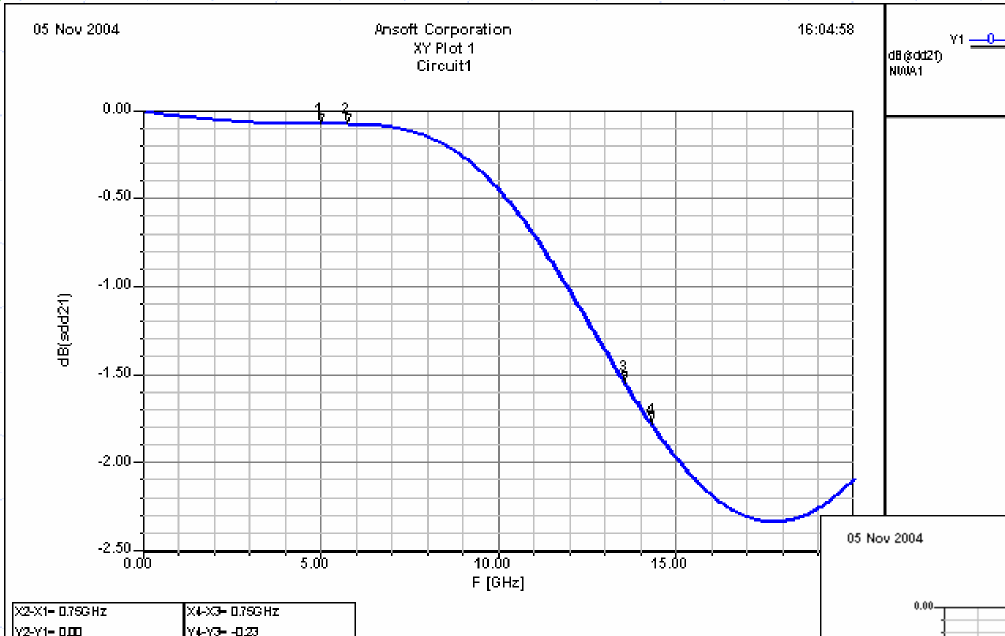
Via resonance
2.5GHz to 7.5GHz
Board thickness
0.150″ to 0.300″
Z0: 90 to 110 Ω



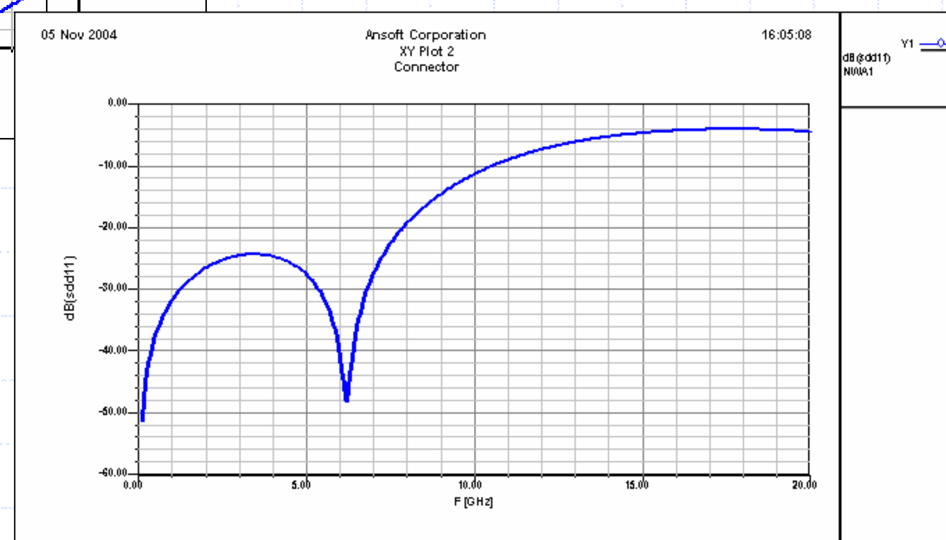
Equal segment lengths
Total line length: 9″ to 37″

Generic Connector Example

SDD21



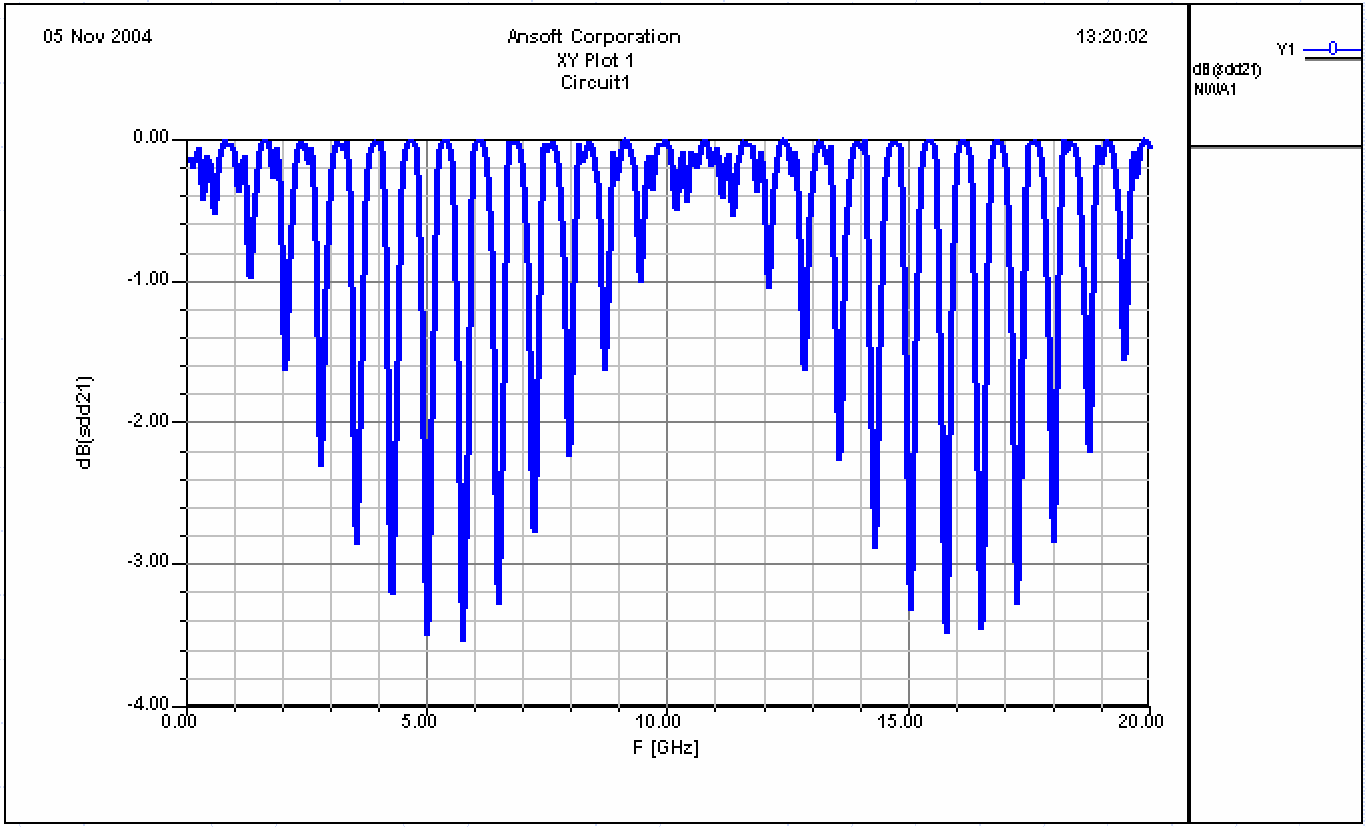
SDD11



Getting a feel for mismatch performance

- Here are simplifying assumptions to get an idea of what's going on
  - First, consider system with no AC losses and no vias
  - Lengths are all the same for all board segments
  - Connectors are 0.3885"
  - Length chosen with formula, lambda*factor, to see if specific resonance has an impact
  - Length range between 9 and 37 inches

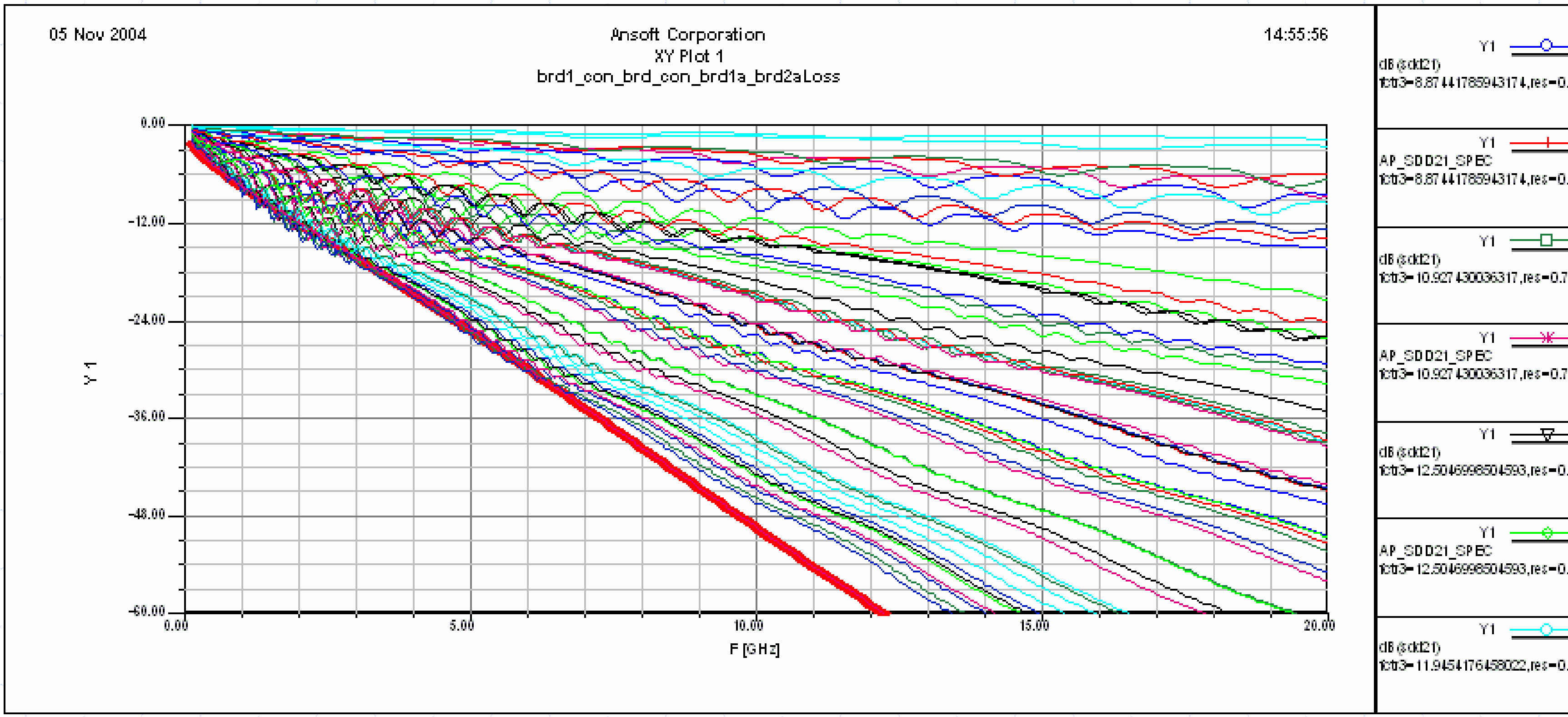
Example Mismatch Response - lossless



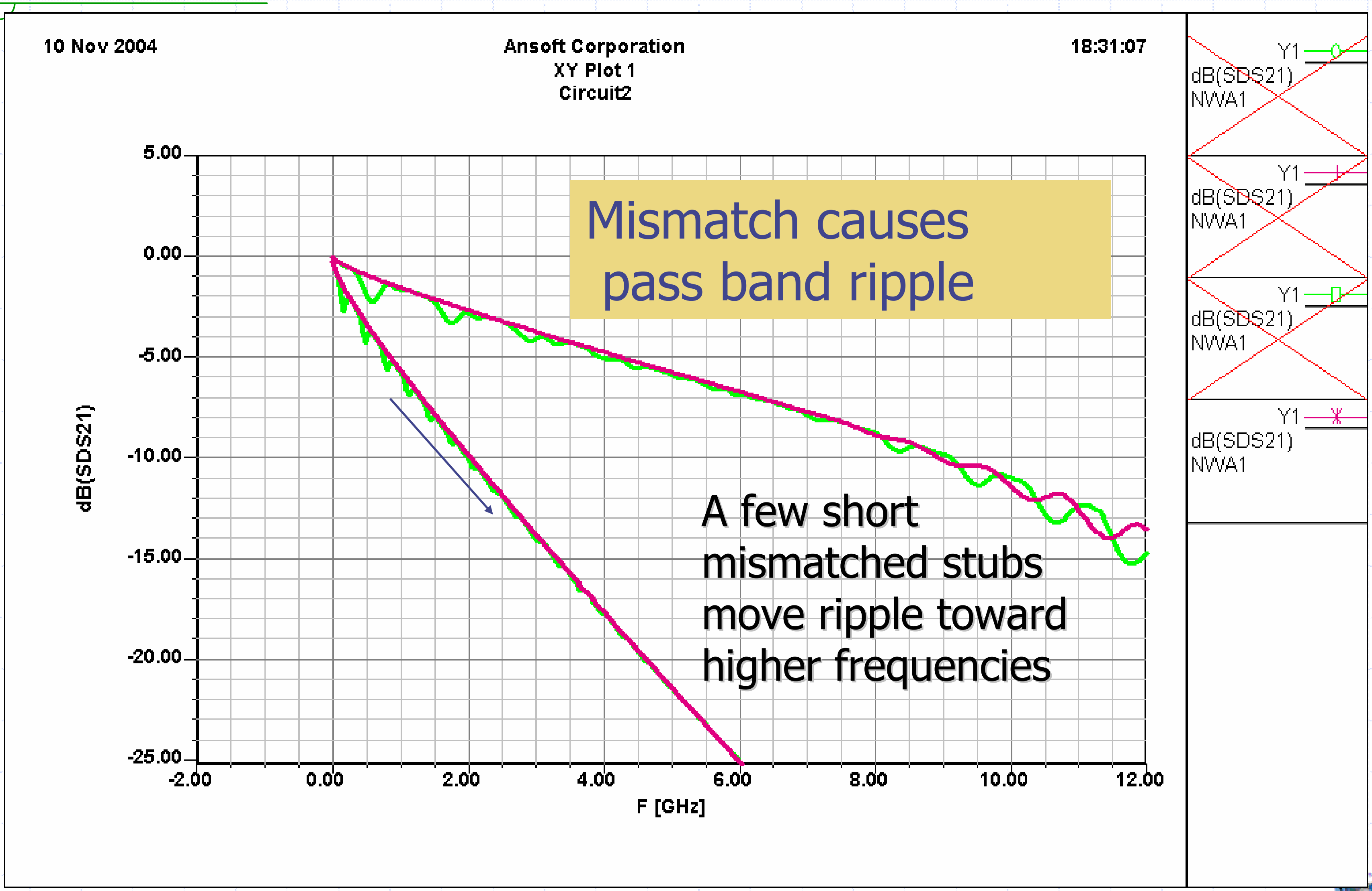
- About 3dB ripple that's has a HF component at 750 MHz period

Example of sub responses in range

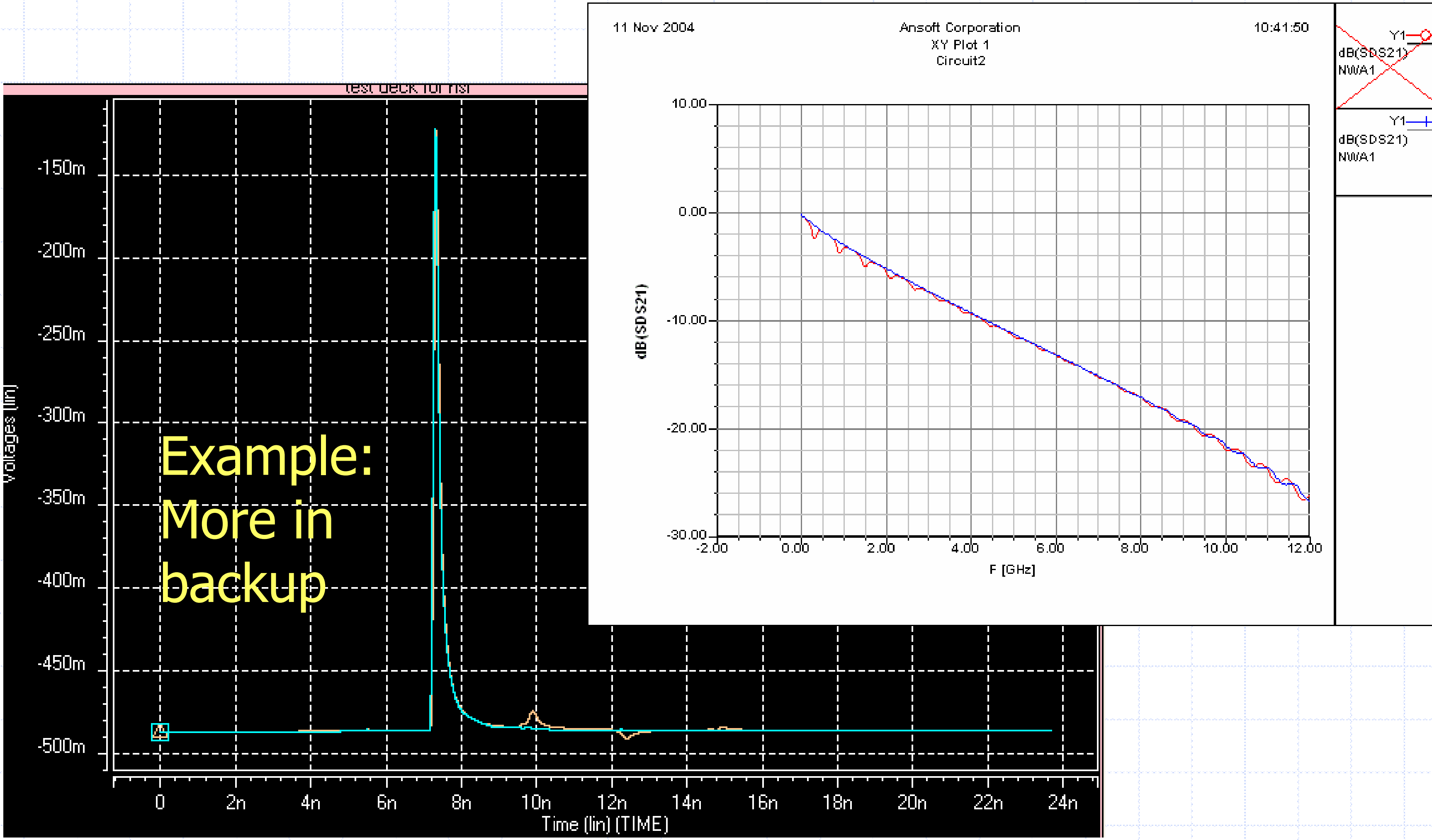
- Adding mismatch to the selection of lossy lines



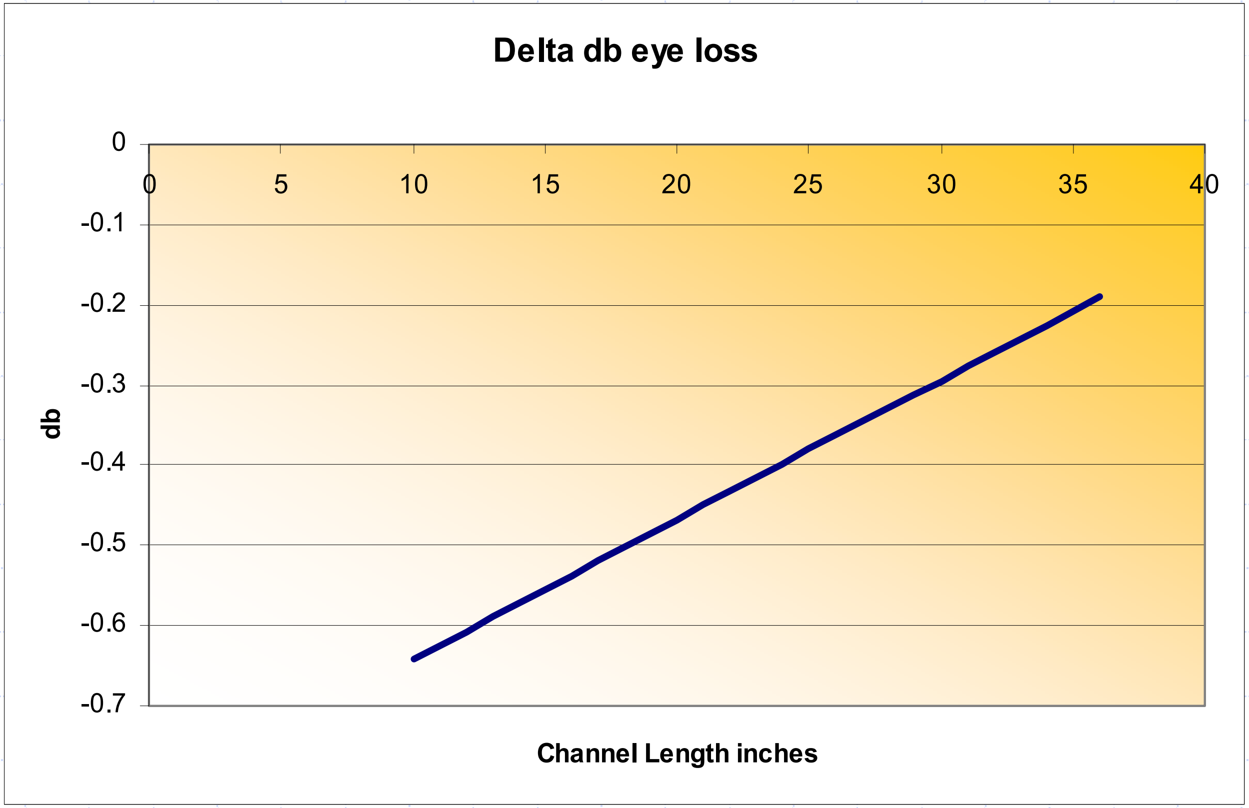
Long vs short line: SDD21 w/wo mismatch



19 inch channel w/wo mismatches



Ripple/Mismatch Convolution Results



- Longer lines have less <u>eye opening impact</u> due to impedance induced ripple
- This ripple is cause by +/- 15% Z0 line card tolerance

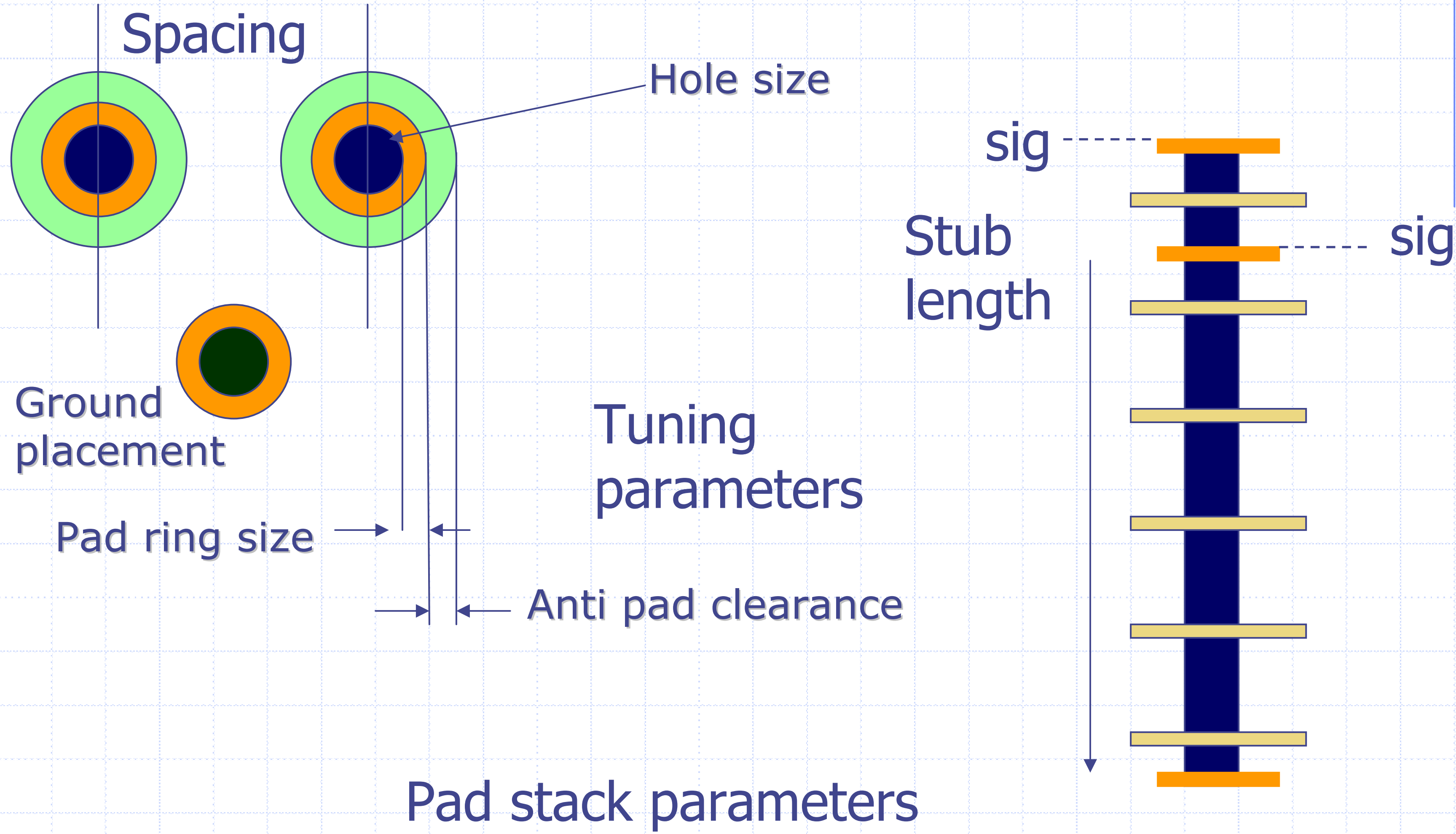
Mismatch Conclusions

- Eye closure is between 0.3 dB and 0.6 dB from board tolerance.
- Packages have much more return loss in the pass band and may present big problems not yet considered.
- At least some of this can be fixed with equalization.
- Mismatch is not a real big issue as long as the system is not at the brink of failure
- Board mismatch effects do not justify pass band ripple requirement.
  - More on this later when we talk about vias
- Connectors with excessive mismatch potentially could justify a pass band ripple requirement.

Via Effects

- Via stubs cause frequency notches
- Review structures
- Compare via parameters and frequency domain characteristics.
  - Use mixture of measurements, behavioral models, and full wave EM solutions.

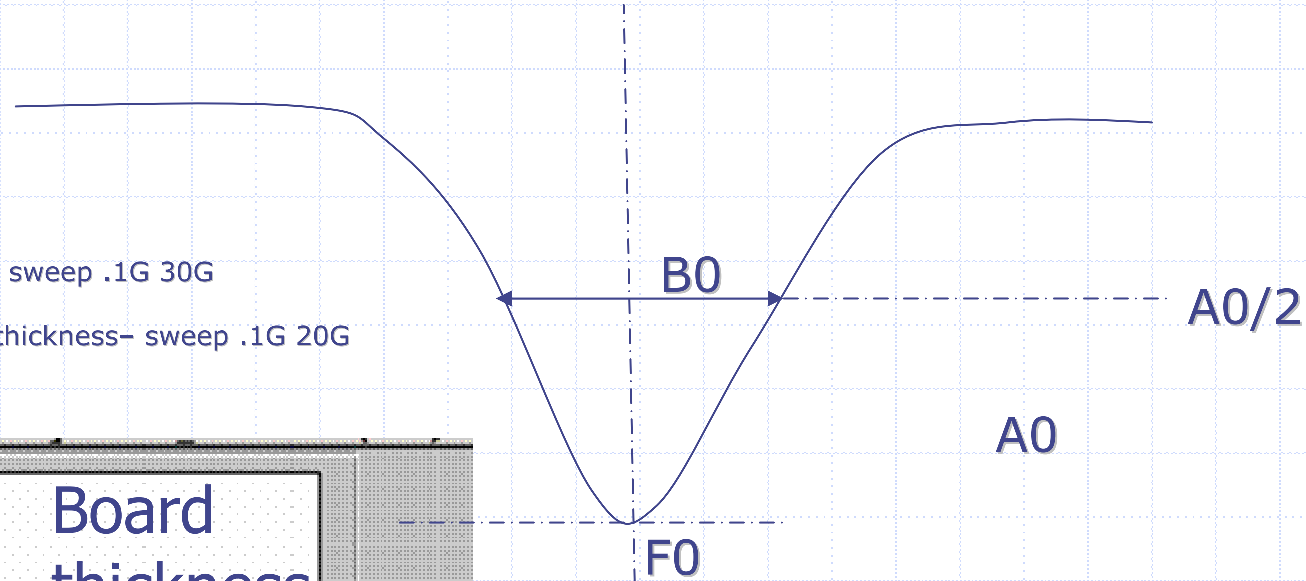
Example of Via Tuning Parameters

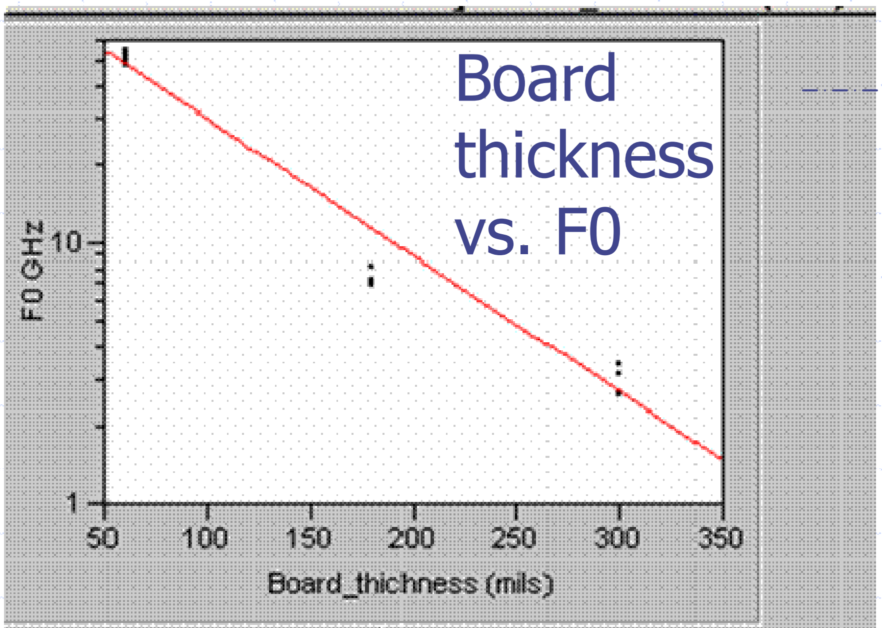


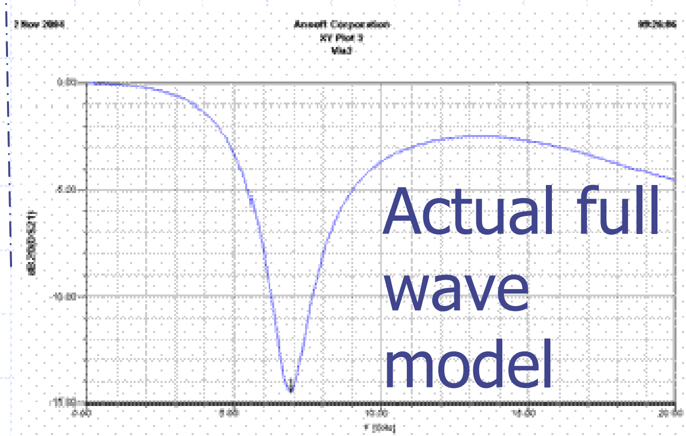
Via measurements – F0 fits a log stub curve

60 mil thickness– sweep .1G 30G

180 and 300 mil thickness– sweep .1G 20G

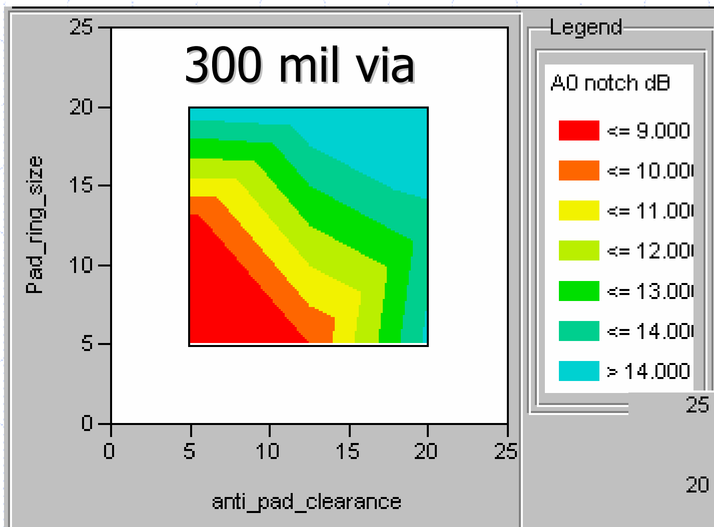


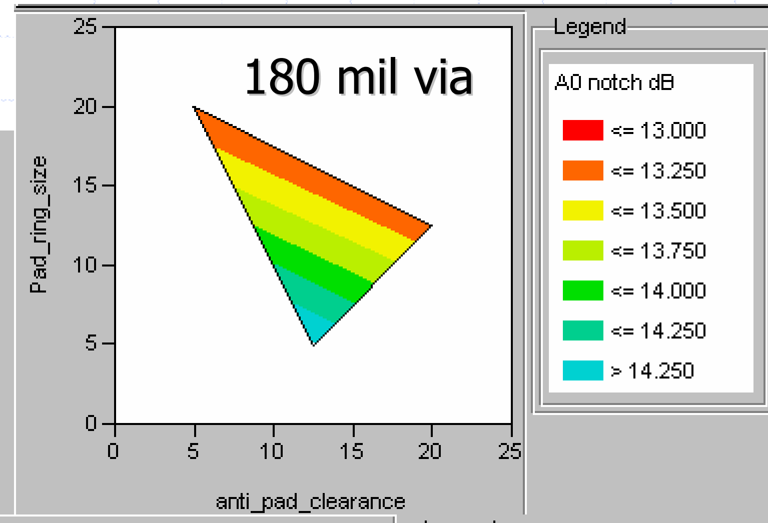


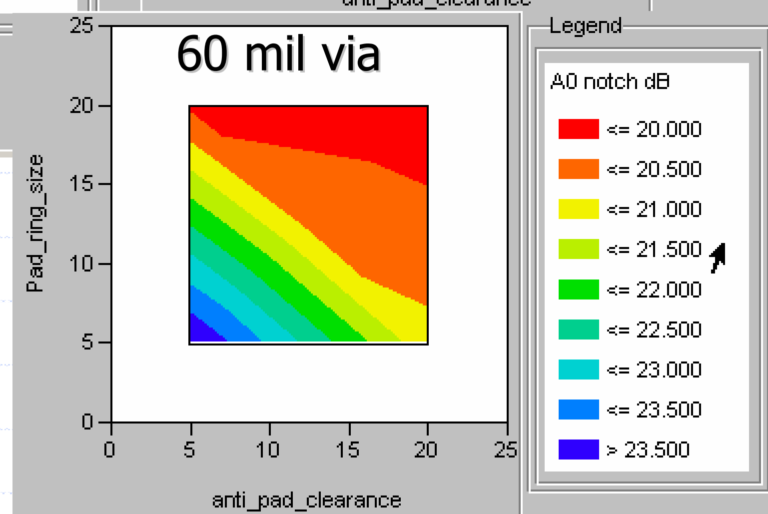


Notch Depth

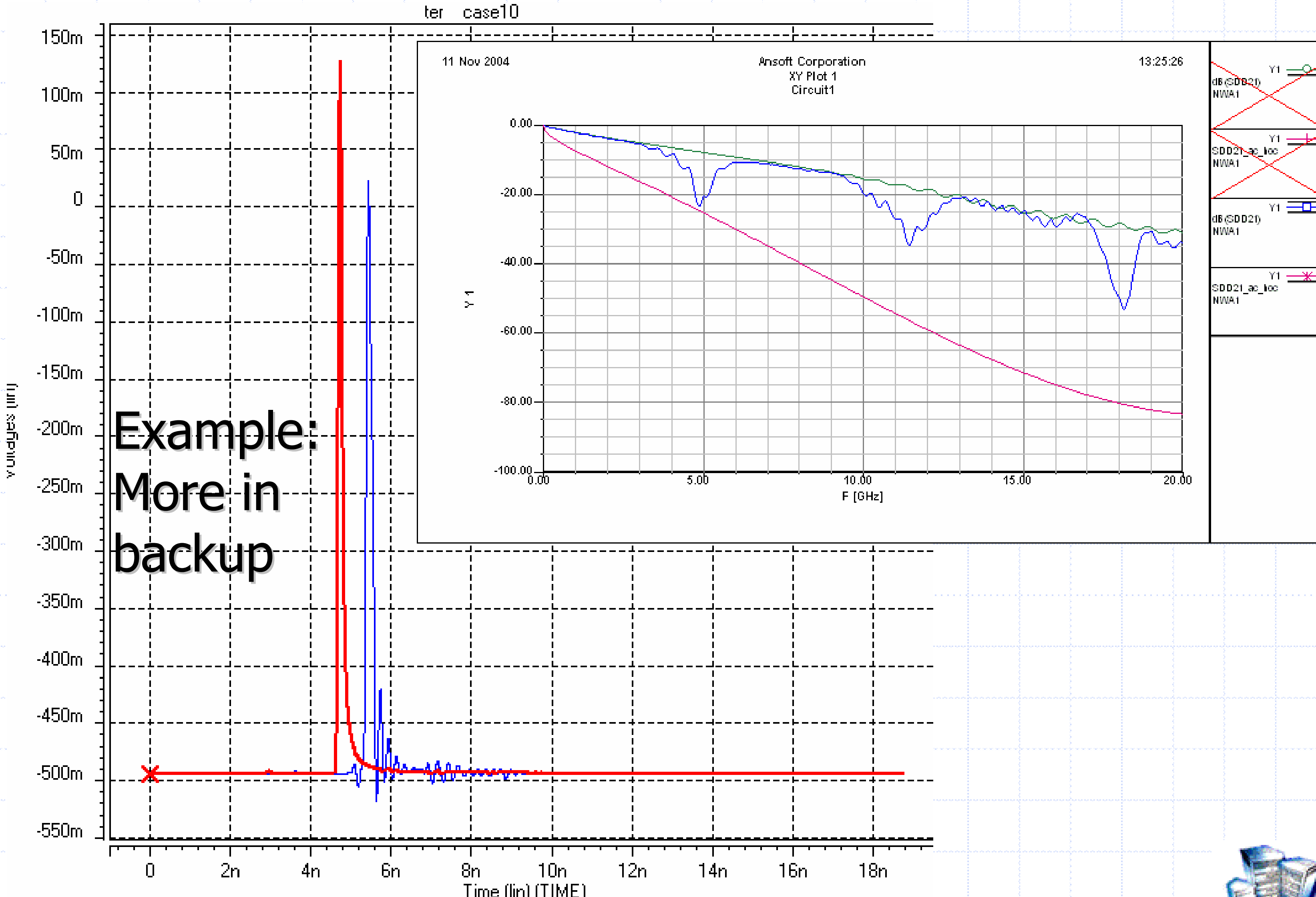
- 1 to 3 db can be adjusted with pad stacks





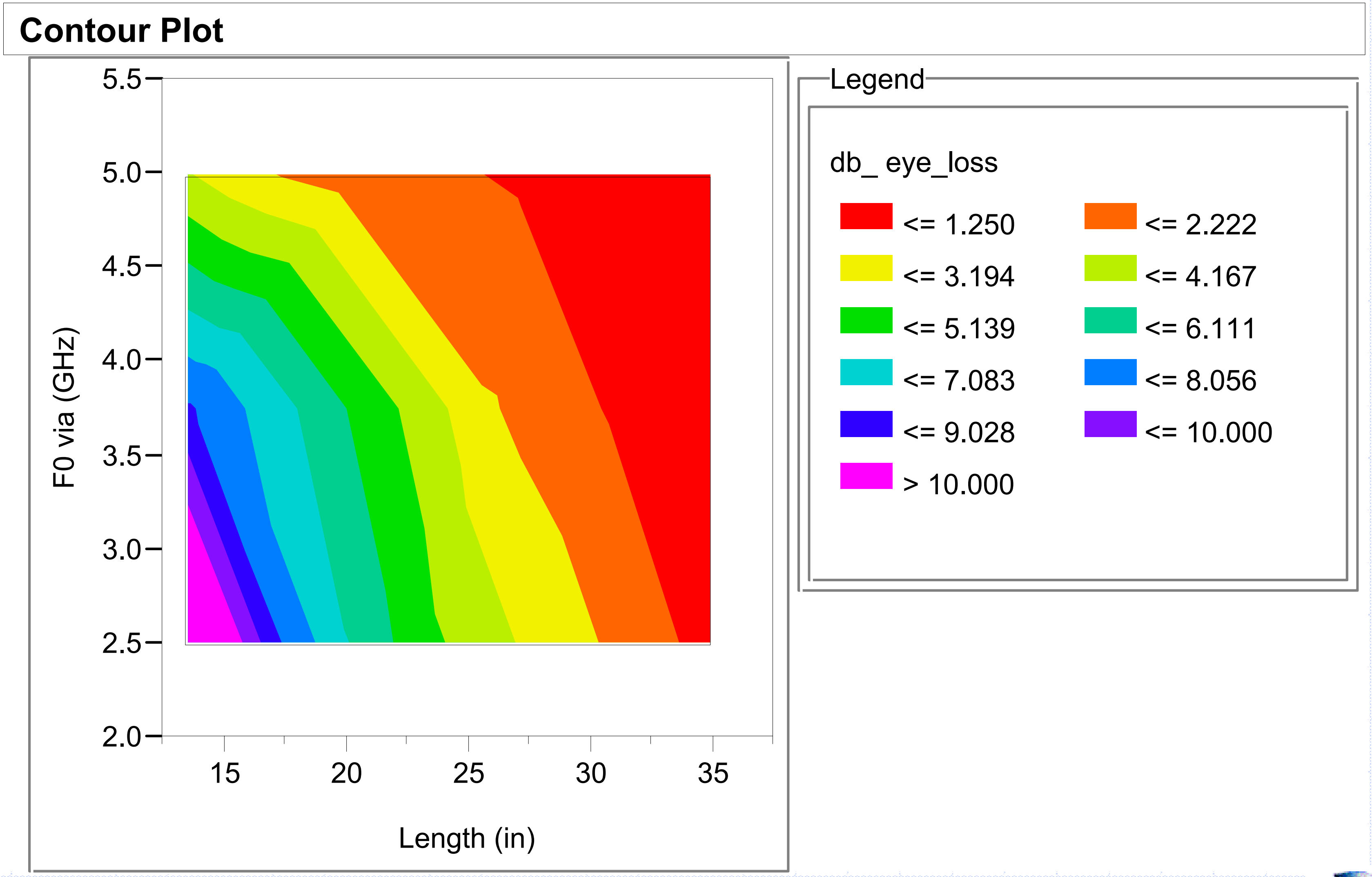


13 in line with via notch at 5 GHz

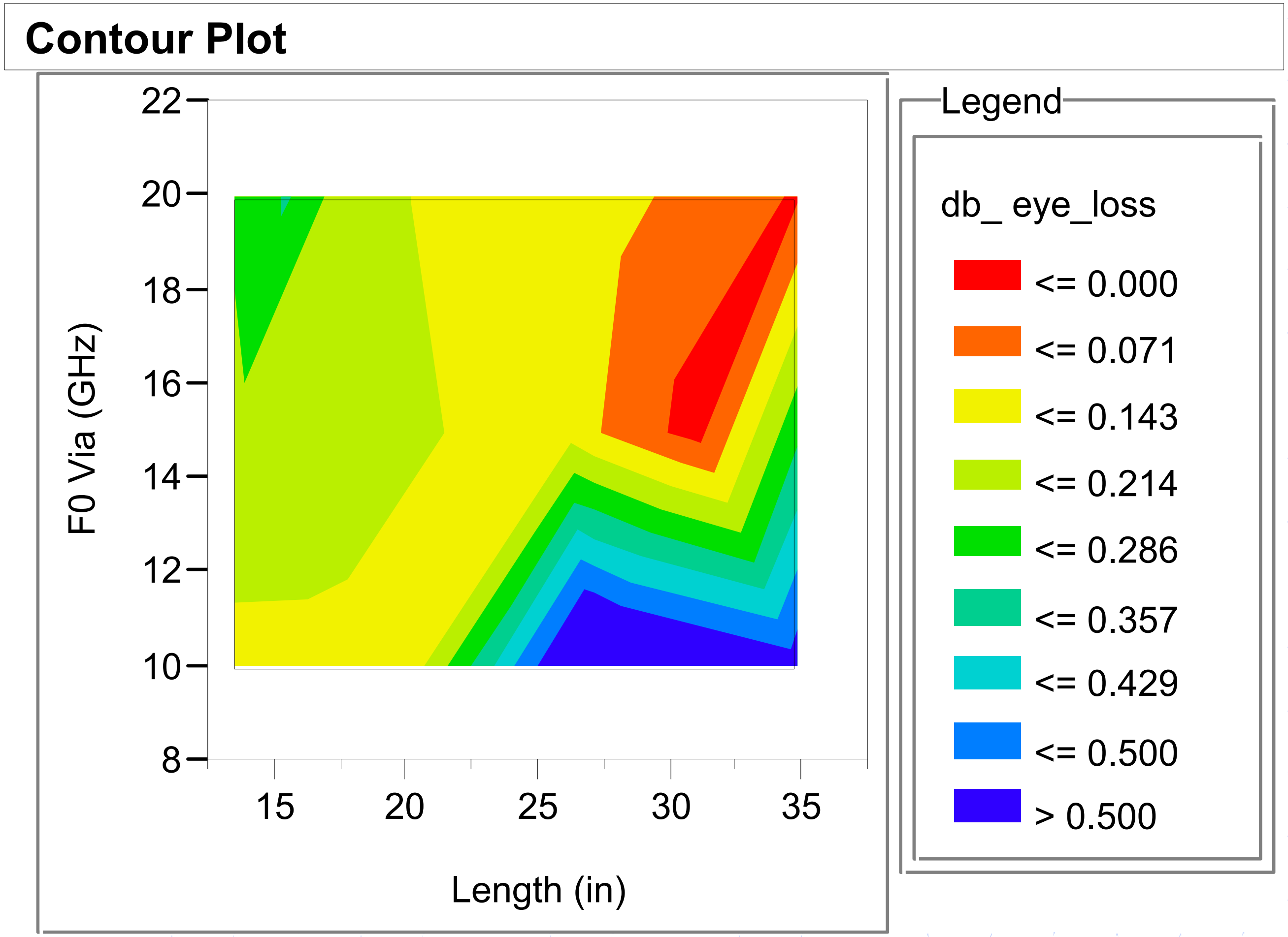


Example:
More in backup

Profile of eye loss vs. length and F0



Vias notches at high frequency have little effect



Via Stub Conclusions

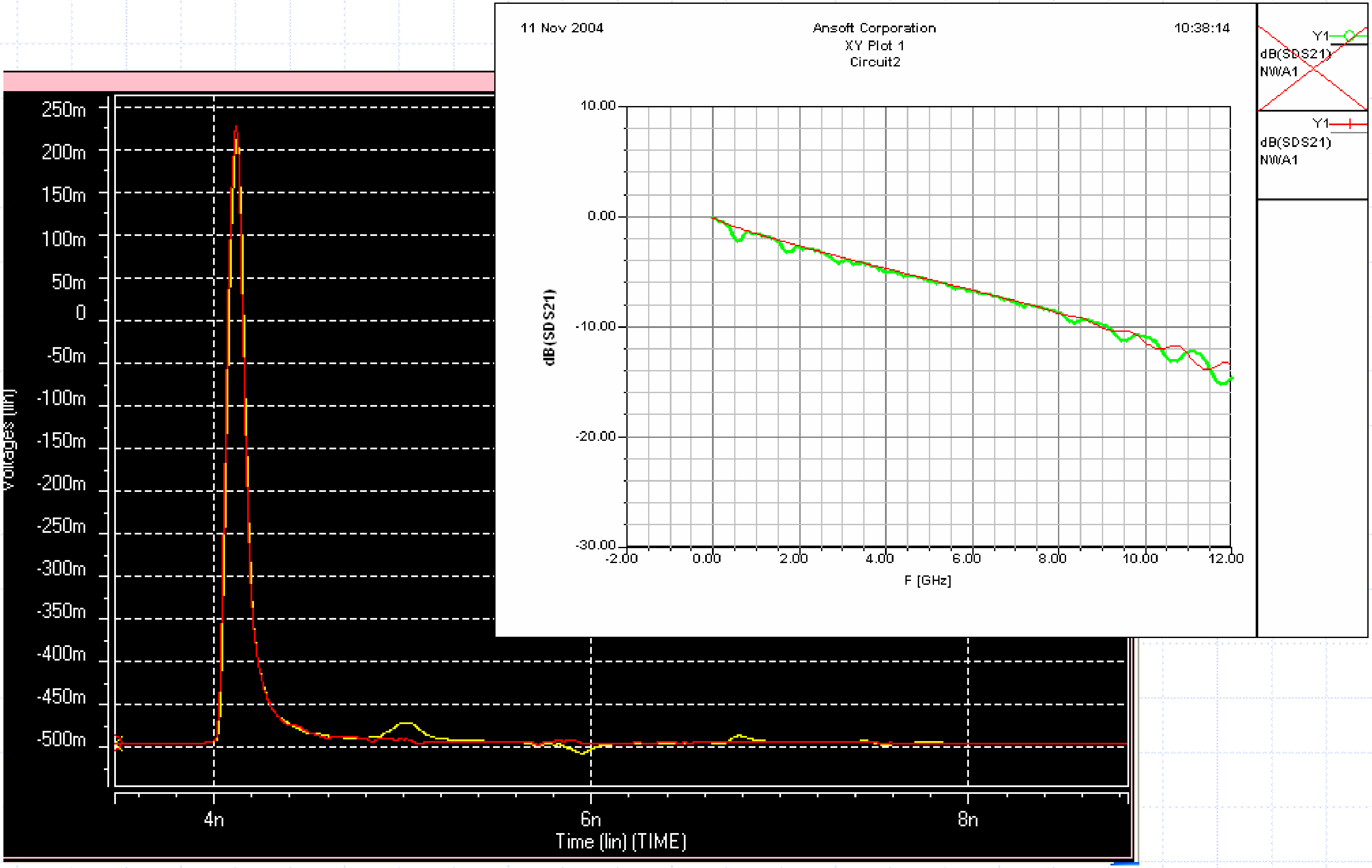
- Eye closure due to a via is between 1 and 10 dB
- Via notch depth:
  - Between 4 and 12 dB
    - Longer vias have deeper notches
    - Pad construction can reduce notch depth a maximum of 3 dB
- Effects due to a particular line wavelength resonance are not noticeable.
  - Only total segment length is important.
- At least some of this can be fixed with equalization.
- Via stubs may be manageable
  - Not real big issue as long as the system is not at the brink of failure
  - The log of stub length controls notch frequency (F0)
- Vias can cause pulse response to ring 40 to 60 UI out
- Via stub effects do justify pass band ripple requirement.
- Sharp notches above Nyquist rate have little effect
- It is possible that connectors could have a similar impact as vias do, so connector selection is very important.

Legacy Design Can Be Controlled to Limit

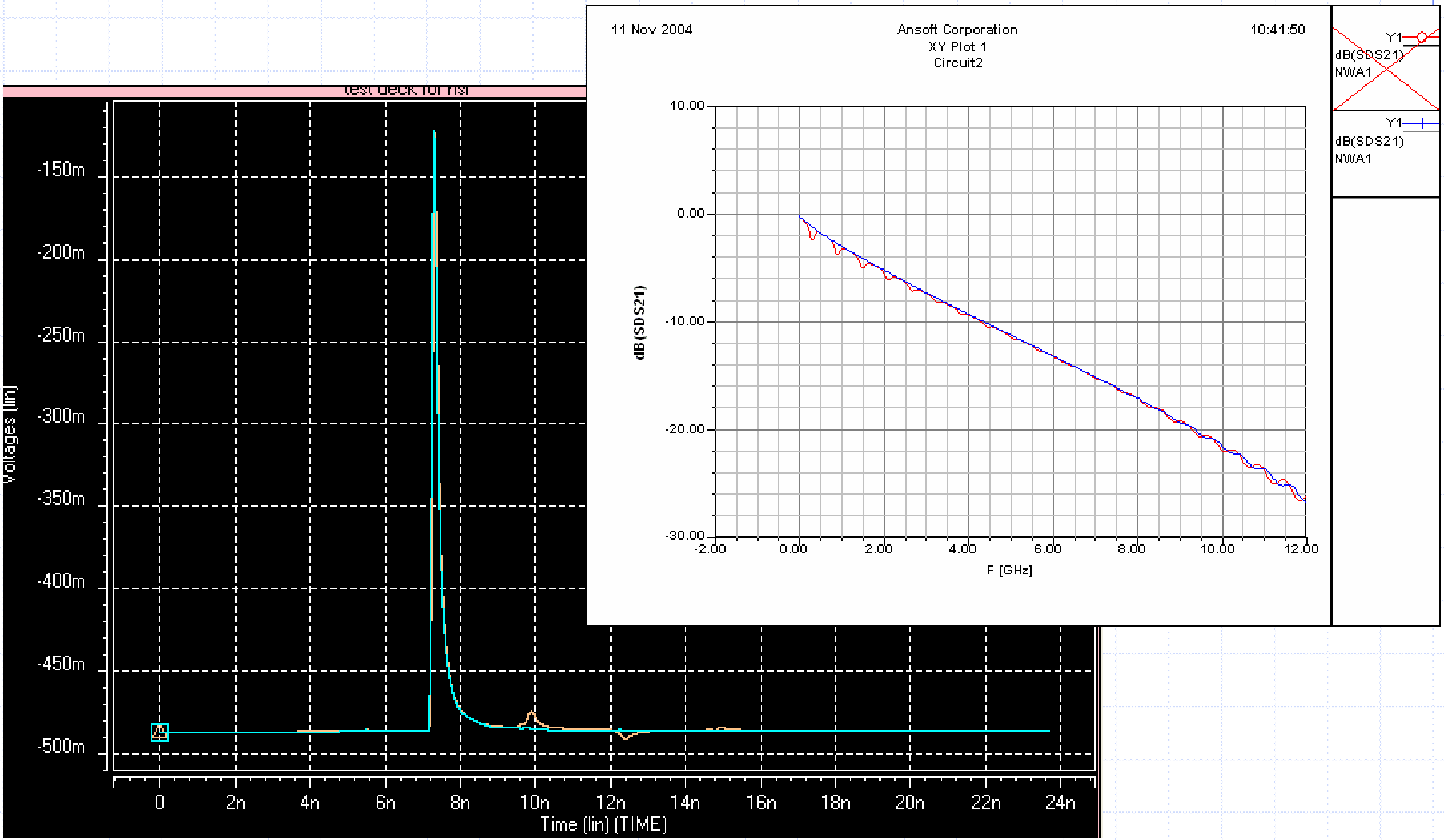
- Pass band ripple seems to be the simplest parameter to observe that directly impacts performance
- Large notches are caused by vias
  - Notches can be adjusted to mitigate effect
  - But only a little bit
- Legacy designs practices that have notches above Nyqusit do not effect pulse response.
- The above is the basis for some slight modifications to the SDD21 spec
- There are challenges for silicon… next

backup

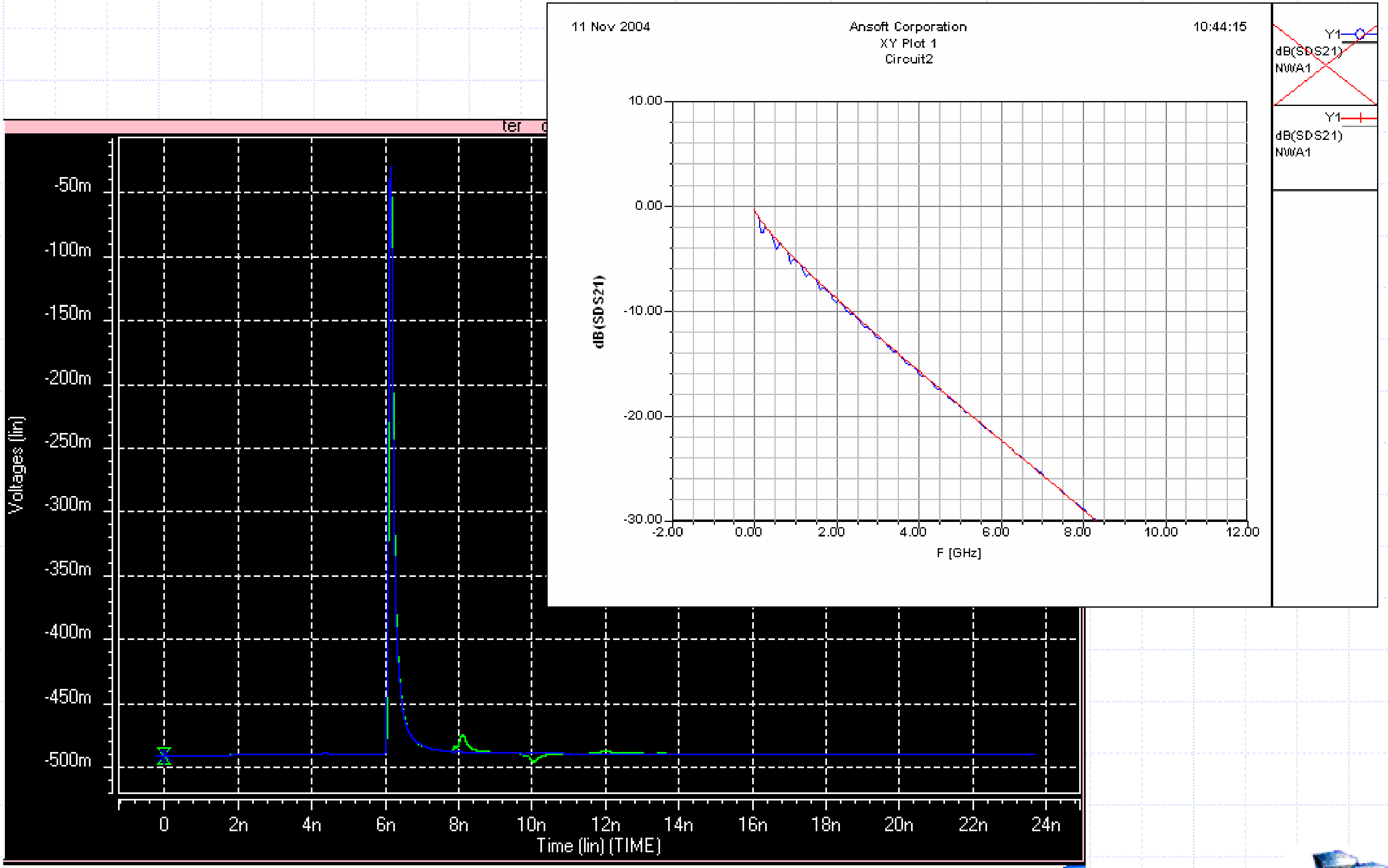
9 inches of channel w/wo mismatches



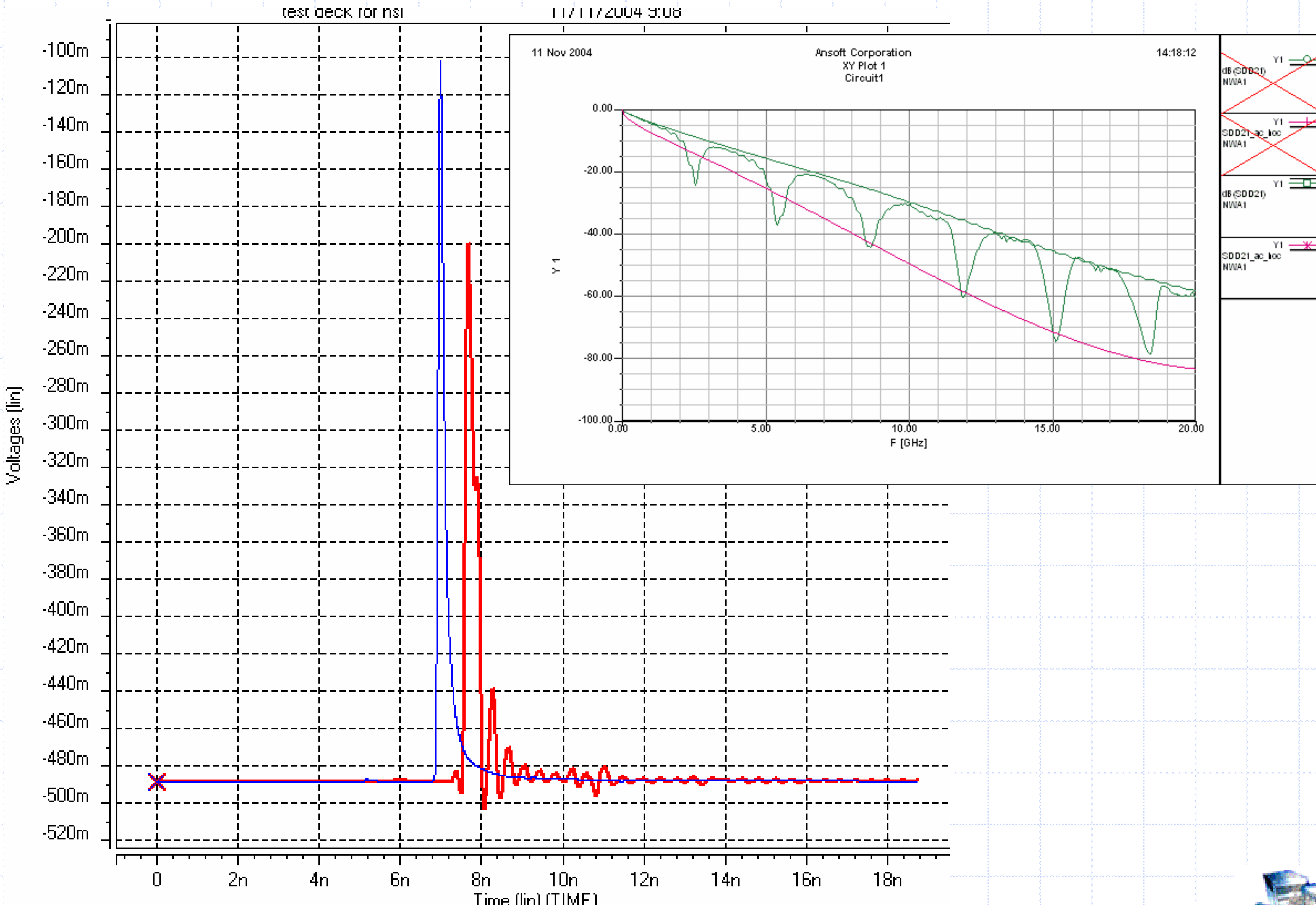
19 inch channel w/wo mismatches



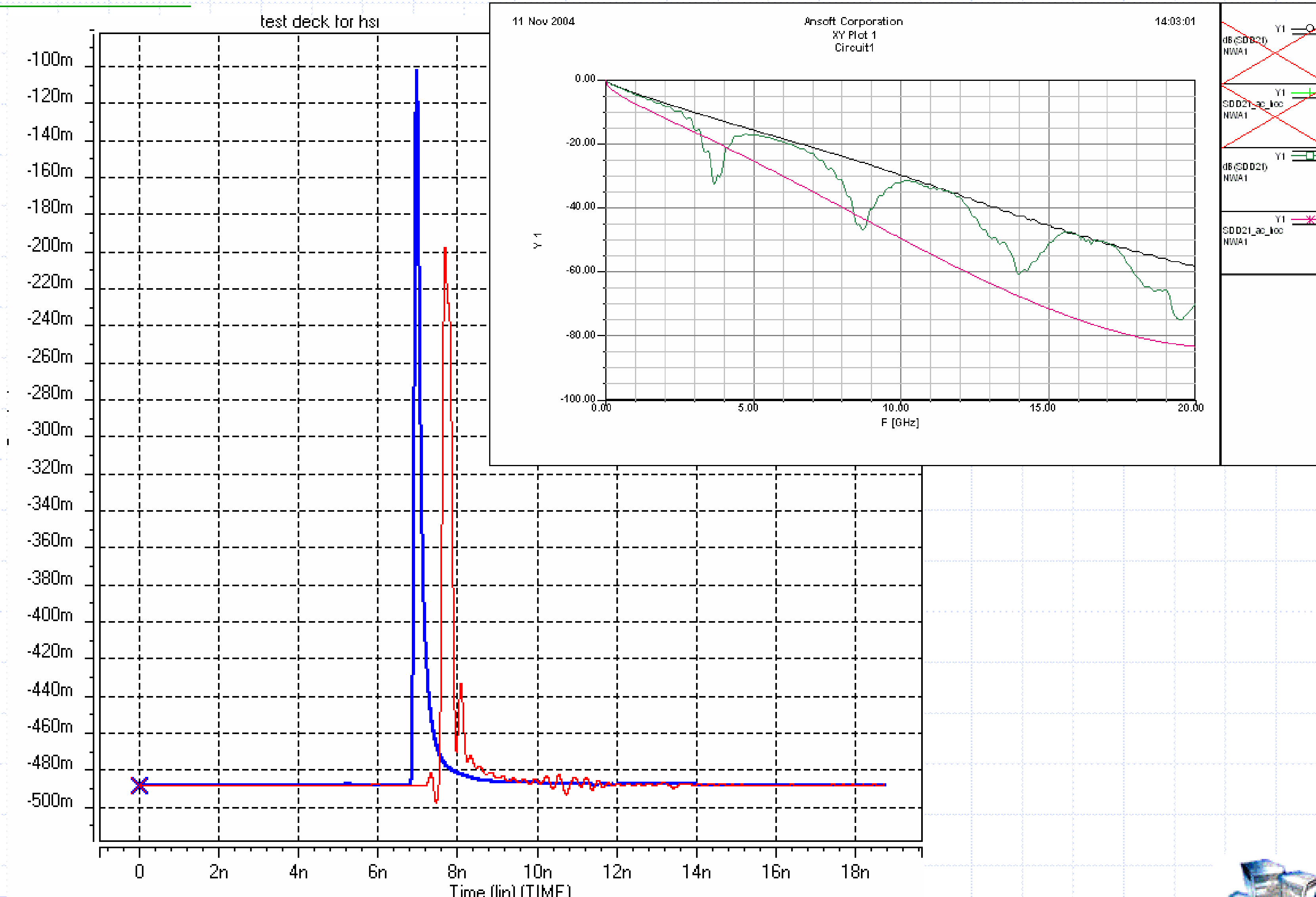
33 inch channel w/wo mismatches



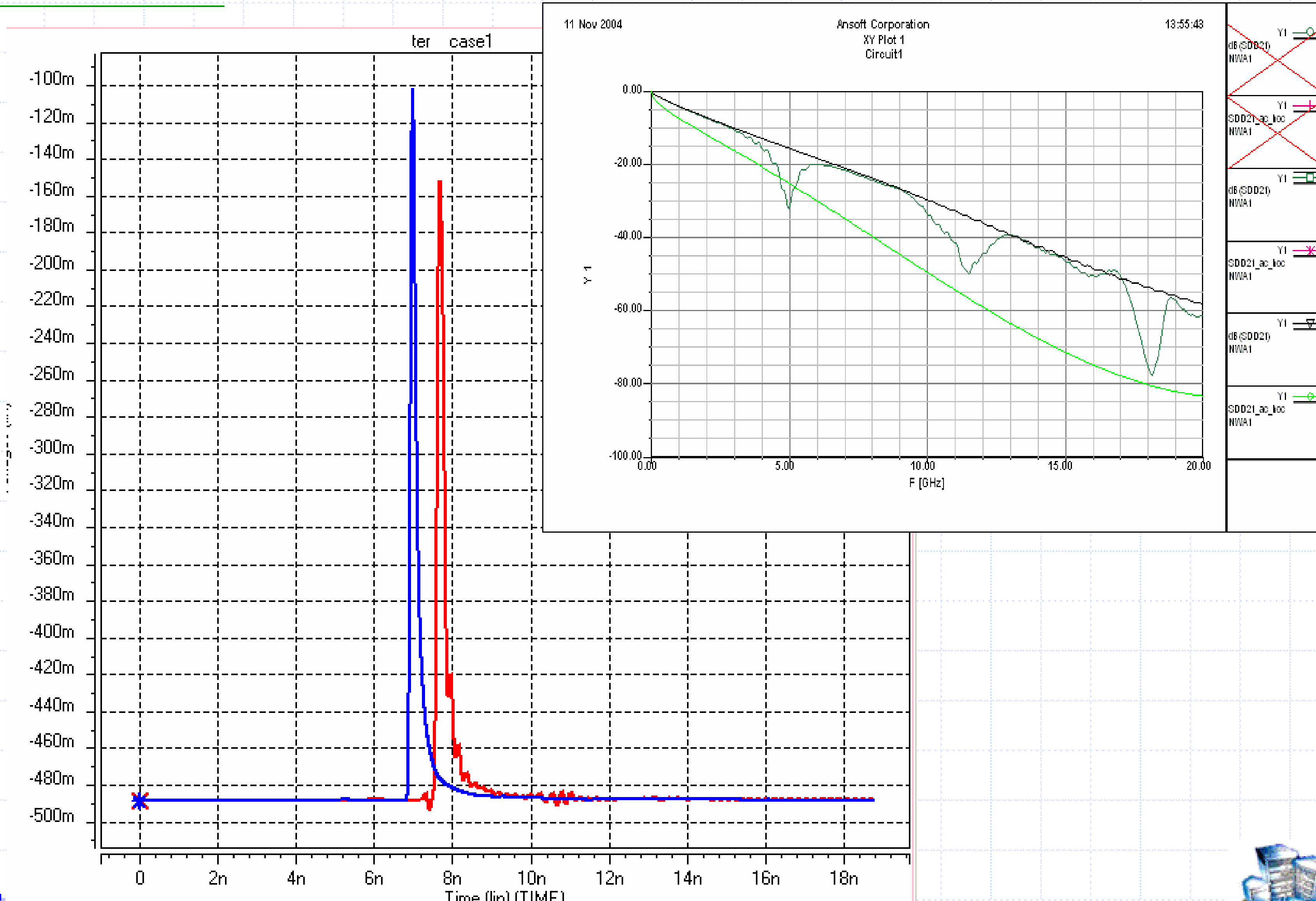
27 in line with via notch at 2.5 GHz



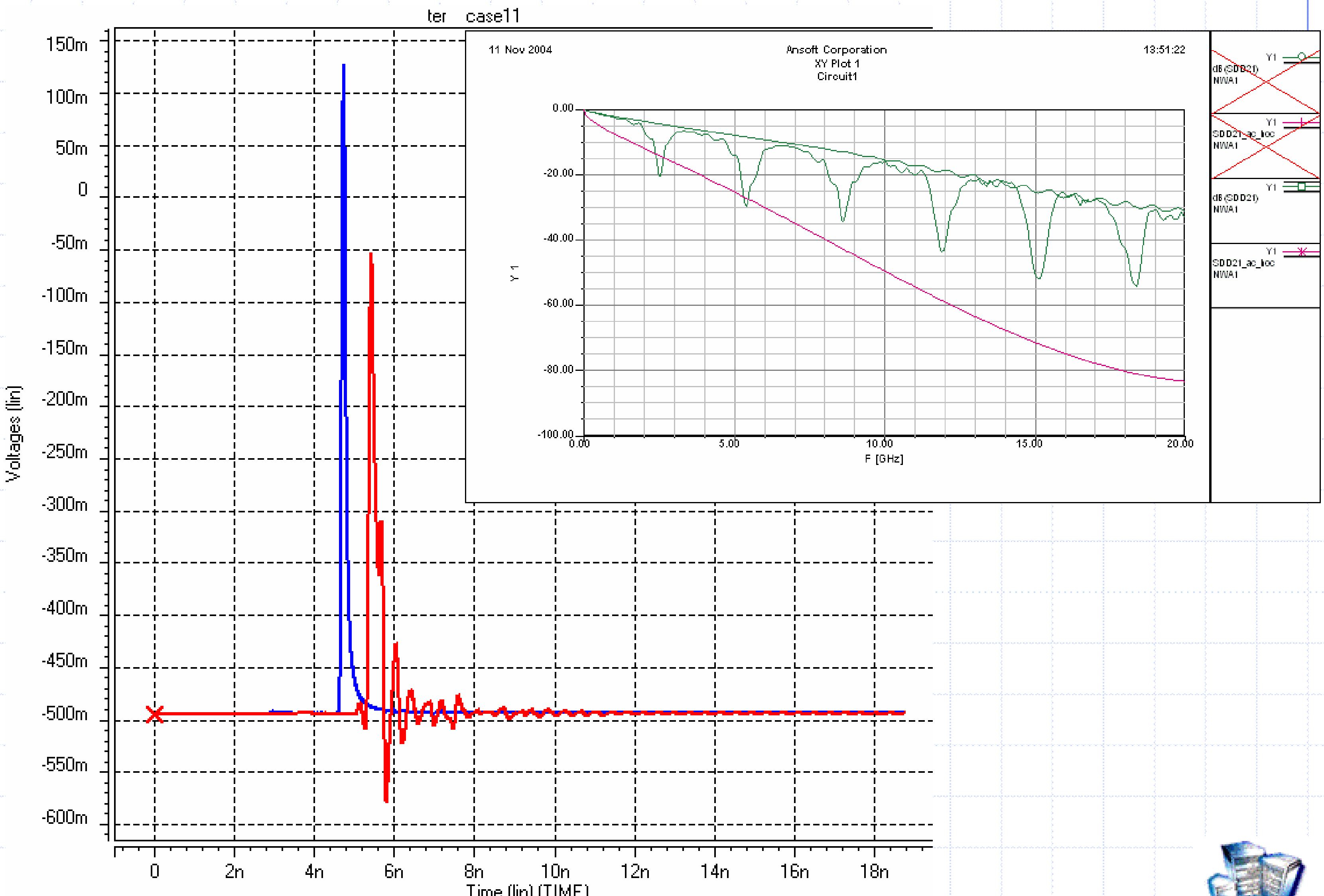
27 in line with via notch at 3.75 GHz



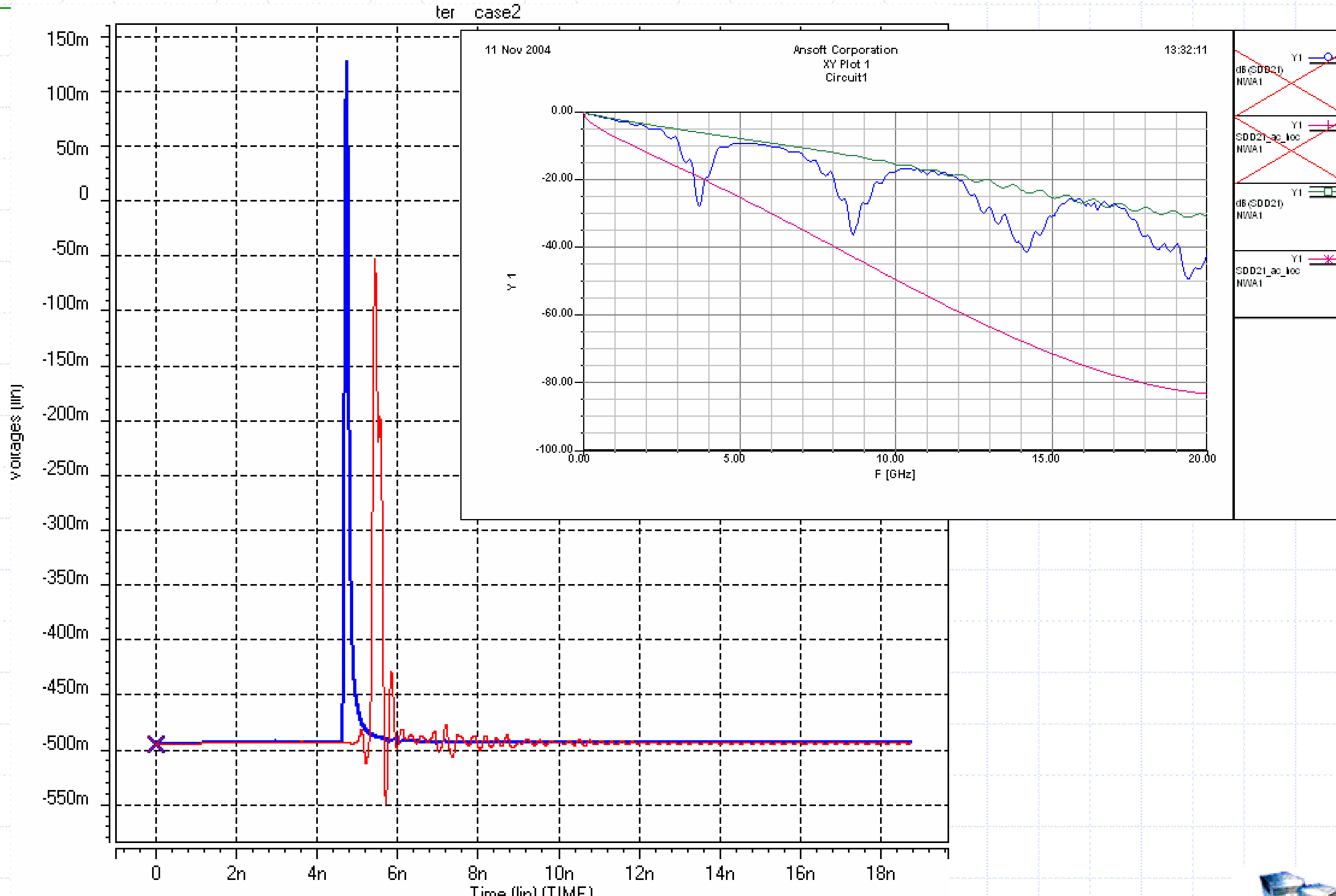
27 in line with via notch at 5 GHz



13 in line with via notch at 2.5 GHz



13 in line with via notch at 3.75 GHz



13 in line with via notch at 5 GHz