

Analysis of FEC proposal for Backplane Ethernet Magesh Valliappan

Theoretical Performance Estimate

• Assumptions:

- Assume memory-less Binary Symmetric Channel (BSC), but with finite error propagation (to model DFE effects)
- Probability of first error in a burst based on Gaussian noise model
- DFE does not propagate errors beyond decoder's capability
- Uncorrected errors are detected and entire code block is rejected
- Method:
 - Estimate Ethernet Frame Error Rate for each SNR using probabilities
 - Translate Frame Error Rate to "Effective BER" of ideal memory-less BSC with Gaussian noise

• Results

- Coding Gain Estimate (from Analysis):
 - 64 byte packets: 2.1 dB
 - 1518 byte packets: 2.3 dB



Analysis Results



everything*

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Time Domain Simulation Setup



Time Domain Simulation Setup

- Tyco Backplane model from 802.3ap website
- TX
 - 0.01 UI RJ
 - 3-tap FIR
 - Simple RC model for transmitter
- Package model included
- Crosstalk 2 aggressors, with similar TX configuration
- RX
 - Adaptive CDR circuit
 - 5-tap DFE
 - Ideal slicer
- AWGN noise source controlled to change BER
- Simulated over 1800 million bits
- Pseudo random bits, PCS not modeled



Simulation Results



everything*

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Simulation Results

- Consistent with 2 2.5 dB coding gain at 1e-12
 - 1.20dB at 1e-6
 - 1.35dB at 1e-7
 - 1.55dB at 1e-8
 - Projected to 1e-12, that gives 2.35dB (0.2dB per decade in BER)
- At 13.25dB, the error propagation statistics are

Burst length	Percent	Burst length	Percent
1	74.6	7	0
2	16.4	8	0
3	7.6	9	0
4	1.3	10	0
5	0.1	11	0
6	0	>11	0.1

everything

3 ROA

Conclusions

- Independently analyzed and simulated QC(2112,2080) code
 - Code provides 2+ dB of additional margin
- Implementation cost is small for 2dB margin
- Margin can be used to accommodate additional noise, jitter, crosstalk or reflections
- Backplane Ethernet should include FEC at least as an option

