Editor's Notes: *To be removed prior to final publication.*

1. The Table of Contents, Table of Figures and Table of Tables are added for reading convenience

2. This document is a straw man proposal

3.

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Addition to IEEE Std. 802.3-2002, Clause 69

Editor's Notes: *To be removed prior to final publication.*

-This draft WP0.5 is a first attempt by the editor to create a structure to this document.

-This text is a is a straw man proposal.

- All 802.3ap-200x are to be replaced with proper year upon final draft approval.

- All imported graphics are to be supplied per RevCom IEEE editorial requirements.

- It is recommended that all instances of "Ohm" and "Ohms" be replaced with the Omega symbol prior to final publication.

- Search and replace all references, other than to Clause 69, with appropriate cross references.

*-**References:***

None

Definitions:

None

Abbreviations:

None

Revision History:

WP0.5	*Initial Draft Working Paper Submitted to Working Group for Review*

69 Physical Medium Dependent (PMD) sublayer and baseband medium, type Ethernet Backplane (1000BASE-KX, 10GBASE-KX4 and 10GBASE-K?)

This clause specifies the requirements for the base PMD backplane considered the "Medium" and the sub-PMDs that are supported by the base PMD. In order to form a complete PHY (physical layer device), a PMD is combined with the appropriate sublayers (see Table 69–1), and with the management functions which are optionally accessible through the management interface defined in Clause 45, or equivalent.

Table 69–1—PHY (physical layer) clauses associated with the 10GBASAE-Kx PMD

Associated Clause	1000BASE-KX	10GBASE-KX4	10GBASE-K?
35—GMII[a]	Optional	NA	NA
36—1000BASE-X PCS/PMA	Required	NA	NA
46— XGMII[a]	NA	Optional	Optional
47—XGXS and XAUI	NA	Optional	Optional
??—10GBASE-X PCS/PMA	NA	Required	??

[a]The (X)GMII is an optional interface. However, if the (X)GMII is not implemented, a conforming implementation must behave functionally as though the RS and (X)GMII were present.

69.1 Ethernet Backplane Overview

The Backplane is designed to support 3 types of PMDs all using the common backplane ??? as the Media:

1) (10GBASE-K?) 4 individual 10 Gigabit serial links, each link is full duplex and has separate transmit and receive pairs, with each pair capable of handling 10 Gbaud signaling rates with an aggregated bandwidth of 40G in each direction

2) (1000BASE-KX4) 1 Channel comprised of 4 individual lanes each running at 3.125 Gigabit (XAUI), each Channel is full duplex and has 4 separate transmit and receive pairs, with each pair capable of handling 3.125 Gbaud signaling rates with an aggregated bandwidth of 10G in each direction

3) (1000BASE-KX) 4 individual 1 Gigabit Ethernet serial links, each link is full duplex and has separate transmit and receive pairs, with each pair capable of handling 1 Gbaud signaling rates with an aggregated bandwidth of 4G in each direction

Each Port can transport either 10 Gb/s or 1 Gb/s or 2.5 Gb/s (1/4 XAUI) data.

10GBASE-K? Describes the Physical Medium Dependent (PMD) for transmission of 10 Gb/s encoded data over the backplane.

1000BASE-KX4 Describes the Physical Medium Dependent (PMD) for transmission of the 10 Gb/s XAUI signaling over the backplane.

1000BASE-KX Describes the Physical Medium Dependent (PMD) for transmission of 1 Gb/s encoded data over the backplane.

Figure 69–1 shows the relationship of the backplane PMD sublayers and MDI to the ISO/IEC Open System Interconnection (OSI) reference model.

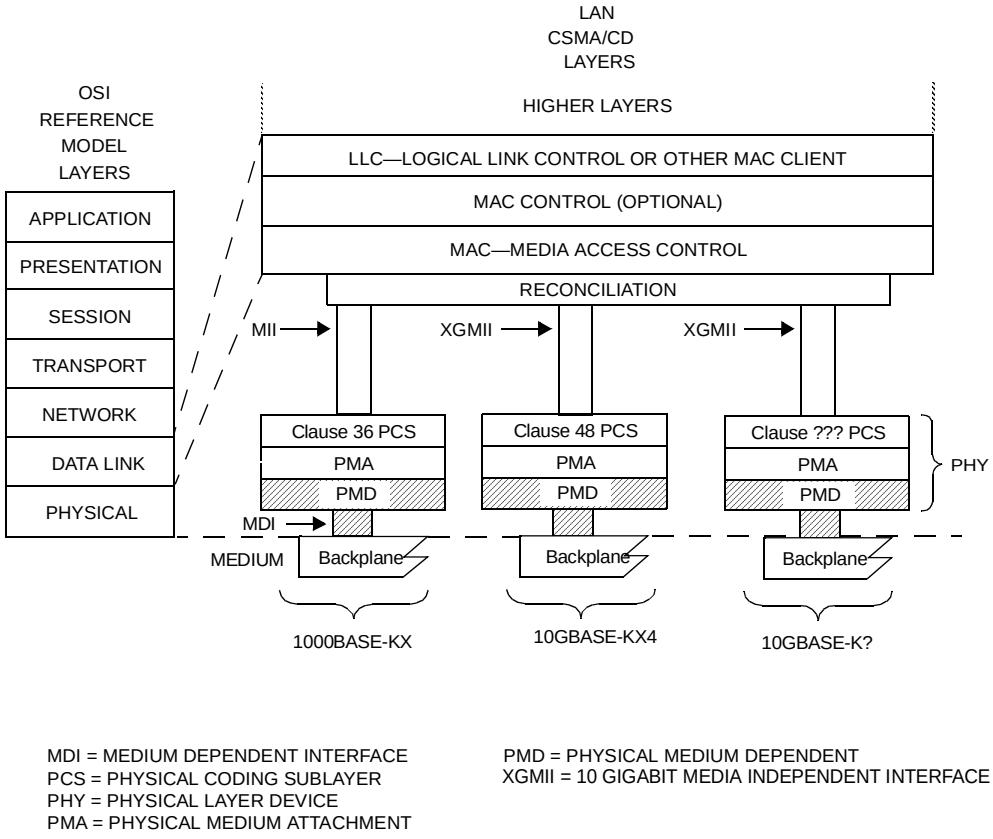

Figure 69–1—Backplane PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

69.1.1 Physical Medium Dependent (PMD) service interface

The backplane PMDs utilize the PMD service interface defined in 53.1.1. The PMD service interface is summarized below:

PMD_UNITDATA.request
PMD_UNITDATA.indicate
PMD_SIGNAL.indicate

69.1.2 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must consider the delay maxima, and that network planners and administrators consider the delay constraints regarding the backplane topology and concatenation of devices. A description of overall system delay constraints and the definitions for bit-times and pause_quanta can be found in 44.3

The sum of the transmit and the receive delays contributed by the backplane PMDs shall be no more than 512 BT or 1 pause_quantum.

69.1.3 PMD MDIO function mapping

The backplane PMDs use the MDIO function mapping as defined in Table 69–2.

Table 69–2—MDIO function mapping

PMD	Clause
1000Base-KX	
10GBASE-KX4	53.3
10GBASE-K?	

69.1.4 PMD functional specifications

The Backplane PMDs perform the transmit and receive functions which convey data between the PMD service interface and the MDI, and provides various management functions if the optional MDIO is implemented.

69.1.4.1 Link block diagram

A backplane link is shown in Figure 69–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The electrical transmit signal is defined at the output pins/balls/traces closest to the chip (TP1). Unless specified otherwise, all transmitter measurements and tests defined at TP1. Unless specified otherwise, all receiver measurements and tests are made at the input pins/balls/traces closest to the chip (TP4).

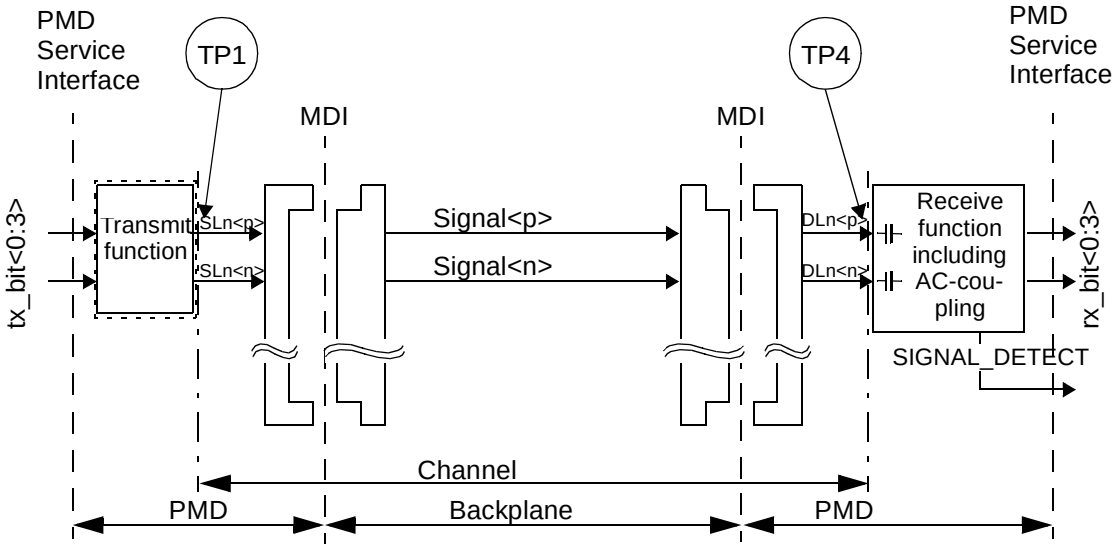

Figure 69–2—Backplane link (half link is shown)

NOTE– SLn<p> and SLn<n> are the positive and negative sides of the transmit differential signal pair and DLn<p> and DLn<n> are the positive and negative sides of the receive differential signal pair for lane n (*n* = 0, 1, 2, 3)

69.1.4.2 PMD transmit function

The PMD Transmit function shall convert the four logical bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signal streams. The four electrical signal streams shall then be delivered to the MDI. A positive output voltage of SLn<p> minus SLn<n> (differential voltage) shall correspond to tx_bit = ONE.

The PMD shall convey the bits received from the PMD service interface using the message PMD_UNITDATA.request(tx_bit<0:3>) to the MDI lanes, where (SL0<p>/<n>, SL1<p>/<n>, SL2<p>/<n>, SL3<p>/<n>) = tx_bit<0:3>.

69.1.4.3 PMD receive function

The PMD Receive function shall convert the electrical signal streams from the MDI into logical bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indicate (rx_bit<0:3>), all according to the receive electrical specifications. A positive input voltage level in each signal stream of DLn<p> minus DLn<n> (differential voltage) shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the MDI lanes to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit<0:3>), where rx_bit<0:3> = (DL0<p>/<n>, DL1<p>/<n>, DL2<p>/<n>, DL3<p>/<n>)

69.1.4.4 Global PMD signal detect function

The Global_PMD_signal_detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indicate message is generated when a change in the value of SIGNAL_DETECT occurs.

SIGNAL_DETECT is a global indicator of the presence of electrical signals on all four lanes. The PMD receiver is not required to verify whether a compliant signal is being received, however, it shall assert SIGNAL_DETECT = OK within 100 µs after the absolute differential peak-to-peak input voltage on each of the four lanes at the MDI has exceeded 175 mV for at least 1 UI (unit interval).

The PMD shall not have asserted SIGNAL_DETECT = FAIL until the absolute differential peak-to-peak input voltage on any of the four lanes at the MDI has dropped below 50 mV and has remained below 50 mV for at least 250 µs. The PMD shall have asserted SIGNAL_DETECT = FAIL when the absolute differential peak-to-peak input voltage on any of the four lanes at the MDI has dropped below 75 mV and has remained below 50 mV for longer than 500 µs.

Table 69–3—SIGNAL_DETECT

Parameter	Value	Units
SIGNAL_DETECT = OK level (maximum differential peak-to-peak amplitude)	175	mV
SIGNAL_DETECT = OK width (minimum)	1	UI
SIGNAL_DETECT = OK assertion time (maximum)	100	µs
SIGNAL_DETECT = FAIL level (minimum differential peak-to-peak amplitude)	75	mV
SIGNAL_DETECT = FAIL de-assertion time maximum minimum	 500 250	 µs µs

NOTE– SIGNAL_DETECT may not activate with a continuous 1010… pattern, such as the high frequency pattern of 48A.1, but it will be activated by an IPG.

69.1.4.5 PMD lane by lane signal detect function

When the MDIO is implemented, each PMD_signal_detect_n value, where n represents the lane number in the range 0:3, shall be continuously updated in response to the amplitude of the receive signal on its associated lane, according to the requirements of section 69.1.4.4.

69.1.4.6 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional. When implemented, it allows all of the transmitters to be disabled with a single variable.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant level (i.e. no transitions) and does not exceed the maximum differential peak-to-peak output voltage.
b) If a PMD_fault (69.1.4.9) is detected, then the PMD may turn off the electrical transmitter in all lanes.
c) Loopback, as defined in 69.1.4.8, shall not be affected by Global_PMD_transmit_disable.

69.1.4.7 PMD transmit disable function

The PMD_transmit_disable_n function is optional. It allows the electrical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that the corresponding transmitter drives a constant level (i.e. no transitions) and does not exceed the maximum differential peak-to-peak output voltage.
b) If a PMD_fault is detected, then the PMD may turn off the electrical transmitter and in the case of 10GBASE-4L all lanes may be turned off.
c) Loopback shall not be affected by PMD_transmit_disable_n.

NOTE– Turning off a transmitter can be disruptive to a network.

69.1.4.8 Loopback mode

Loopback mode shall be provided for the backplane PMDs by the transmitter and receiver of a device as a test function to the device. When loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. The transmitters shall not be disabled when loopback mode is enabled. A device must be explicitly placed in loopback mode because loopback mode is not the normal mode of operation of a device. Loopback applies to each individual Lane in the case of 1000BASE-KX or 10GBASE-K? and all lanes as a group for 10GBASE-KX4 (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing loopback mode is not defined by this standard.

Control of the loopback function is specified in 45.2.1.1.4.

NOTE– The signal path that is exercised in the loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

NOTE– Placing a network port into loopback mode can be disruptive to a network.

Editor's Notes: *To be removed prior to final publication.*

1. Is there a need to define an on chip test pattern?

69.1.4.9 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE, otherwise the PMD shall set PMD_fault to ZERO.

69.1.4.10 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE, otherwise the PMD shall set PMD_transmit_fault to ZERO.

69.1.4.11 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE, otherwise the PMD shall set PMD_receive_fault to ZERO.

69.1.5 MDI Electrical specifications

69.1.5.1 Signal levels

The MDI is a low-swing AC-coupled differential interface. Transmitter to receiver path AC-coupling, as defined in the corresponding subclauses, allows for interoperability between components operating from different supply voltages. Low-swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

69.1.5.2 Signal paths

The MDI signal paths are point-to-point connections. Each path corresponds to a backplane MDI lane and comprises two complementary signals making a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to 100 cm in length from TP1 to TP4. This includes the backplane, two connectors and two line cards as described in 69.1.6.

69.1.6 Channel characteristics

Editor's Notes: *To be removed prior to final publication.*

1. This Clause 69.1.6 is based on 10GBASE-CX4

2. This Clause is a straw man proposal

The Channel contains 50 Ohm differential traces terminated in a connector at each end for use as a link segment between MDIs. This Channel is primarily intended as a point-to-point interface of up to 100 cm between network ports using controlled impedance traces. All Channel measurements are to be made between TP2 and TP3 as shown in Figure 69–3.

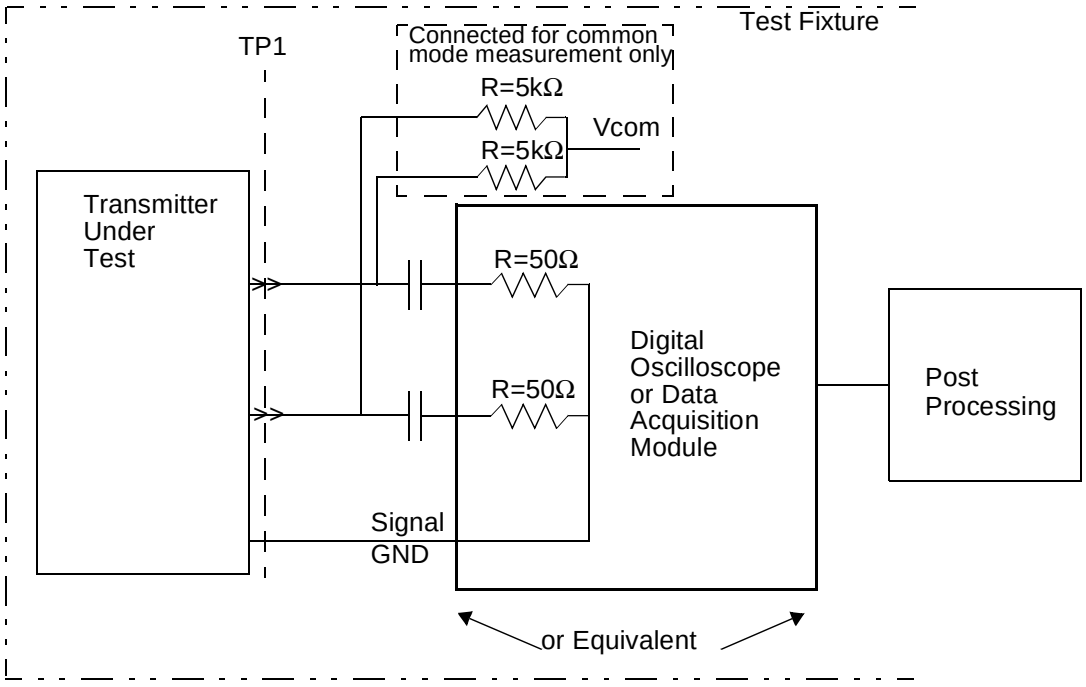

Figure 69–3—Channel transmit test fixture

These Channel specifications are based upon Channel trace characteristics as specified in 69–4.

Table 69–4—Channel differential characteristics

Description	Reference	Value	Unit
Maximum Insertion loss at ?? MHz	69.1.6.2 & 69.1.6.3	16	dB
Minimum Return loss at ?? MHz	69.1.6.3	12.0	dB
Minimum NEXT loss at ?? MHz	69.1.6.4.1	31.8	dB
Minimum MDNEXT loss at ?? MHz	69.1.6.4.2	29.8	dB
Minimum ELFEXT loss at ?? MHz	69.1.6.5.1	23.3	dB
Minimum MDELFEXT loss at ?? MHz	69.1.6.5.2	21.1	dB

69.1.6.1 Characteristic impedance and reference impedance

The nominal differential characteristic impedance of the Channel is 100 Ohms. The differential reference impedance for Channel specifications shall be 100 Ohms.

69.1.6.2 Channel insertion loss

The insertion loss, in dB with *f* in MHz, of each pair of the 10GEBP-xx Channel shall be:

$$\text{InsertionLoss}(f) \le (0.2629 \times \sqrt{f}) + (0.0034 \times f) + \left(\frac{12.76}{\sqrt{f}}\right) \qquad (69\text{–}1)$$

for all frequencies from 100 MHz to 2000 MHz. This includes the attenuation of the differential cabling pairs, and the assembly connectors.

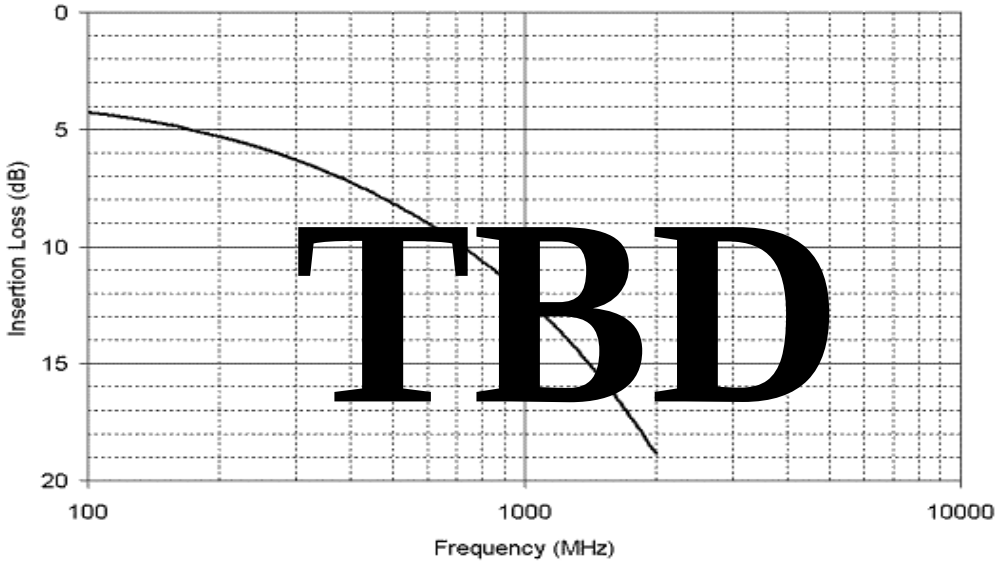

Figure 69–4—Channel insertion loss (informative)

69.1.6.3 Channel return loss

The return loss, in dB with *f* in MHz, of each pair of the 10GEBP-xx Channel shall be:

$$\text{ReturnLoss}(f) \geq 22.35 - 17.19 \times \log\left(\frac{f}{100}\right) \quad (69\text{–}2)$$

for 100 MHz <= *f* < 400 MHz.

$$\text{ReturnLoss}(f) \geq 12 \quad (69\text{–}3)$$

for 400 MHz <= *f* <= 2000 MHz.

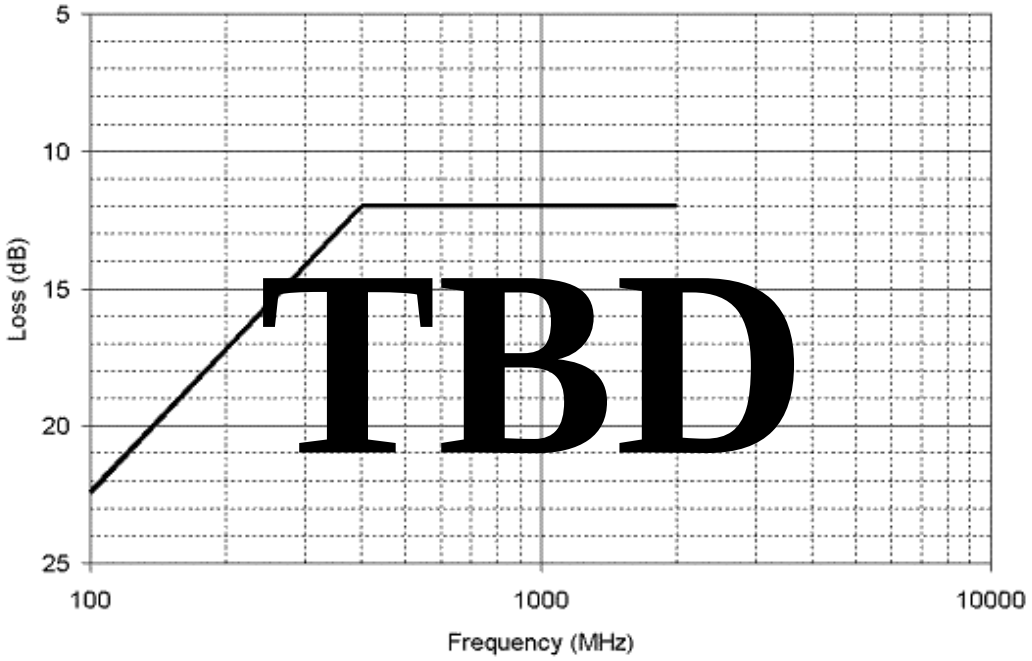

Figure 69–5—Channel return loss (informative)

69.1.6.4 Near-End Crosstalk (NEXT)

69.1.6.4.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between any of the four transmit lanes and any of the four receive lanes is specified to meet the BER objective of 10^{-12}. The NEXT loss between any transmit and receive lane of a link segment, in dB with *f* in MHz, shall be at least:

$$\mathrm{NEXT}(f) \geq 30 - 17 \times \log\left(\frac{f}{2000}\right) \quad (69\text{–}4)$$

for all frequencies from 100 MHz to 2000 MHz.

69.1.6.4.2 Multiple Disturber Near-End Crosstalk (MDNEXT)

Since four transmit and four receive lanes are used to transfer data between PMDs, the NEXT that is coupled into a receive lane will be from the four transmit lanes. To ensure the total NEXT coupled into a receive lane is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses.

The Power Sum loss between a receive lane and the four transmit lanes, in dB with *f* in MHz, shall be at least:

$$\mathrm{MDNEXT}(f) \geq 28 - 17 \times \log\left(\frac{f}{2000}\right) \quad (69\text{–}5)$$

for all frequencies from 100 MHz to 2000 MHz.

MDNEXT loss is determined by summing the power of the four individual pair-to-pair differential NEXT loss values over the frequency range 100 MHz to 2000 MHz as follows:

$$\mathrm{MDNEXT}_{\mathrm{loss}}(f) = -10 \times \log\left(\sum_{i=0}^{i=3} 10^{-NL(f)_i/10}\right) \quad (69\text{–}6)$$

where

$\mathrm{MDNEXT}_{\mathrm{loss}}(f)$	is the MDNEXT loss at frequency *f*
$\mathrm{NL}(f)_{\mathrm{i}}$	is the power of the NEXT loss at frequency *f* of pair combination i, in dB
f	is frequency ranging from 100 MHz to 2000 MHz
i	is the 0, 1, 2, or 3 (pair-to-pair combination)

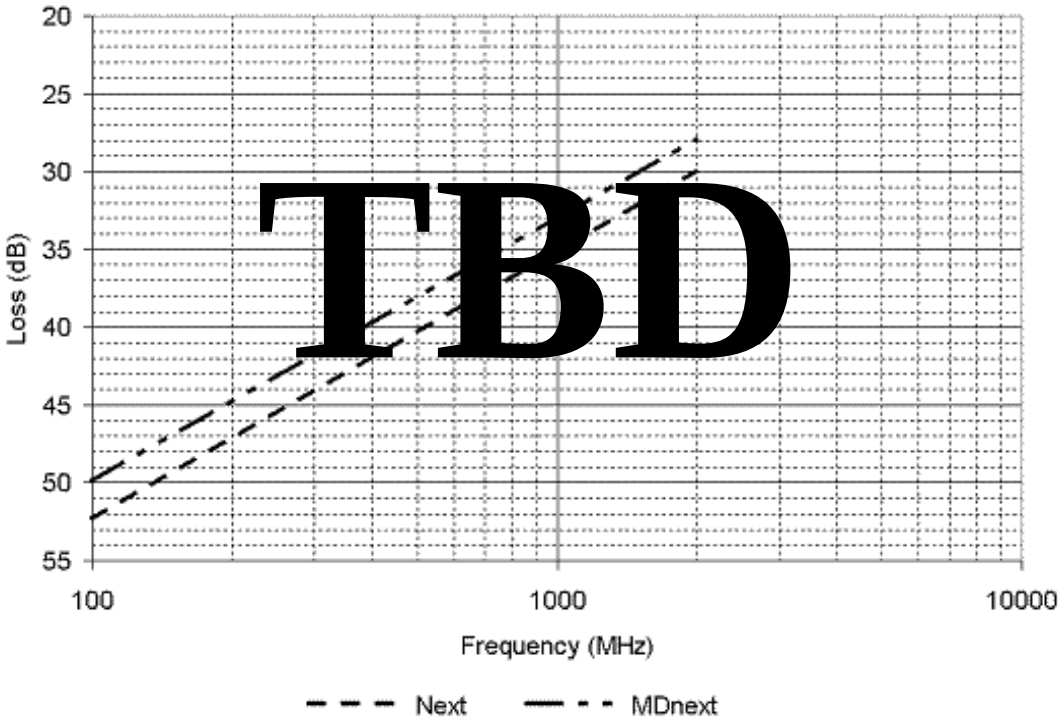

Figure 69–1—Channel NEXT / MDNEXT loss (informative)

69.1.6.5 Far-End Crosstalk (FEXT)

69.1.6.5.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment and meet the BER objective specified in 69.1.6.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a lane (disturbed lane), which is coupled from another lane (disturbing lane) with the noise source (transmitters) at the near end. FEXT loss is defined as

FEXT_Loss(*f*) = 20 x log(Vpds(*f*)/Vpcn(*f*))

and ELFEXT Loss is defined as

ELFEXT_Loss(*f*) = 20 x log(Vpds(*f*)/Vpcn(*f*)) – SLS_Loss(*f*)

where

FEXT_Loss(*f*)	is the FEXT loss at frequency *f*
ELFEXT_Loss(*f*)	is the ELFEXT loss at frequency *f*
Vpds	is the peak voltage of the disturbing signal (near-end transmitter)
Vpcn	is the peak crosstalk noise at the far end of the disturbed lane
SLS_Loss(*f*)	is the insertion loss of the disturbed lane in dB
f	is frequency ranging from 100 MHz to 2000 MHz

The worst pair ELFEXT loss between any two lanes shall be at least:

$$\mathrm{ELFEXT}(f) \geq 21 - 20 \times \log\left(\frac{f}{2000}\right) \quad (69\text{–}7)$$

for all frequencies from 100 MHz to 2000 MHz.

69.1.6.5.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four lanes are used to transfer data between PMDs, the FEXT that is coupled into a data carrying lane will be from the three other lanes in the same direction. To ensure the total FEXT coupled into a lane is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss (labeled as MDELFEXT) between a lane and the three adjacent disturbers shall be at least:

$$\mathrm{MDELFEXT}(f) \geq 19 - 20 \times \log\left(\frac{f}{2000}\right) \quad (69\text{–}8)$$

for all frequencies from 100 MHz to 2000 MHz.

MDELFEXT loss is determined by summing the power of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 100 MHz to 2000 MHz as follows:

$$\mathrm{MDELFEXT}_{\mathrm{loss}}(f) = -10 \times \log\left(\sum_{i=0}^{i=3} 10^{-NL(f)_i/10}\right) \quad (69\text{–}9)$$

where

$\mathrm{MDELFEXT}_{\mathrm{loss}}(f)$ is the MDELFEXT loss at frequency f

$\mathrm{NL}(f)_i$ is the power of ELFEXT loss at frequency f of pair combination i, in dB

f is frequency ranging from 100 MHz to 2000 MHz

i is the 1, 2, or 3 (pair-to-pair combination)

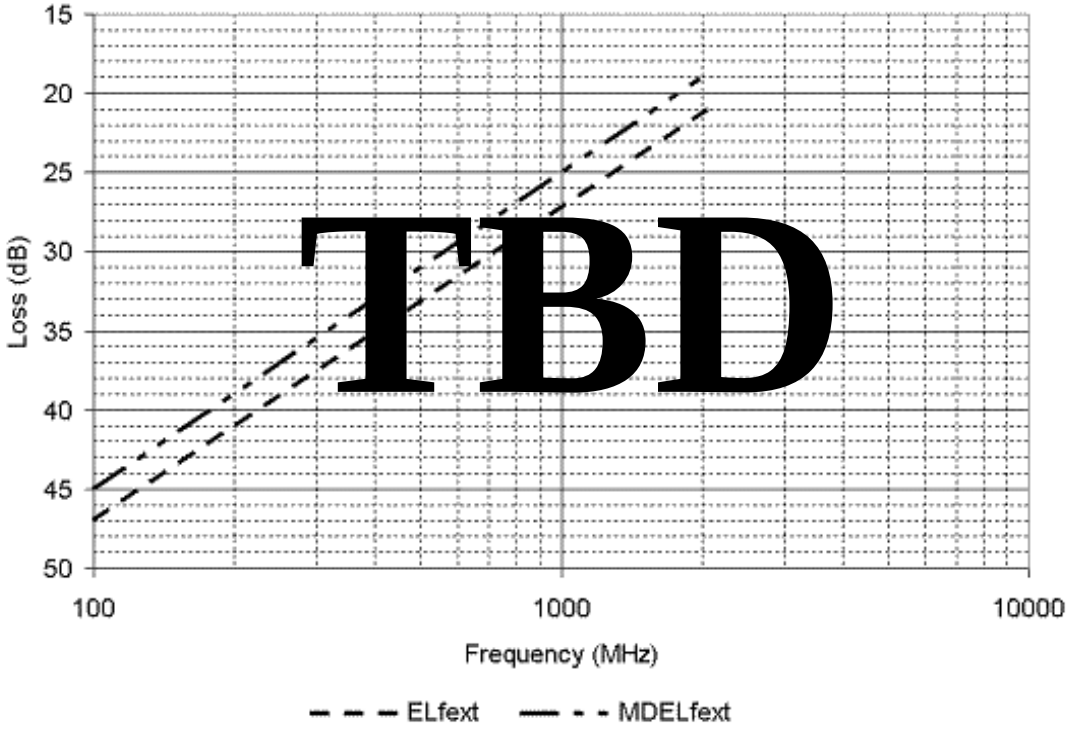

Figure 69–1—Channel ELFEXT / MDELFEXT loss (informative)

69.1.6.6 Shielding

The Channel shall provide Class 2 or better shielding in accordance with IEC 61196-1.

69.1.6.7 Crossover function

The Channel shall be routed in a crossover fashion as shown in Figure 69–2, with each of the pairs being attached to the transmitter contacts at one end and the receiver contacts at the other end.

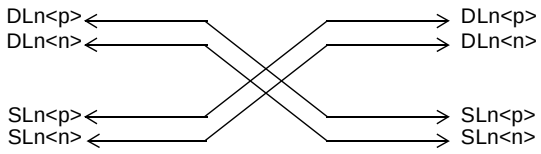

Figure 69–2—Trace Routing

NOTE– SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n=0,1,2,3)

69.1.7 MDI specification

The connector at each end of the Channel is not defined in this specification.

69.1.8 Environmental specifications

All equipment subject to this Clause shall conform to the applicable requirements of 14.7.

69.2 Electrical characteristics for 1000BASE-KX

Editor's Notes: *To be removed prior to final publication.*

1. This Clause 69.2 is based on 1000BASE-CX when converted from 75 Ohm to 50 Ohm.

2. This Clause is a straw man proposal

The backplane supports 4 Lanes in each direction. Each Lane is designed to transport 10 Gigabit Ethernet. Each Lane has separate transmit and receive pairs, with each pair capable of handling ??? Gbaud signaling rates. Each Lane can asynchronously transport either 10 Gb/s data, or 1 Gb/s data. However, in the case of 10GBASE-KX4 the 4 lanes, each transporting 3.125 Gb/s data, are bundled together to transport 10Gb/s.

This section describes the electrical characteristics of the 1Gb/s

69.2.1 Transmitter characteristics at TP1 for 1000BASE-KX

Transmitter characteristics shall meet the specifications in Table 69–1 at TP1 while transmitting the test pattern specified in 48A.2, unless otherwise noted.

Table 69–1—Transmitter characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Signaling speed, per lane		1.25 ± 100 ppm	GBd
Differential peak-to-peak output voltage[a]	69.2.1.3	800 to 1600	mVp-p
Common mode voltage limits	69.2.1.4	0.2 - 1.2?	V
Differential output return loss minimum	69.2.1.5	12	dB
Output jitter (peak-to-peak) Max. Random jitter component[b] Deterministic jitter[c] Total jitter	69.2.1.6	 0.27 0.17 0.35	 UI UI UI

[a]See Figure 69–5 for an illustration of the definition of differential peak-to-peak output voltage
[b]Maximum random jitter component
[c]Deterministic jitter is already incorporated into the differential output template.

69.2.1.1 Test fixtures for 1000BASE-KX

The test fixture of Figure 69–3, or its functional equivalent, is required for measuring the transmitter specifications described in 69.2.1.

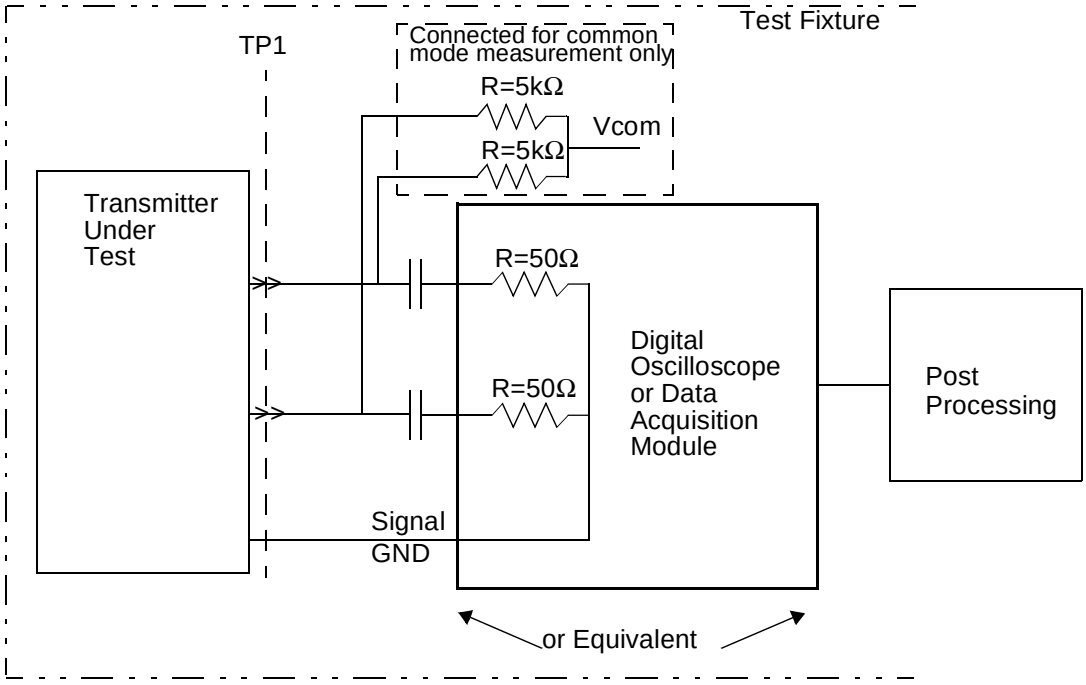

Figure 69–3—Transmit Test Fixture for 1000BASE-KX

69.2.1.2 Test fixture impedance for 1000BASE-KX

The nominal differential impedance of the transmit test fixture depicted in Figure 69–3 shall be 100 Ohms with a return loss Lower than -26 dB from 50 MHz to 625 MHz.

69.2.1.3 Differential output template for 1000BASE-KX

The transmitter differential output signal is defined at TP1, as shown in Figure 69–4. The transmitter shall provide equalization such that the output waveform falls within the template shown in Figure 69–4 for the test pattern specified in 48A.2, with all other transmitters active. Voltage and time coordinates for inflection points on Figure 69–4 are given in Table 69–2. The signals on each pair at TP1 shall meet the transmit tem-

plate specifications when connected to the transmitter test fixture shown in Figure 69–3, with all other transmitters active.

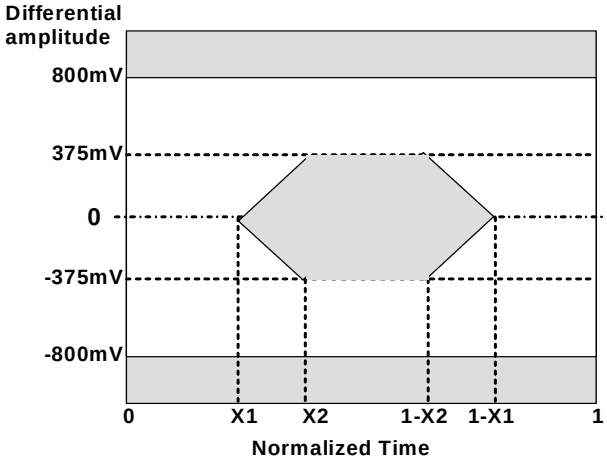

Figure 69–4—Absolute eye diagram mask at TP-1 for 1000BASE-KX

Table 69–2—Transmitted eye mask at TP-1 for 1000BASE-KX

Symbol	Value	Units
X1	0.125	Unit intervals (UI)
X2	0.325	Unit intervals (UI)

69.2.1.4 Output amplitude at TP1 for 1000BASE-KX

DC-referenced logic levels are not defined since the receiver is AC-coupled. The common mode voltage of SLn<p> and SLn<n> shall be between 0.2 V and 1.2 V with respect to backplane ground as measured at Vcom in Figure 69–3.

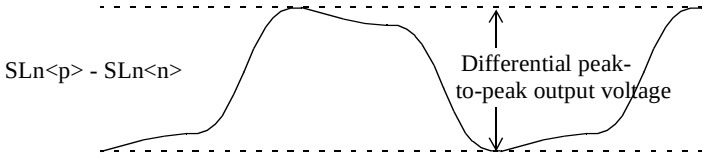

Figure 69–5—Transmitter differential peak-to-peak output voltage definition

NOTE– SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n=0,1,2,3).

69.2.1.5 Output return loss for 1000BASE-KX

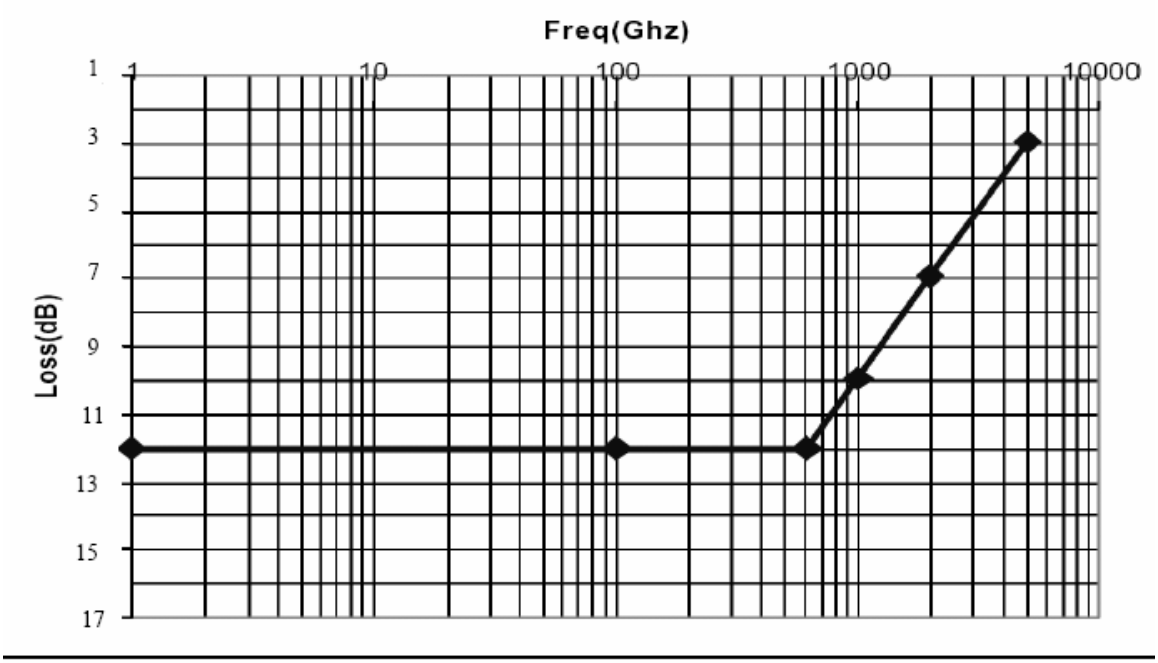

Figure 69–6—Output return loss for 1000BASE-KX

69.2.1.6 Transmit jitter for 1000BASE-KX)

The transmitter shall satisfy the jitter requirements of 69.2.1.7 with a maximum total jitter of 0.350 UI peak-to-peak, a maximum deterministic component of 0.170 UI peak-to-peak and a maximum random component of 0.270 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 69.2.1.7.

69.2.1.7 Transmit Jitter test requirements for 1000BASE-KX

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the CJPAT pattern defined in Annex 48A.5. All four lanes of the backplane transceiver are active in both directions, and opposite ends of the link use asynchronous clocks. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

69.2.2 Receiver characteristics at TP4 for 1000BASE-KX

The receiver shall have the characteristics as summarized in Table 69–3 and detailed in the following subclauses.

Table 69–3—Receiver characteristics for 1000BASE-KX

Parameter	Subclause reference	Value	Units
Bit error ratio	69.2.2.1	10^{-12}	
Signaling speed, per lane		1.25 ± 100 ppm	GBd
Receiver coupling	69.2.2.2	AC	
Differential input peak-to-peak amplitude max.	69.2.2.3	1600	mV
Return loss differential	69.2.2.4	12	dB

Editor's Notes: *To be removed prior to final publication.*
1. Do we need to define a common mode and crosstalk?

69.2.2.1 Bit error ratio for 1000BASE-KX

The receiver shall operate with a BER of better than 10^{-12} when receiving a compliant transmit signal, as defined in 69.2.1, through a compliant backplane as defined in 69.1.6.

NOTE– The BER should be met with a worst case insertion loss, long trace, as well as a low loss, short trace. The low loss trace may be a more stringent requirement on the system due to higher reflections and crosstalk than with long traces.

69.2.2.2 AC-coupling for 1000BASE-KX

The receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various PMD components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE– It is recommended that the maximum value of the coupling capacitors be limited to 470 pF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

69.2.2.3 Input signal amplitude for 1000BASE-KX

Receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 69.2.2.1. Note that this may be larger than the 1600 mV differential maximum of 69.2.1.4 due to the actual transmitter out-

put and receiver input impedances. The input impedance of a receiver can cause the minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ohms test load. Since the receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

69.2.2.4 Input return loss for 1000BASE-KX

For frequencies from 50 MHz to 625MHz, the differential return loss, in dB with *f* in MHz, of the receiver shall be greater than or equal to Equation 54–1 and Equation 54–2. This input impedance requirement applies to all valid input levels. The reference impedance for differential return loss measurements is 100 Ohms.

69.3 Electrical characteristics for 10GBASE-KX4

Editor's Notes: *To be removed prior to final publication.*

1. This Clause 69.3 is based on 10GBASE-CX4 with moved test point from TP2 to TP1

2. 3.This Clause is only a straw man

69.3.1 Transmitter characteristics (10GBASE-KX4)

Transmitter characteristics in Table 69–4 shall meet specifications at TP1, unless otherwise noted.

Table 69–4—Transmitter characteristics for 10GBASE-KX4

Parameter	Subclause reference	Value	Units
Signaling speed, per lane		3.125 ± 100 ppm	GBd
Unit interval nominal		320	ps
Differential peak-to-peak output voltage	69.3.1.3	800-1600	mV
Differential peak-to-peak output voltage difference (maximum)	69.3.1.3	150	mV
Common mode voltage limits	69.3.1.3	0.2? to 1.2?	V
Differential output return loss minimum	69.3.1.4	[See Equation (69–10) and Equation (69–11)]	dB
Differential output template	69.3.1.5	[See figure (69–9) and table (69–5)]	V
Transition time	69.3.1.6	60-130	ps
Output jitter (peak-to-peak) Random jitter Deterministic jitter[a] Total jitter	69.3.1.6	 0.27 0.17 0.35	 UI UI UI

[a]Deterministic jitter is already incorporated into the differential output template.

69.3.1.1 Test fixtures (10GBASE-KX4)

The test fixture of Figure 69–7, or its functional equivalent, is required for measuring the transmitter specifications described in 69.3.1.

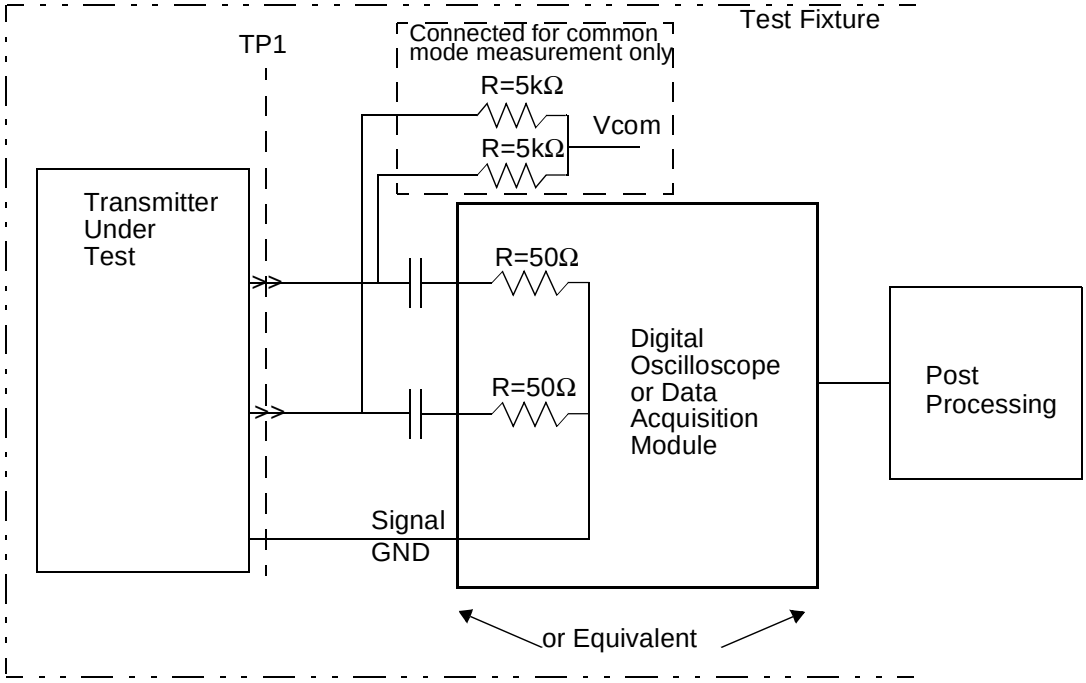

Figure 69–7—Transmit Test Fixture for 10GBASE-KX4

69.3.1.2 Test fixture impedance (10GBASE-KX4)

The nominal differential impedance of the transmit test fixture depicted in Figure 69–7 shall be 100 Ohms with a return loss greater than 20 dB from 100 MHz to 2000 MHz.

69.3.1.3 Output amplitude (10GBASE-KX4)

While transmitting the test pattern specified in 48A.2:

1) The transmitter maximum differential peak-to-peak output voltage shall be less than 1600 mV.
2) The minimum differential peak-to-peak output voltage shall be greater than 800 mV.
3) The maximum difference between any two lanes' differential peak-to-peak output voltage shall be less than or equal to 150 mV.

See Figure 69–8 for an illustration of the definition of differential peak-to-peak output voltage.

DC-referenced logic levels are not defined since the receiver is AC-coupled. The common mode voltage of SLn<p> and SLn<n> shall be between –0.4 V and 1.9 V with respect to Signal Shield as measured at Vcom in Figure 69–7.

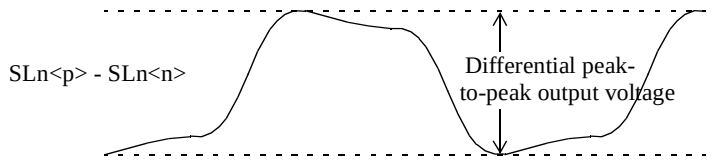

Figure 69–8—Transmitter differential peak-to-peak output voltage definition

NOTE– SLn<p> and SLn<n> are the positive and negative sides of the differential signal pair for Lane n (n=0,1,2,3).

69.3.1.4 Output return loss (10GBASE-KX4)

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with *f* in MHz, of the transmitter shall meet Equation 69–10 and Equation 69–11. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements shall be 100 Ohms.

$$\mathrm{ReturnLoss}(f) \geq 10 \tag{69–10}$$

for 100 MHz <= *f* < 625 MHz and

$$\mathrm{ReturnLoss}(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{69–11}$$

for 625 MHz <= *f* <= 2000 MHz.

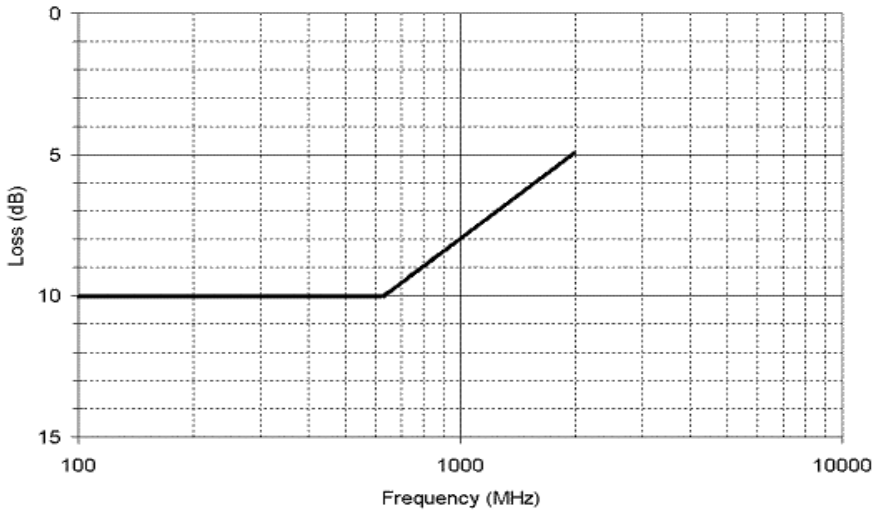

Figure 69–9—Transmit differential output return loss (informative)

69.3.1.5 Differential output template (10GBASE-KX4)

The transmitter differential output signal is defined at TP1, as shown in Figure 69–9. The transmitter shall provide equalization such that the output waveform falls within the template shown in Figure 69–10 for the test pattern specified in 48A.2, with all other transmitters active. Voltage and time coordinates for inflection points on Figure 69–10 are given in Table 69–5. The signals on each pair at TP1 shall meet the transmit template specifications when connected to the transmitter test fixture shown in Figure 69–7, with all other transmitters active. The waveform under test shall be normalized by using the following procedure:

1) Align the output waveform under test, to achieve the best fit along the horizontal time axis.
2) Calculate the +1 low frequency level as V_{lowp} = average of any 2 successive unit intervals (2UI) between 2.5 UI and 5.5 UI.
3) Calculate the 0 low frequency level as V_{lowm} = average of any 2 successive unit intervals (2UI) between 7.5 UI and 10.5 UI.
4) Calculate the vertical offset to be subtracted from the waveform as $V_{off} = (V_{lowp} + V_{lowm}) / 2$.
5) Calculate the vertical normalization factor for the waveform as $V_{norm} = (V_{lowp} - V_{lowm}) / 2$.
6) Calculate the normalized waveform as:
Normalized_Waveform=(Original_Waveform-V_{off})*(0.69/V_{norm}).
7) Align the Normalized_Waveform under test, to achieve the best fit along the horizontal time axis.

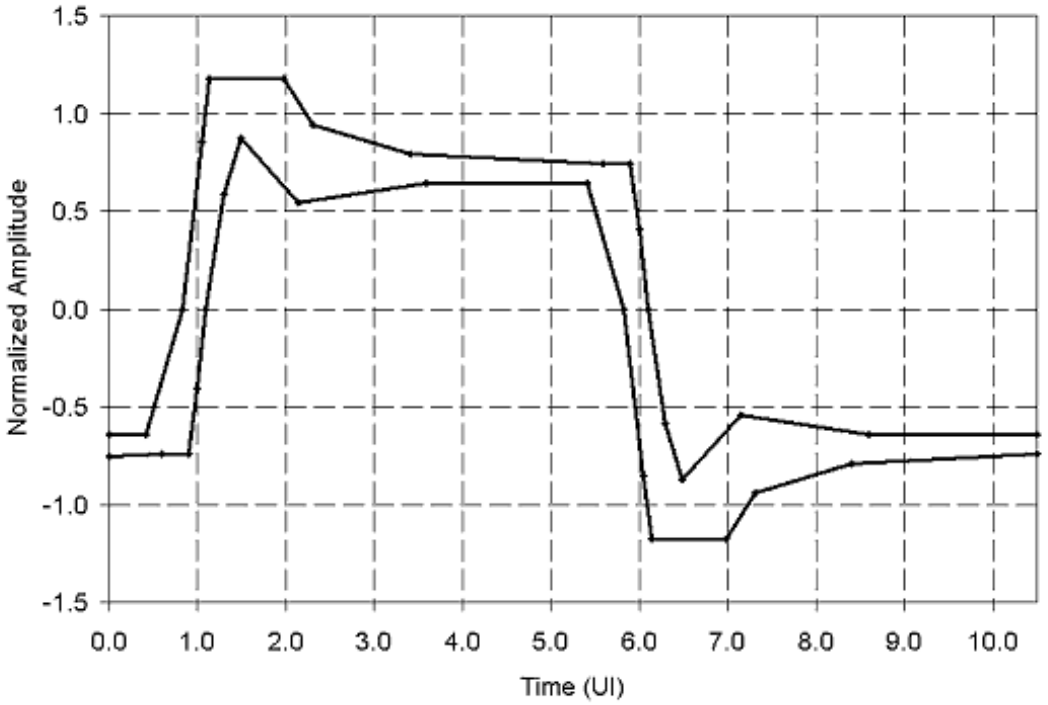

Figure 69–10—Normalized transmit template

Table 69–5—Normalized transmit time domain template

Upper Limit				Lower Limit			
Time (UI)	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**	**Time (UI)**	**Amplitude**
0.000	-0.640	5.897	0.740	0.000	-0.754	5.409	0.640
0.409	-0.640	5.997	0.406	0.591	-0.740	5.828	0.000
0.828	0.000	6.094	0.000	0.897	-0.740	6.050	-0.856
1.050	0.856	6.294	-0.586	0.997	-0.406	6.134	-1.175
1.134	1.175	6.491	-0.870	1.094	0.000	6.975	-1.175
1.975	1.175	7.141	-0.546	1.294	0.586	7.309	-0.940
2.309	0.940	8.591	-0.640	1.491	0.870	8.500	-0.790
3.409	0.790	10.500	-0.640	2.141	0.546	10.500	-0.742
5.591	0.740			3.591	0.640		

69.3.1.6 Transition time (10GBASE-KX4)

The rising edge transition time shall be between 60 ps and 130 ps as measured at the 20% and 80% levels of the peak-to-peak differential value of the waveform using the high frequency test pattern of 48A.1. The falling edge transition time shall be between 60 ps and 130 ps as measured at the 80% and 20% levels of the peak-to-peak differential value of the waveform using the high frequency test pattern of 48A.1.

69.3.1.7 Transmit jitter (10GBASE-KX4)

The transmitter shall satisfy the jitter requirements of 69.3.1.7 with a maximum total jitter of 0.350 UI peak-to-peak, a maximum deterministic component of 0.170 UI peak-to-peak and a maximum random component of 0.270 UI peak-to-peak. Jitter specifications include all but 10^{-12} of the jitter population. Transmit jitter test requirements are specified in 69.3.1.7.

69.3.1.8 Transmit Jitter test requirements (10GBASE-KX4)

Transmit jitter is defined with respect to a test procedure resulting in a BER bathtub curve such as that described in Annex 48B. For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements shall be the CJPAT pattern defined in Annex 48A.5. All four lanes of the 10GEBP-xx transceiver are active in both directions, and opposite ends of the link use asynchronous clocks. Crossing times are defined with respect to the mid-point (0 V) of the AC-coupled differential signal.

69.3.2 Receiver characteristics (10GBASE-KX4)

The 10GBASE-KX4 Receivers shall have the characteristics as summarized in Table 69–4 and detailed in the following subclauses.

Table 69–6—Receiver characteristics

Parameter	Subclause reference	Value	Units
Bit error ratio	69.3.2.1	10^{-12}	
Signaling speed, per lane	69.3.2.2	3.125 ± 100 ppm	GBd
Unit interval (UI) nominal	69.3.2.2	320	ps
Receiver coupling	69.3.2.3	AC	
Differential input peak-to-peak amplitude (maximum)	69.3.2.4	1600	mV
Return loss[a] differential (minimum)	69.3.2.5	[See Equation (69–10) and Equation (69–11)]	dB

[a]Relative to 100 Ohms differential.

69.3.2.1 Bit error ratio (10GBASE-KX4)

The receiver shall operate with a BER of better than 10^{-12} when receiving a compliant transmit signal, as defined in 69.3.2, through a compliant backplane as defined in 69.1.6.

NOTE– The BER should be met with a worst case insertion loss, long trace, as well as a low loss, short trace. The low loss trace may be a more stringent requirement on the system due to higher reflections and crosstalk than with long traces.

69.3.2.2 Signaling speed range (10GBASE-KX4)

A 10GBASE-KX4 receiver shall comply with the requirements of Table 69–6— for any signaling speed in the range 3.125 GBd +/- 100 ppm. The corresponding unit interval is nominally 320 ps.

69.3.2.3 AC-coupling (10GBASE-KX4)

The 10GBASE-KX4 receiver shall be AC-coupled to the backplane to allow for maximum interoperability between various 10 Gbps components. AC-coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC-coupling in actual implementations.

NOTE– It is recommended that the maximum value of the coupling capacitors be limited to 470 pF. This will limit the inrush currents to the receiver that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

69.3.2.4 Input signal amplitude (10GBASE-KX4)

10GBASE-KX4 receivers shall accept differential input signal peak-to-peak amplitudes produced by compliant transmitters connected without attenuation to the receiver, and still meet the BER requirement specified in 69.3.2.1. Note that this may be larger than the 1600 mV differential maximum of 69.3.1.3 due to the actual transmitter output and receiver input impedances. The input impedance of a receiver can cause the

minimum signal into a receiver to differ from that measured when the receiver is replaced with a 100 Ohms test load. Since the 10GEBP-xx receiver is AC-coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

69.3.2.5 Input return loss (10GBASE-KX4)

For frequencies from 100 MHz to 2000 MHz, the differential return loss, in dB with *f* in MHz, of the receiver shall be greater than or equal to Equation 69–10 and Equation 69–11. This input impedance requirement applies to all valid input levels. The reference impedance for differential return loss measurements is 100 Ohms.

69.4 Electrical characteristics for 10GBASE-K?

Editor's Notes: *To be removed prior to final publication.*

1. This Clause 69.4 is just a placeholder and contains dummy text

2. This Clause has not been reviewed by anyone

69.4.1 Transmitter characteristics (10GBASE-K?)

69.4.1.1 Test fixtures (10GBASE-K?)

69.4.1.2 Test fixture impedance (10GBASE-K?)

69.4.1.3 Output amplitude (10GBASE-K?)

69.4.1.4 Output return loss (10GBASE-K?)

69.4.1.5 Differential output template (10GBASE-K?)

69.4.1.6 Transition time (10GBASE-K?)

69.4.1.7 Transmit jitter (10GBASE-K?)

69.4.1.8 Transmit Jitter test requirements (10GBASE-K?)

69.4.2 Receiver characteristics (10GBASE-K?)

69.4.2.1 Bit error ratio (10GBASE-K?)

69.4.2.2 AC-coupling (10GBASE-K?)

69.4.2.3 Input signal amplitude (10GBASE-K?)

69.4.2.4 Input return loss (10GBASE-K?)

69.5 Auto Negotiation?

Editor's Notes: *To be removed prior to final publication.*

1. This Clause 69.5 is just a placeholder and contains dummy text

2. This Clause has not been reviewed by anyone