Forward Error Correction proposal for 10G Backplane Ethernet

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Objectives

- FEC to provide additional gain
  - BER objective of 10^{-12} or better on broader set of channels (green/gray)
  - Achieve 10^{-12} in a 10^{-7} channel with error propagation as discussed in szczepanek_05_0505.pdf
  - Meet Mean Time to False Packet Acceptance (MTTFPA) requirements for 10GbE
- Minimum changes to existing sublayers
  - Locate between PCS & PMA and be compatible with existing PCS (clause 49) & PMA (clause 51)
  - No increase in baud rate or decrease in payload rate
  - Low overhead (latency/area/power)
- Leverage previous work presented to the 802.3ap task force
  - FEC proposal made by Szczepanek in Mar '05 interim (Reference: szczepanek_01_0305.pdf)
  - Error Propagation results by Belogolovy & Szczepanek in May '05 interim (Reference: szczepanek_05_0505.pdf)
- Negotiate FEC capability through AN

Overview

- Main parameters of PHY proposal
- FEC code description
- Performance and comparison
- Framing
- FEC sublayer synchronization
- Auto-Negotiation
- Implementation
- Conclusions

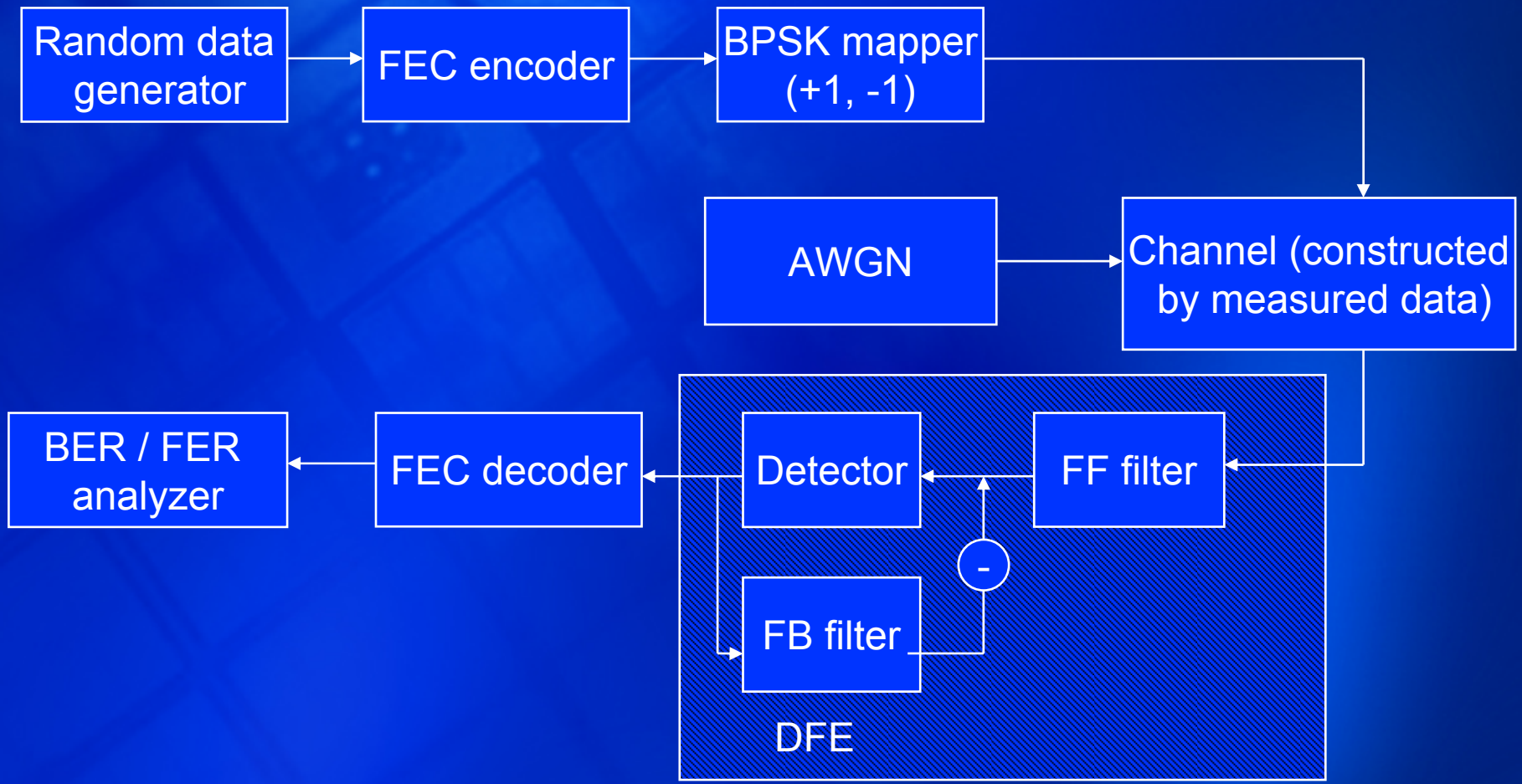
Parameters of PHY proposal

- Binary burst error correction code (2112, 2080)
- Modulation: BPSK{+1,-1} (NRZ)
- Equalization: from 802.3ap D2.0 spec
- Symbol rate: 10.3125G
- Compression and usage of 32 sync bits from 64B/66B blocks
- Compatibility with Clause 49 & Clause 51 (use of 16-bit data path as in XSBI)

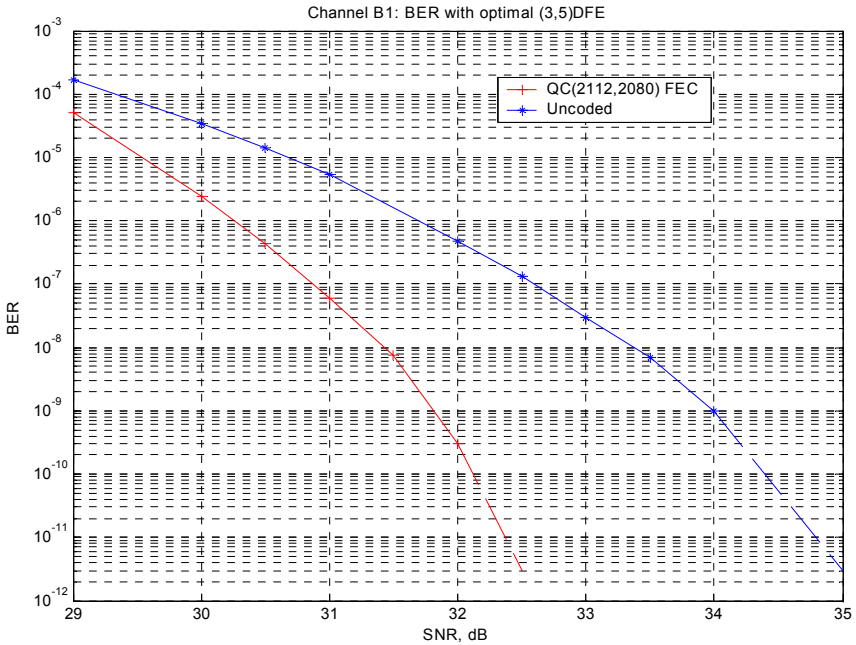
FEC description

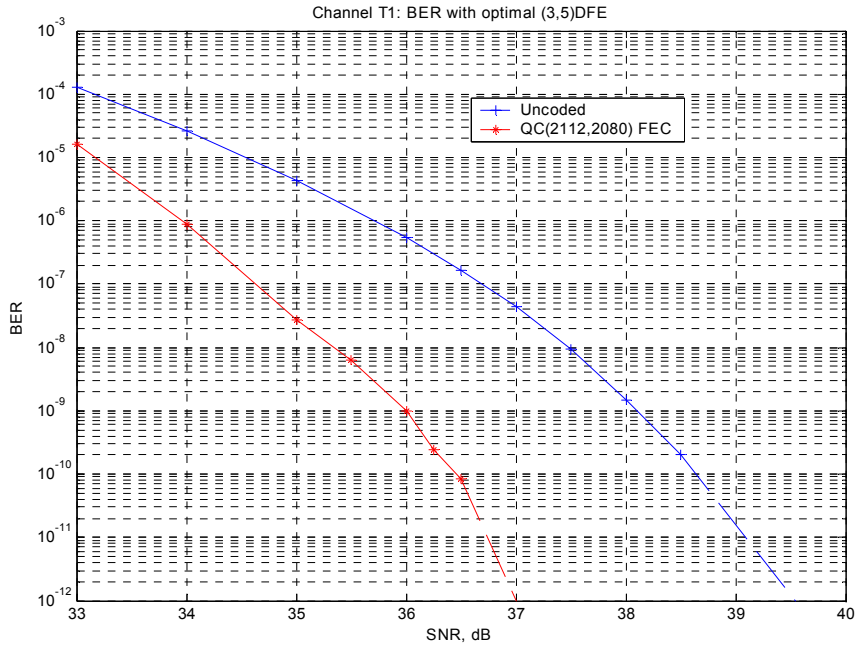
- QC(2112, 2080) burst error correction code is a shortened cyclic code with 32 redundant bits
- Generator polynomial
  - $g(x)=x^{32}+x^{23}+x^{21}+x^{11}+x^{2}+1$
- For (2112, 2080) code
  - encoder: systematic, represented by LFSR of length 32
  - decoder: Meggitt decoder for shortened cyclic codes
  - detector: syndrome calculation
  - Performance: able to correct error burst of length up to 16 (based on simulations)
- PN-2112 bit sequence
  - Generated by scrambler polynomial from Clause 49 $r(x)= x^{58}+x^{39}+1$ with initial state of $x^{57}=1$ and $x^{i-1}=x^{i}$(XOR)1 or binary 101010….
  - For every codeword PN-2112 sequence is returned to its initial state

Simulation pipeline



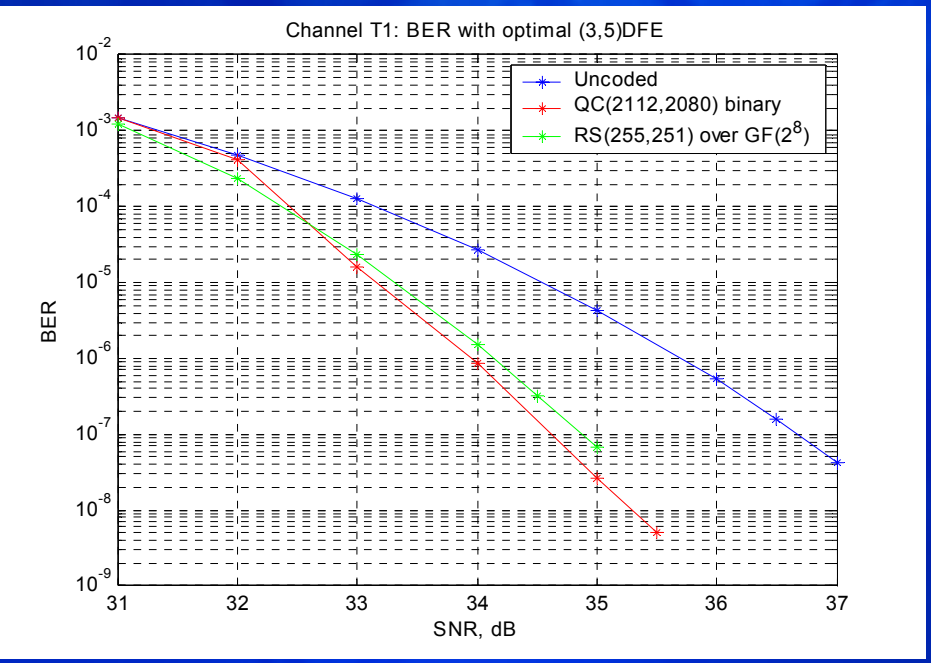
Gains of FEC





- Considering bit error rate, FEC with 32 redundant bits give:
  - 2dB coding gain at BER=10^{-8}, 2.5dB gain at BER=10^{-12}
  - BER goes from ~ 10^{-7} to 10^{-12} with same SNR

Codes comparison

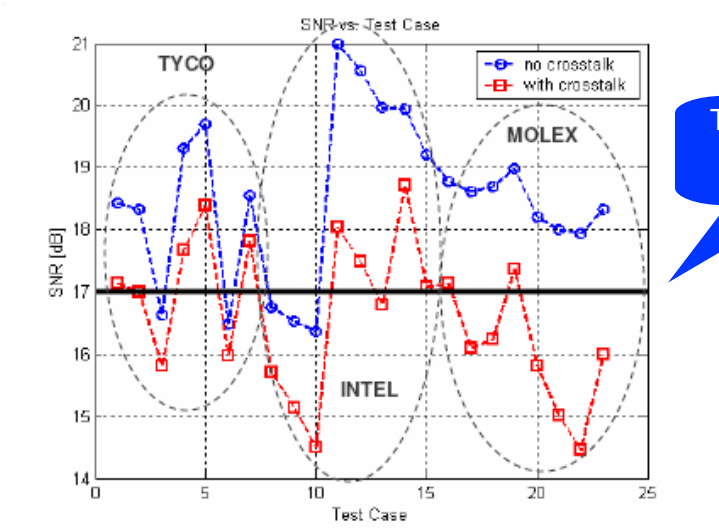


- Codes with 32 parity check bits were compared
  - QC(2112,2080), binary burst error correction code with Meggitt decoder
  - RS(255,251) over GF(2^8) with Berlekamp decoder
- Coding gain of binary code is better
  - For the same coding gain (or better) RS codes should have 40 redundant bits
    - RS over GF(2^{10}) with 2 parity check symbols
- Implementation of Meggitt decoder is significantly simpler than Berlekamp decoder

FEC Gain Vs SNR for test channels

- Gain of 2.5dB allows channels listed in the graph to meet the target SNR of 17dB
- SNR difference between worst and best case channels is ~5dB
- In relative terms 2.5dB gain provides ~50% improvement for worst case channels

SNR Results Summary



Target SNR 17dB for BER 10^{-12}

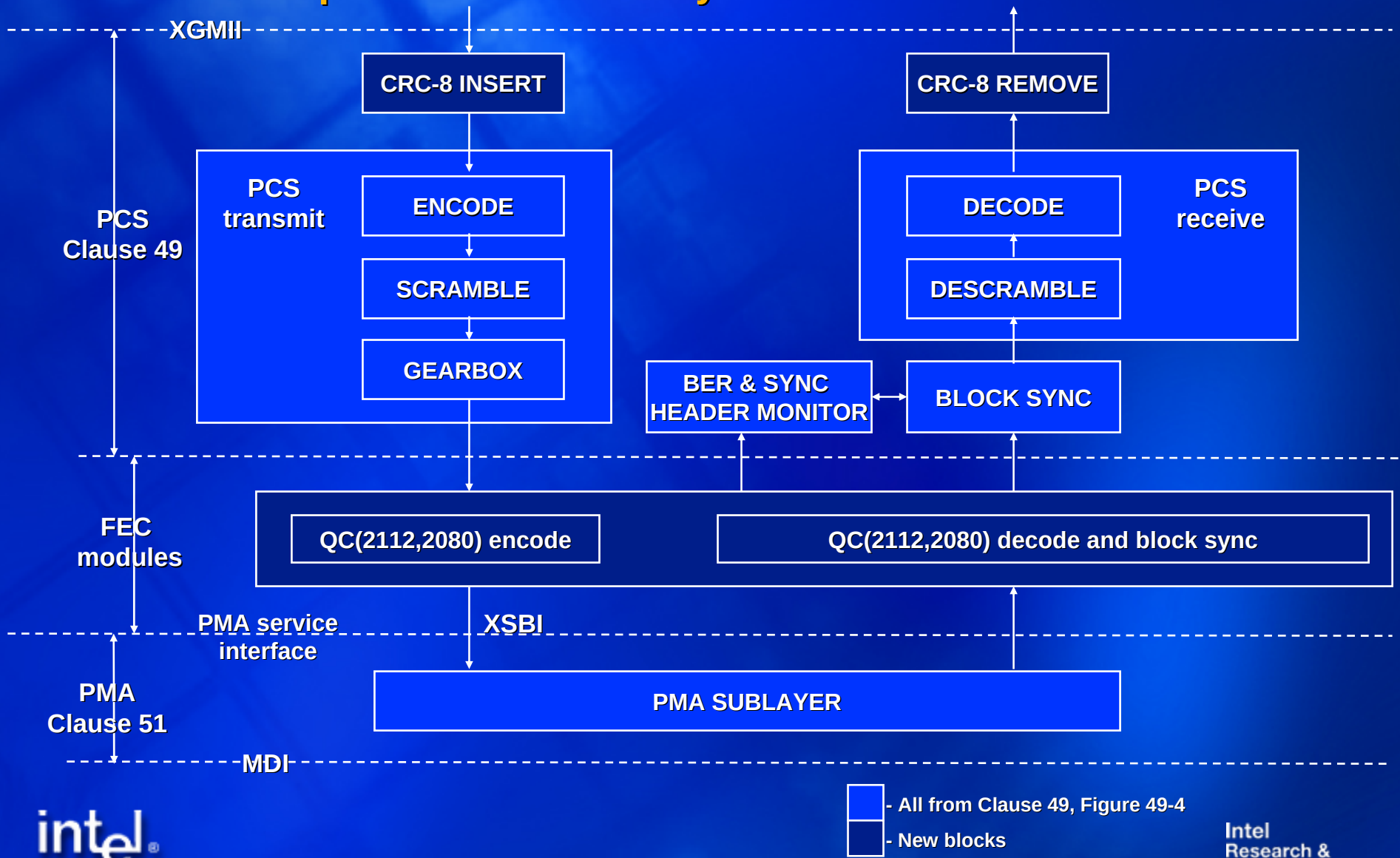
17 May 17, 2005 (r1.0) IEEE P802.3ap Task Force

agere systems

Reference: slide from healey_01_0505.pdf

FEC functional block

Relationship to PCS/PMA sublayers



FEC modules sublayer

- Transparent to PCS and PMA (clauses 49 & 51)
  - 16-bit input and 16-bit output interface
  - Operates on 64b/66b block boundaries
- Uses Quasi Cyclic QC(2112, 2080) burst error correction code
  - For 32 parity check bits 1 of the 2 sync bits from 32 64B/66B blocks is used
  - Encoding latency is 32 bits
- Establishes synchronization at FEC block boundaries (32 64B/66B blocks)
  - Scrambling with PN-2112 sequence is necessary to maintain DC balance and to ensure FEC block sync (any shift in code word is not equal to another)
- Provides 2.5dB energy gain

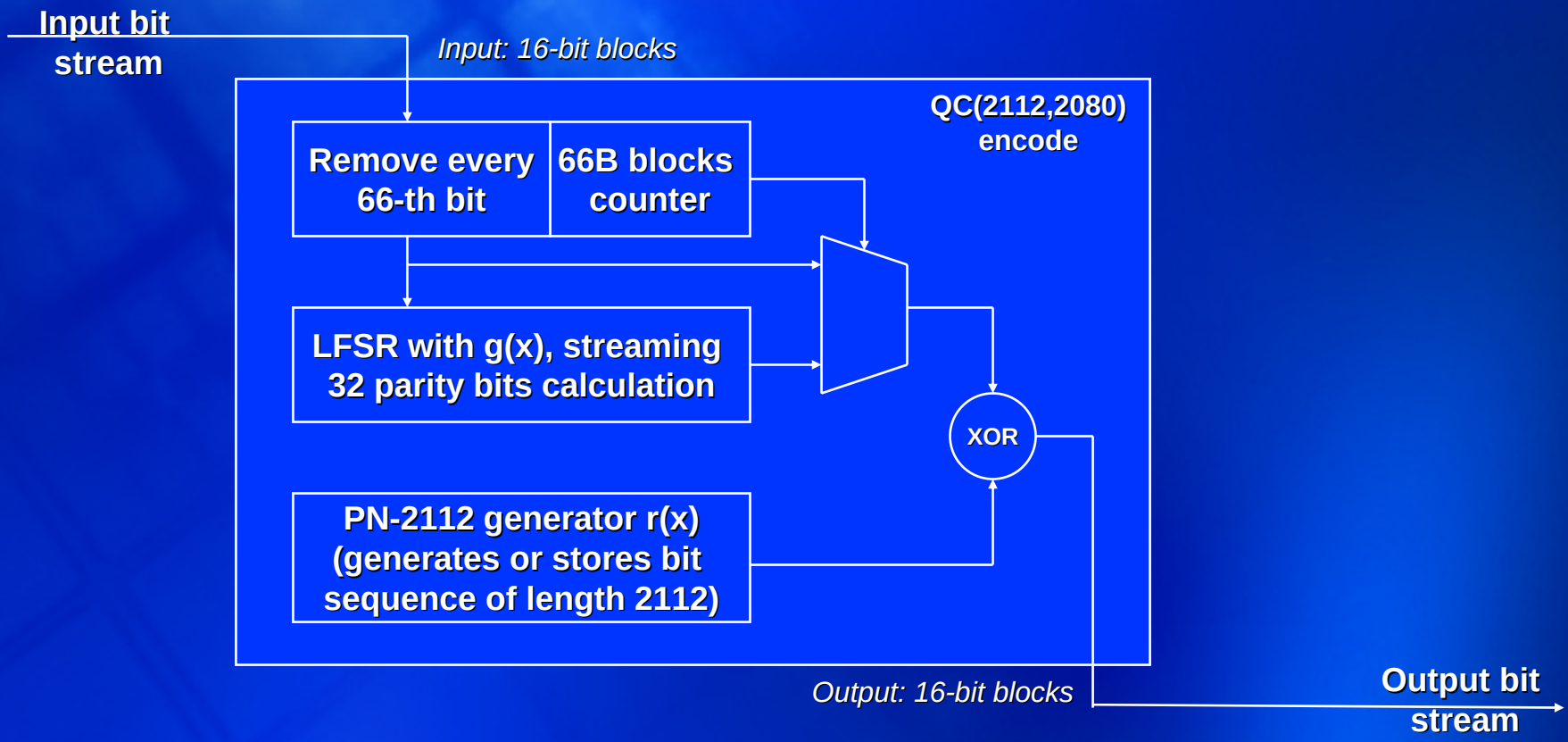
FEC Block Format

T_0	64 Bit Payload Word 0	T_1	64 Bit Payload Word 1	T_2	64 Bit Payload Word 2	T_3	64 Bit Payload Word 3
T_4	64 Bit Payload Word 4	T_5	64 Bit Payload Word 5	T_6	64 Bit Payload Word 6	T_7	64 Bit Payload Word 7
T_8	64 Bit Payload Word 8	T_9	64 Bit Payload Word 9	T_{10}	64 Bit Payload Word 10	T_{11}	64 Bit Payload Word 11
T_{12}	64 Bit Payload Word 12	T_{13}	64 Bit Payload Word 13	T_{14}	64 Bit Payload Word 14	T_{15}	64 Bit Payload Word 15
T_{16}	64 Bit Payload Word 16	T_{17}	64 Bit Payload Word 17	T_{18}	64 Bit Payload Word 18	T_{19}	64 Bit Payload Word 19
T_{20}	64 Bit Payload Word 20	T_{21}	64 Bit Payload Word 21	T_{22}	64 Bit Payload Word 22	T_{23}	64 Bit Payload Word 23
T_{24}	64 Bit Payload Word 24	T_{25}	64 Bit Payload Word 25	T_{26}	64 Bit Payload Word 26	T_{27}	64 Bit Payload Word 27
T_{28}	64 Bit Payload Word 28	T_{29}	64 Bit Payload Word 29	T_{30}	64 Bit Payload Word 30	T_{31}	64 Bit Payload Word 31
32 parity bits							

Total Block length = (32 x 65) + 32 = 2112 bits

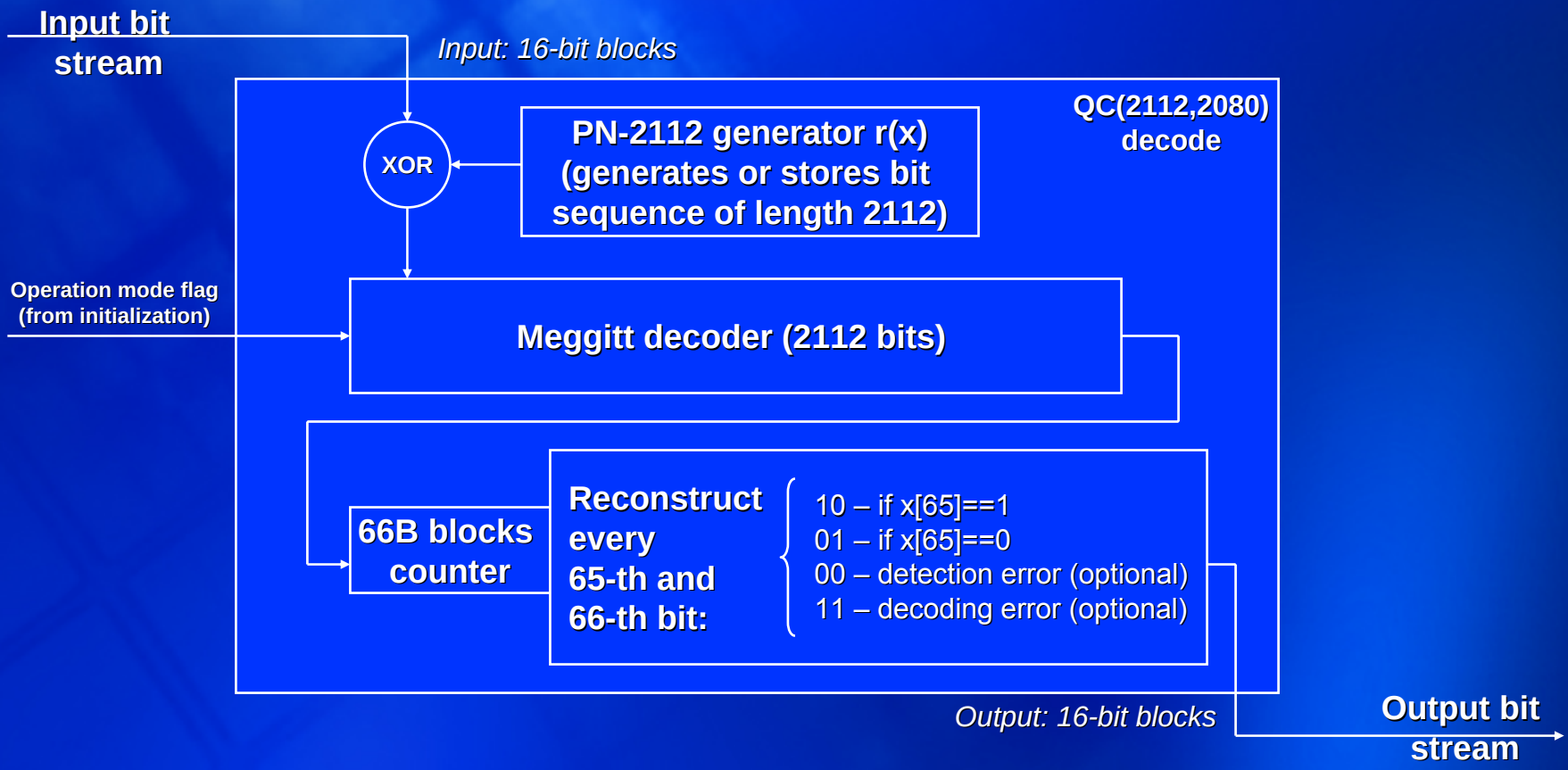
- Payload words carry the 10GBASE-R scrambled payload words
- Tn = Transcode bit carries the state of the 10GBASE-R sync bits for the associated payload word
  - Sync bits are compressed to a single bit then scrambled to ensure DC balance
  - 64b/66b sync bits are either 10 or 01 hence can be reconstructed from the T bit
  - Synchronization is achieved at FEC block level
- Block has the same overhead as 64B/66B encoding

QC(2112,2080) encoding



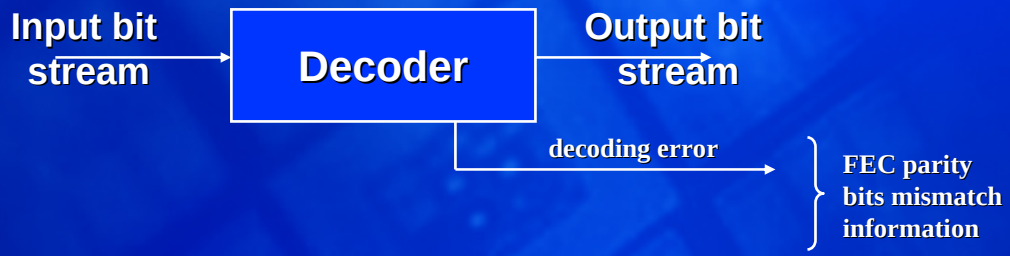
- Output is streaming
- Operation latency is 2 16-bit blocks

QC(2112,2080) decoding



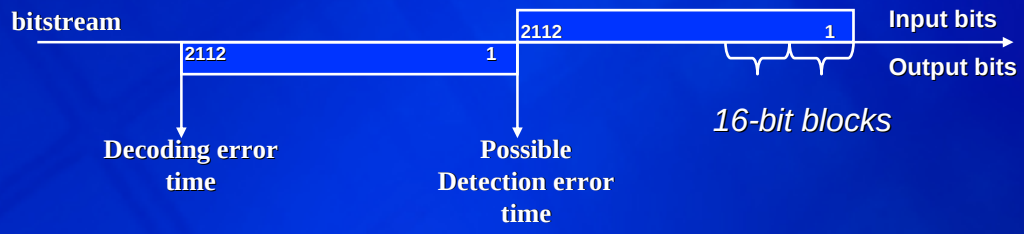
- Output is streaming
- Operation latency is 132 16-bit blocks (approx 200ns at 10.3125G)

Decoding & Error Correction

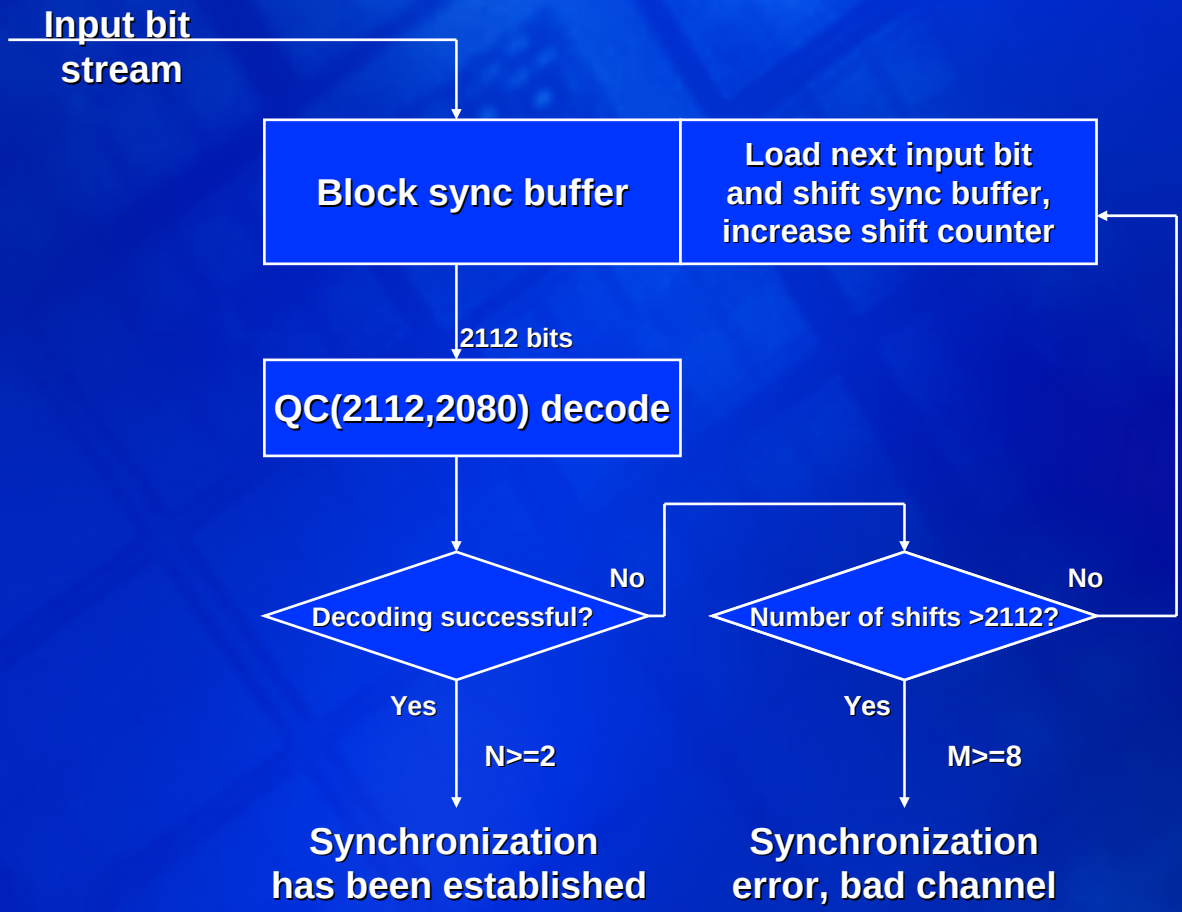


- After the entire codeword is in buffer the decoder knows if there were errors
- To correct errors the decoder should delay 1st input bit until the entire codeword is received (plus delay for correction)
- After processing the decoder knows if there was an unrecoverable error and can indicate it.

Decoding and Error Correction



FEC sublayer synchronization

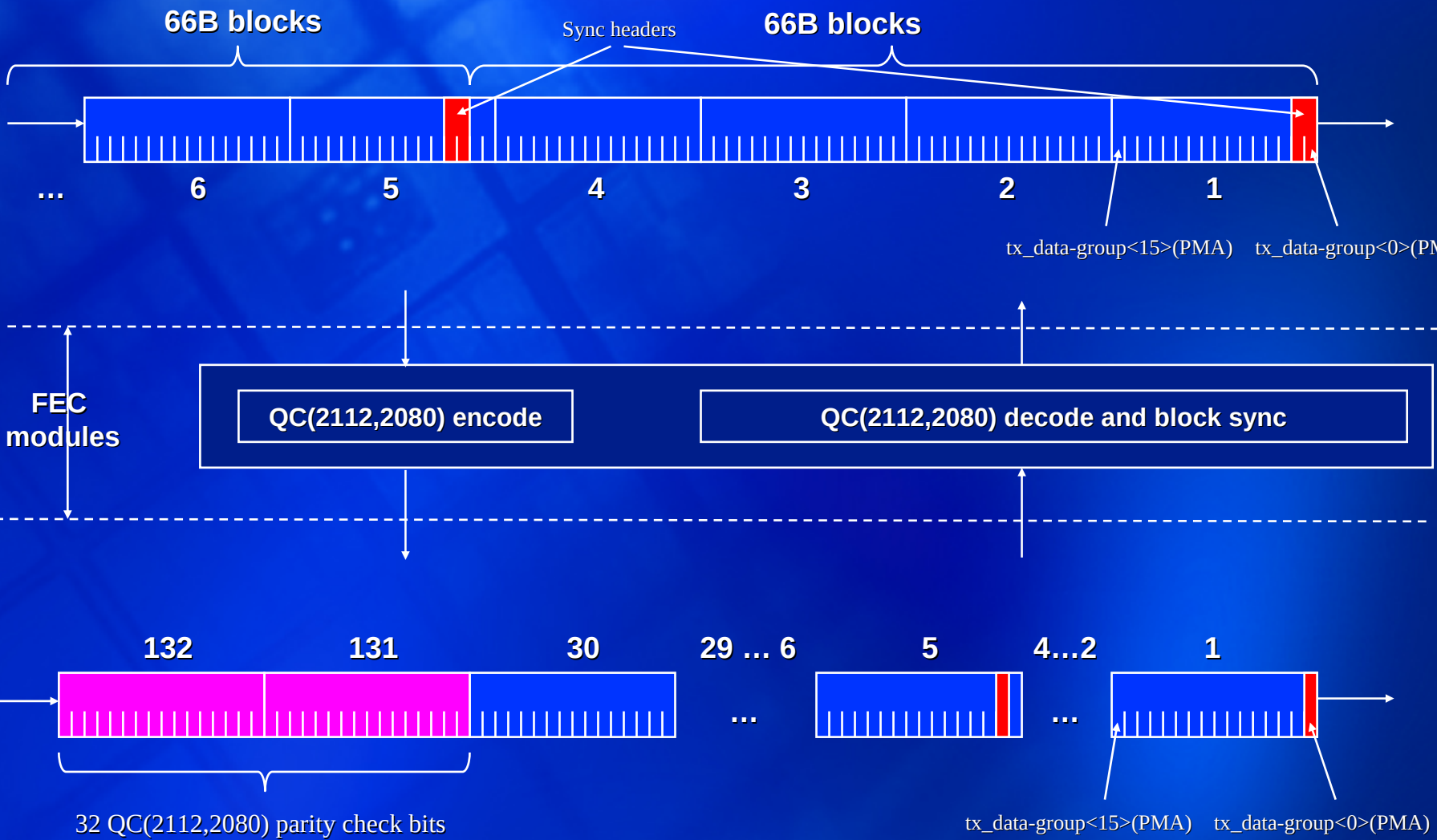


- Use conventional n/m serial locking techniques
- Similar to 64B/66B word sync State Machine
- Requires up to 2112 bit shifts to establish synchronization
- Uses error detection properties of QC(2112,2080) decoder and PN-2112 sequence for frame delineation
- Wrong synchronization probability is lower than 10^{-8}
- Loss of sync is reported if parity check failed for m >= 8 consecutive frames
- Sync is reported if parity check passed for n >= 2 consecutive frames

Block synchronization algorithm

1. Test a candidate block start position
   - FEC decoder decodes block (or evaluates parity) for potential block
     - If it fails shifts candidate start one bit position and tries again
2. Valid potential block start position has good parity for "n" consecutive blocks
   - If any fails shift candidate start one bit position and start again
3. Block Sync is established
4. If "m" consecutive blocks are received with bad parity, drop Block Sync and restart again at 1
5. If "n" consecutive blocks are received with good parity, report "Block Sync"

Transmit bits ordering



Auto-negotiation

- Parameters that should be negotiated during AN
  - Enable FEC (Yes/No)
    - Affects transmit bits ordering and receive decoding
    - No additional Latency when FEC is disabled
- Parameters may be defined in RX
  - Return additional info in 64B/66B sync bits in Decoding mode (Yes/No)
    - Affects 64B/66B decoder compatibility
    - Configuration through Management register in Clause 45 (1.150.3)
- Make changes to Clause 73.6 to include FEC capability bits
  - Bit F0 [D46] to indicate FEC enabled for 10GBASE-KR PHY
  - Make corresponding changes to Clause 45 Tech Ability field registers
  - 10GBASE-KR control register (1.150.2) to indicate FEC enabled for PHY

FEC Implementation

- QC(2112, 2080) encoder:
  - systematic code, no intrinsic latency
  - encoded via single LSR of length 32
- QC(2112, 2080) decoder:
  - allows decoding with only 1 codeword latency
  - uses 3 LFSRs for decoding, requires less than 5K gates in consecutive implementation, power and gate count trade-offs are possible. Other implementations possible

FEC Implementation complexity estimate

- Block code protected frames can be corrected using simple error trapping.
  - Parallel implementations are practical and efficient at 10G data rates
- Area will be comparable to that of a CEI-P implementation
  - Polynomial is longer, but synchronization is much easier
  - See szczepanek_01_0305.pdf for CEI-P details
    - Total Rx/Tx ~= 14K gates + 64x33 dual port RAM @ 312.5Mhz
- Operation Latency
  - 2112+ bits of latency (~ 200ns during normal operation)
- Sync time
  - ~450us worst case during Loss of Sync or Link Start up
    - To parse at all 2112 possible FEC block starts
  - Parallel Implementations will reduce sync latency

Conclusions

- QC(2112, 2080) allows:
  - to have 2.5 dB TX energy gain
  - the BER to go from ~10^{-8} to 10^{-12} or better with same SNR
- Low latency
  - Encoder latency is 32 bits
  - Decoder latency is 2112+ bits (approx 200ns at 10G)
- Synchronization establishing
  - 2112 bits block shifts will find lost sync, continuous sync monitoring during normal operation mode
  - Required only at link start or in case of loss of connection

Proposal

- Include Forward Error Correction (FEC) for 10GBASE-KR PHY
  - FEC sublayer between PCS & PMA (similar to WIS and compatible to clause 49 & 51)
- Use QC(2112,2080) code for FEC
- Changes to Auto-negotiation to advertise FEC Enabled in PHY