

# **Presentation to IEEE P802.3ap Backplane Ethernet Task Force February 2005 Signaling Ad-hoc Session**

**Title:**           **Package & IC Model Impacts**

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**Abstract:**      This contribution provides simulation results comparing impacts of package and IC models.

## Simulations performed across a mix of package/ic model configurations

- ▶ no package, no ic model (ideal 50 ohm terminations only)
- ▶ ind\_like package, no ic model
- ▶ cap\_like package, no ic model
- ▶ no package, ic model
- ▶ ind\_like package, ic model
- ▶ cap\_like package, ic model

## Simulations performed across a subset of ad-hoc channels

- ▶ Tyco Case5, Case6
- ▶ Peters B3, B12

## Simulation setup same as that for results provided in abler\_01\_0105

# Simulation Conditions

## Simulation model summary

▪ Launch amplitude set to minimum	800 mVpp
▪ Transmitter DJ set to maximum	0.15 UIpp
▪ Transmitter RJ set to maximum	0.0107 UIrms (0.15UIpp @ $10^{-12}$ BER)
▪ Tx/Rx termination set to nominal (ideal)	5050/5050 ohms
▪ Receiver DJ	0.10 UIpp
▪ Receiver RJ set to maximum	0.0107 UIrms (0.15UIpp @ $10^{-12}$ BER)
▪ Data rate	10.3 Gbps
▪ Receiver offset	0 ppm
▪ Data pattern	PRBS15
▪ Random noise	1.46mV rms
▪ AC coupling:	4.7nf

## Simulate across package types

- ▶ Spec\_RL\_ind\_like
- ▶ Spec\_RL\_cap\_like
- ▶ Comparison to IBM organic package

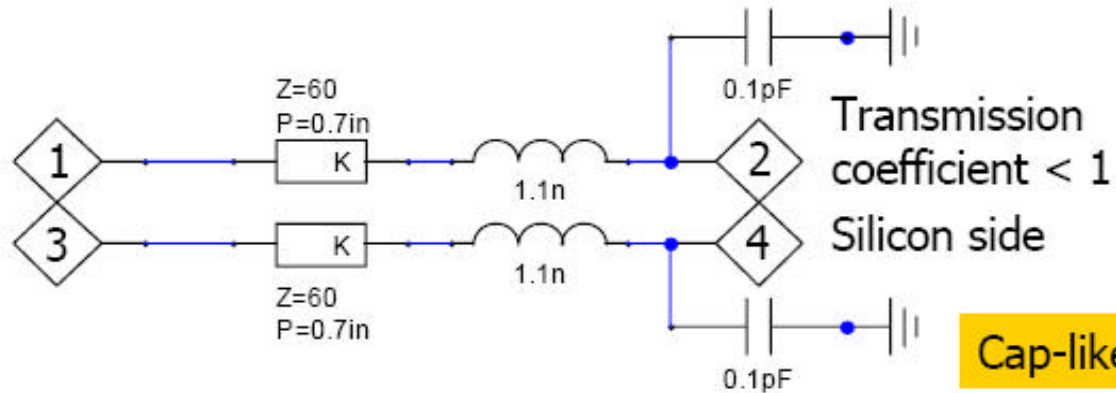
## Simulate FFE3/DFE5 NRZ configuration

- ▶ Includes all crosstalk channels
- ▶ Results provided for BER E-12

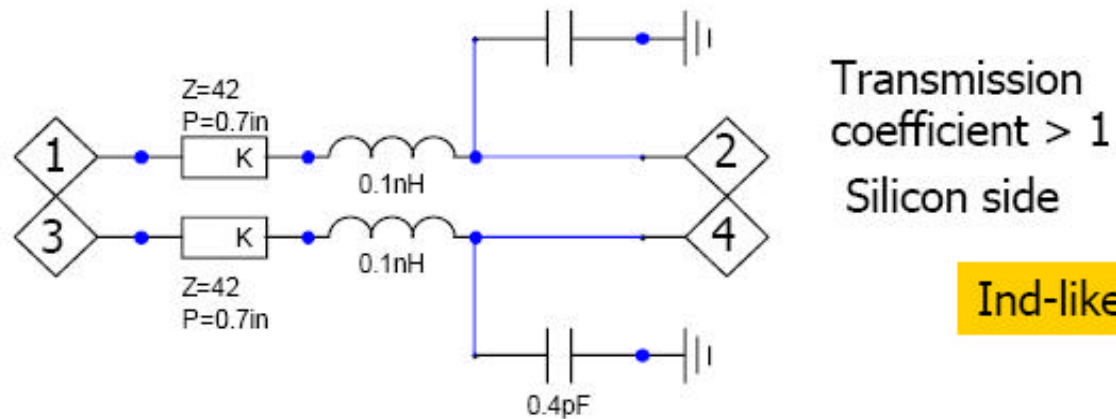
# Package Models (from Mellitz WC Pkg Models)



Pin side  
(PWB)



Pin side  
(PWB)



**Note:** A simple IC model would likely be a shunt C to ground

- ▶ Already captured in package model

# Simulation Results



FFE3/DFE5 (E-12)	Tyco Channels				Peters Channels			
	Case 5		Case 6		B3		B12	
	timing margin (ps <sub>p-p</sub> )	voltage margin (mV <sub>p-p_diff</sub> )	timing margin (ps <sub>p-p</sub> )	voltage margin (mV <sub>p-p_diff</sub> )	timing margin (ps <sub>p-p</sub> )	voltage margin (mV <sub>p-p_diff</sub> )	timing margin (ps <sub>p-p</sub> )	voltage margin (mV <sub>p-p_diff</sub> )
no package, no ic	26.7	55.7	15.6	21.8	9.4	16.9	14.4	25.6
no package, IBM ic	22.7	37.9	10.5	12.7	12.0	23.3	10.2	18.9
cap_like pkg, no addl ic	28.4	47.5	7.0	11.5	0	0	14.1	18.8
cap_like pkg, IBM ic	17.2	30.5	9.9	15.9	0	0.3	4.1	5.6
ind_like pkg, no addl ic	19.4	37.0	5.0	6.3	10.6	23.3	2.5	2.8
ind_like pkg, IBM ic	21.2	36.2	6.1	7.9	5.8	9.2	9.5	15.8
IBM pkg, IBM ic	26.8	44.4	3.7	0.2	3.4	6.0	0	0.2

## Observations

- ▶ Simulation without package model provides overly optimistic results
  - Doesn't account for device return loss
- ▶ Simulation with ind or cap packages in comparison to IBM pkg/ic provides mixed results
  - Dependent on particular channel
  - Impedance matching varies depending on model

# Recommendations

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## Common IC model approach:

- ▶ Would likely be modeled as shunt C to gnd
  - Would simply add to existing cap on package models
- ▶ Package models already defined for -10dB return loss at 5GHz
  - Should not need to be updated

## Package model selection:

- ▶ Results can vary significantly depending on package model and channel
  - One will always provide better matching than the other

## Require simulations to be done with a common package

- ▶ Agree on at least one package to be common across all simulations
  - ind or cap
- ▶ Simulation with 2'nd package is optional