## Proposed remedy for Comment #109 Tom Lindsay

<u>Specifications (for Table 68-3)</u> Transmitter waveform and dispersion penalty (TWDP) max [5 dB proposed]

## Method (for subclause 68.6.4)

The transmitter waveform and dispersion penalty is intended to control deterministic dispersion. A waveform from TP2 of the DUT is to be captured on an oscilloscope for analysis to determine if its performance, when operating in conjunction with channels expected in the application, is within acceptable penalty bounds.

The DUT shall repetitively transmit the BnBi data pattern, as defined in clause 52.9.1.1, or a PRBS7 data pattern through a test patchcord into an O/E converter and through a 4<sup>th</sup>-order 7.5 GHz Bessel-Thomson filter. The filtered output data should then run into the oscilloscope and also into a trigger recovery circuit. The trigger recovery circuit must recover a suitable pattern and/or clock trigger for the scope so that the waveform can be captured and stored. Averaging of at least 16 waveforms, or equivalent, is required. An effective sample rate of at least 8 samples per unit interval is required. If the BnBi pattern is transmitted, then the specific sub-pattern is to be recorded. If PRBS7 is used, then the entire pattern is to be recorded. The DUT must be fully operational in both transmit and receive directions during this test.

The stored waveform is to be analyzed in combination with each of the three emulated channels equivalent to the ISI generators defined in subclause 68.6.5.1 for the TP3 static stressed sensitivity test and with an emulated reference EDC circuit. The reference EDC circuit is defined as equivalent to an infinite length decision feedback equalizer. The stored waveform may be analyzed with the emulated channels and EDC using the algorithm described by the following MATLAB code which calculates the worst penalty from the set of three emulated channels:

[MATLAB code TBD]



<u>Test patterns</u> (goes into new subclause for test patterns – for this test only)

Transmitted sequence Sub-sequence Sub-sequence key BnBi, per clause 52.9.1.1 348 bits, beginning at bit #3258 101010111011011, beginning immediately before the sub-sequence at bit #3242



Optionally, for component (module) testing, a conventional PRBS7, 2<sup>^</sup>7-1 pattern may be used.