# IC Process Choices for 10GBASE-LRM : A Vendor's Perspective

*Badri Gomatam*
*Kevin Witt*
*Adrian Robinson*

# Overview

- Response to D3.1 Comments #3, 29, 30
- The issue has been raised whether the present description of split-symmetric stressor “outlaws” CMOS implementations
- This presentation addresses this issue

- Supporters:
  - Frank Chang, Vitesse
  - Ahmet Balcioglu, Vitesse
  - Kevin Witt, Vitesse
  - Adrian Robinson, Vitesse
  - Badri Gomatam, Vitesse
- Jonathan King, Finisar
- Ali Ghiasi, Broadcom
- Ryan Latchman, Gennum
- Tom Lindsay, Clariphy

# The issues in question

- Issue #1: Split Symmetrical (S-S) Tests as in D3.1
- Issue # 2: Noise Loading as in D3.1
- Suggested Remedy: “…drop S-S test or reduce noise-loading…”
- Concerns That:
  - CMOS Implementations have trouble with Split Symmetric Pulses…
  - the noise Loading “outlaws” low power, low-latency implementations….
  - and
  - integration into XAUI IC’s or other IC’s is restricted

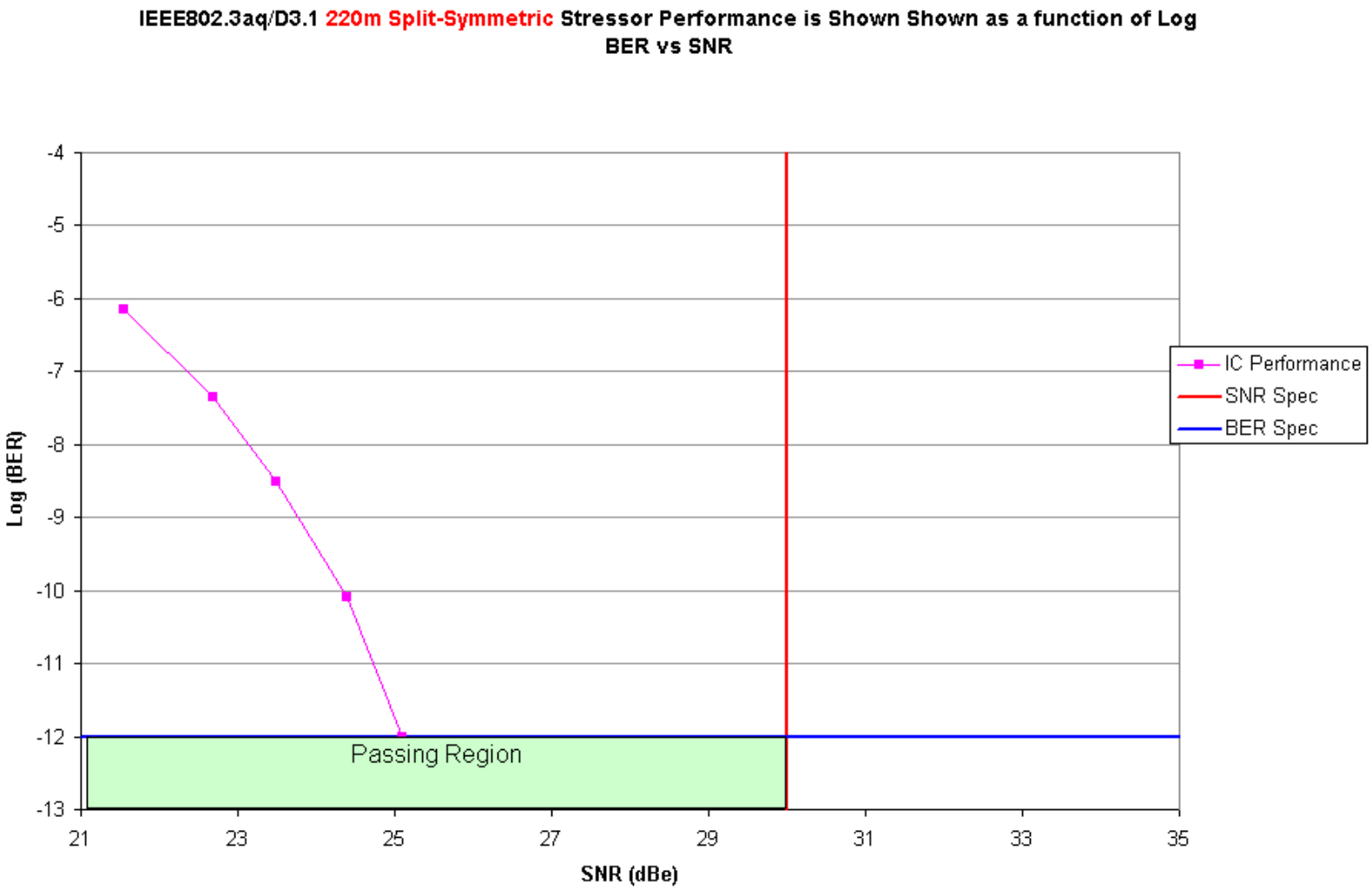
# Our Position on Issue #1

- CMOS is NOT limited by the S-S Test
  - We are not aware of “fundamental” limits to this process for the problem of 10GBASE-LRM
- Vitesse/Others have working implementations in both SiGe and CMOS
- IC Process Choice is up to the implementor
  - Cost, Power  tradeoffs do not affect SiGe negatively
  - For example, a cell phone PA has SiGe, III-Vs AND CMOS combined in 1 package
  - XFP IC’s are competitive in either process choice, as an additional example
- IC Process Choice NOT a constraint for S-S test

# Our Position on Issue #2

- CMOS implementation is NOT limited by the Noise Loading
  - Nothing specific to CMOS…
  - ALL equalizers are affected by noise…
  - conversely, a WELL-DESIGNED circuit is affected much less !
- Vitesse/Others have working implementations in both SiGe and CMOS

# Performance to Noise Loading



# Refer to Interop Report Nov 2005

## Issue 3: The demonstration failed to provide sufficient evidence of technical feasibility

- The interoperation results showed successful interoperability of 4 PMD vendors over 4 lengths of 300m fiber of different types.
- This exceeds both the distance and number of channels required by the motion (which states 1 channel at rated distance).
- All TP2 and virtually all TP3 specifications demonstrated
  - Vendors have stated that they see no problem with remaining specifications.
  - No requests from vendors for related specification relaxations are pending
  - At least one vendor has subsequently reported meeting ALL TP3 specs
- These results exceed earlier interop testing precedents

# Summary

- Vendors can / will meet existing TP3 specifications regardless of IC process choice
- No rationale to change test based on IC process choice…
  - latency
  - power
  - CMOS or SiGe or otherwise
  - integration, size, density
- Prior Interop report concluded readiness to TP3