

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 3.4.2 P37 L24 # 35
 Beia, Christian STMicroelectronics

Comment Type E Comment Status D

In table 33-11a the Mark event Voltage is defined between 6.9V and 10V, while in figure 33-12a (pg 34) the Mark threshold is indicated between 10V and 14.5V. Since the state change is defined by the mark threshold, I propose to add a row in Table 33-11a for the parameter Mark Threshold Vthm, with range between 10V and 14.5V.

SuggestedRemedy

Add parameter Mark Threshold in Table 33-11. Symbol Vthm, Units V, Min 10, Max 14.5.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 33 SC 3.4.2 P37 L26 # 36
 Beia, Christian STMicroelectronics

Comment Type E Comment Status X

The behavior of the PD in the voltage range between 10V and 14.5V is undefined. In this range the PD should sink enough current to discharge the port voltage, and should not exceed the maximum Class 4 current. I propose to add a row in Table 33-11a to define Mark Threshold Current between 0.25mA and 44mA, and to add a paragraph in section 33.3.4.2 to link the Mark Threshold current to the Mark threshold voltage range.

SuggestedRemedy

Add parameter Mark Threshold Current in table 33-11a, Symbol Ithm, Units mA, Min 0.25, Max 44, Additional Information See 33.3.4.2.3
 Add paragraph 33.3.4.2.3 with title Mark Threshold behavior, with text: A Type 2 PD shall not exceed the Ithr current limits when voltage at the PI enters the Mark Threshold voltage specification.

Proposed Response Response Status W

-

Cl 99 SC P1 L # 37
 Diab, Wael Broadcom

Comment Type ER Comment Status D

The draft should have an expiration date on it. This will become more important as we enter more formal reviews. The current language suggests that the document is valid but can change.

SuggestedRemedy

Here is an example from an EFM draft that could be used:

The draft has no special status, and ALL OF IT IS SUBJECT TO CHANGE. The formal expiration date of this draft is April 14, 2004.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Choose an expiration date of the next meeting?

Cl 00 SC P L # 38
 Diab, Wael Broadcom

Comment Type ER Comment Status D

Please make the pdf pages match the draft pages. This will reduce confusion from commenters in TF and WG reviews

SuggestedRemedy

When creating the book for the draft you can have Frame autonumber and you can select the frontmatter chapter to be in roman vs. regular numbers for rest of draft

Proposed Response Response Status W

PROPOSED ACCEPT.

Wael to help Matt with this for the next draft.

Cl 99 SC P3 L2 # 39
 Diab, Wael Broadcom

Comment Type E Comment Status D

Im assuming the box on this page is an editor's note

SuggestedRemedy

Please mark accordingly

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add 'NOTE -' in front of 'This'

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Cl 99 SC P L # 40
 Diab, Wael Broadcom
 Comment Type E Comment Status D
 Please add line numbers on frontmatter
 SuggestedRemedy
 Please add line numbers on frontmatter
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Wael to help editor get line number on frontmatter.

Cl 99 SC P4 L2 # 41
 Diab, Wael Broadcom
 Comment Type E Comment Status D
 Please replace current list of participants with a note that indicates when it will be added
 SuggestedRemedy
 Please replace current list of participants with a note that indicates when it will be added
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Please remove Jefferson and Lincoln placeholders. Add box with note that participants will be added before sending to REVCOM.

Cl 99 SC P14 L # 42
 Diab, Wael Broadcom
 Comment Type E Comment Status D
 Please delete extra page.
 SuggestedRemedy
 One convention is to always have even number pages in the draft so adding a blank page when you end in an odd page is an easy check at the end
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 1 P1 L18 # 43
 Diab, Wael Broadcom
 Comment Type TR Comment Status D
 Line (d) is optional for 802.3af and required for 802.3at baseline. The language should reflect this as we will just have one clause after the project
 SuggestedRemedy
 Append the following text: ""This method i optional for Type I devices and mandatory for Type II devices""
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

The sentence makes no declaration of optional or mandatory, it only refers to methods that are later defined as optional or mandatory. A simple edit is to change it to "Optional or mandatory methods to classify.."
 But I am also OK with not changing it at all.

Cl 33 SC 1 P1 L22 # 44
 Diab, Wael Broadcom
 Comment Type TR Comment Status D
 Item (f) is not accurate. The L2 method is mandatory for all Type 2 devices. It is optional for Type 2 PSEs. Again, as with previous comment this relates to clause 33 becoming the same clause for .3at and .3af
 SuggestedRemedy
 Strike "An Optional" and replace with "A".
 Append the following text. This method is mandatory for all Type 2 devices. It is optional for Type 2 PSEs.
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 The suggested text isn't quite accurate either. "This method is mandatory for all Type 2 POWERED devices."
 I am also OK with just striking optional and leaving the rest as is. (see 43)

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Cl 33 SC Figure 33-3 P19 L2 # 45
 Diab, Wael Broadcom
 Comment Type T Comment Status D
 Im not sure that this figure is now accurate for Gigabit Midspans
 SuggestedRemedy
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 See 119

Cl 33 SC 2 P3 L32 # 46
 Diab, Wael Broadcom
 Comment Type TR Comment Status D
 Deleting the word optional makes the functionality requirement of classification ambiguous for Type 1 vs. Type 2
 SuggestedRemedy
 Append the following sentence to the end of the paragraph: ""The classification function may be optional depending on the Type of PSE""
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 2 P3 L51 # 47
 Diab, Wael Broadcom
 Comment Type TR Comment Status D
 Please delete the word both at the end of that line
 SuggestedRemedy
 Please show technical feasibility that midspans can support both A and B working together on the same link.
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 2.2 P7 L50 # 48
 Diab, Wael Broadcom
 Comment Type TR Comment Status D
 Please reinsert deleted text
 SuggestedRemedy
 I dont think we have had a decision to formally do this yet. I think we have discussed it but never voted on 4-pair explicitly
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 See 113

Cl 33 SC 2.2a P8 L13 # 49
 Diab, Wael Broadcom
 Comment Type TR Comment Status X
 Please change power requirement to PD power delivered.
 SuggestedRemedy
 We know that the objective calls for up to 30W of power at the PD. The final current is still under discussion. I would suggest using the language that a Type 2 PSE will supply at least 30W to the PD
 Proposed Response Response Status W
 see 83, does this satisfy commentor?

Cl 33 SC 2.2a P8 L24 # 50
 Diab, Wael Broadcom
 Comment Type ER Comment Status D
 Is there a reason why we are using a as heading as opposed to a new level or renumbering the subsections
 SuggestedRemedy
 rename to 33.2.2.1
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 See 57.

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CI 33 SC 2.2a P8 L19 # 51
 Diab, Wael Broadcom
 Comment Type E Comment Status D
 ambiguous text
 SuggestedRemedy
 Replace: NOTE-A Type 2 PSE satisfies all requirements of a Type 1 PSE, whereas a Type 1 PSE does not necessarily meet the requirements of a Type 2 PSE.
 with:
 NOTE-A Type 2 PSE is a superset of a Type 1 PSE. A Type 1 PSE may or may not meet the requirements of a Type 2 PSE.
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 33 SC 2.7 P16 L25 # 52
 Diab, Wael Broadcom
 Comment Type T Comment Status D HWvsL1
 The title of HW classification is confusing
 SuggestedRemedy
 Some of the Layer 2 functions may also be implemented in HW. I would suggest something like Layer 1 vs. Layer 2 designation
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 See 55, 52, 54, 65, 224

CI 33 SC 2.7 P16 L27 # 53
 Diab, Wael Broadcom
 Comment Type E Comment Status D
 Delete the following text ""such as load management to be implemented.""
 SuggestedRemedy
 It does not add any value and classification may be implemented for other reasons that are strictly not load management. Further a non-classifying PSE may also do load management
 Proposed Response Response Status W
 PROPOSED REJECT.
 It is only an example and not normative text (may and not shall). This is text from .3af.

CI 33 SC 2.7 P16 L29 # 54
 Diab, Wael Broadcom
 Comment Type T Comment Status D HWvsL1
 Designation of HW for Layer 1 functionality is ambiguous
 SuggestedRemedy
 Replace HW with Layer 1
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 See 55, 52, 54, 65, 224

CI 00 SC P L # 55
 Diab, Wael Broadcom
 Comment Type TR Comment Status D HWvsL1
 Please replace HW Classification with Layer 1 classification as some parts of Link Layer may be performed in HW
 SuggestedRemedy
 See comment
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 See 55, 52, 54, 65, 224

CI 33 SC Table 33-3 P17 L22 # 56
 Diab, Wael Broadcom
 Comment Type TR Comment Status X
 The entry for the classes and class 4 in specific is confusing as it does not capture the capability for the link layer classification to override the HW. Also, for a Link Layer capable Type II it may never have to
 SuggestedRemedy
 Add footnote to explicitly clarify the Link Layer behavior identified in the comment
 Proposed Response Response Status W
 -

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Cl 00 SC P L # 57
Diab, Wael Broadcom

Comment Type ER Comment Status D

Please avoid using subsections with alphanumeric designations.

SuggestedRemedy

Please either renumber the sections or use a new level

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Hugh Barrass had commented (not written, verbally) that this needs to be a difference document with Clause 33 editorial instructions. This would mean the would draft would need reworked - unless these alphanumeric subsections are an attempt at editorial change instructions. The TF needs to determine what IEEE expects as an output from the group.

See 50

Cl 00 SC P L # 58
Diab, Wael Broadcom

Comment Type TR Comment Status X

There is a subtle inconsistency between the classification baseline we adopted and the draft. Specifically, the PD can only expect to see a maximum of 12.95W from the PSE while it waits for the L2 mechanism to come up. The issue in the draft is in several places describing this process it says that the PSE will treat a class 4 PD as it would under HW classification until the L2 engine is up. If I look at the power tables for HW classification they say 36W not 15.4W!

SuggestedRemedy

Please correct the following:

- In describing what a Type-2 PSE that is L2 capable does please specifically call out the limits to the power to be 15.4W consistent with the adopted baseline

- Please qualify the HW power tables with a footnote to explain when these apply for a Type 4

I will try to point out the discrepancies in other comments and specific locations but if I miss something please use this commenry

Proposed Response Response Status W

-

Cl 33 SC 2.7.2a P18 L35 # 59
Diab, Wael Broadcom

Comment Type TR Comment Status D

As with my general comment, this incorrectly implies that a PD with Class 4 can expect to get the full power of 30W if a second mark event is eliminated and while the PSE's L2 engine is coming up

SuggestedRemedy

Please clarify that the limit from the PSE will be 15.4 until the L2 comes up

Proposed Response Response Status W

PROPOSED REJECT.

It already says : "In this case, the Type 2 PSE shall assume it is powering a Type 1 PD until successful link layer classification is performed."

What does "Type 2 PSE shall assume it is powering a Type 1 PD" mean? I read that as 15.4W.

Cl 33 SC 2.7.2a P18 L43 # 60
Diab, Wael Broadcom

Comment Type TR Comment Status D

I like the note. I would suggest that we have a default in case this case happens for some error in the system. Undefined behaviour is scary

SuggestedRemedy

I would suggest that the whole detection process is restarted and no power is applied if the 2 results are different.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This change requires moving from a note to normative text and adding a shall. Need to decide on the action and change the text.

Another option is to power at the first class event level. This is based on the assumption that you have encountered a legacy non-compliant PD and that it is some weird operational mode during the second class event.

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Cl 33 SC 2.7a.1 P20 L5 # 61
 Diab, Wael Broadcom
 Comment Type **TR** Comment Status **X**
 This seems like an example of a packet exchange, I think what is needed is a state diagram
 SuggestedRemedy
 Please remove this diagram or rename it as an example of packet exchange between the PSE and PD.
 Please add a state diagram with variables and conditions that can capture the process. I would suggest that this be part of the work that the L2 ad-hoc we assigned in Geneva generate and review so we can accept as a baseline
 Proposed Response Response Status **W**
 -

Cl 33 SC Tab13 33-5 P23 L32 # 62
 Diab, Wael Broadcom
 Comment Type **TR** Comment Status **X**
 720 mA number is not final
 SuggestedRemedy
 Please footnote the 720 mA number that it is a placeholder and dependent on input from other bodies. Please note that it will require 75% to adopt final number
 Proposed Response Response Status **W**
 No proposed response
 Part of this note does exist on PDF page 2.

Cl 33 SC 3.1 P31 L42 # 63
 Diab, Wael Broadcom
 Comment Type **TR** Comment Status **D**
 I dont recall that we formally made a decision to change the draft from disallowing 4-pairs to treating them as out of scope. The draft should reflect the decisions made in the group, I would request that we retain the old wording and formalize the decision in the TF first.
 SuggestedRemedy
 Please return the original text until we make a formal decision on this in the group
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.

Cl 33 SC 3.2.3 P34 L24 # 64
 Diab, Wael Broadcom
 Comment Type **ER** Comment Status **X**
 Please redraw Figure 33-12a in Frame. It is difficult to maintain non-frame figures in the 802.3 documents once the group is done. for example, modifications due to maintenance are hard.
 SuggestedRemedy
 Please redraw using Frame and similar conventions as used in other state diagrams
 Proposed Response Response Status **W**
 see 115

Cl 33 SC 3.4 P36 L3 # 65
 Diab, Wael Broadcom
 Comment Type **T** Comment Status **D** HWvsL1
 Hardware classification is an ambiguous term
 SuggestedRemedy
 Please use the term Layer 1
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 This change impacts many spots in the doc. The TF should decide if this is enough of a problem to warrant that much editing.
 Suggest a straw poll:
 See 55, 52, 54, 65, 224

Cl 33 SC 3.4a P37 L52 # 66
 Diab, Wael Broadcom
 Comment Type **ER** Comment Status **X**
 Can we reproduce the TLV in the 802.3 document?
 SuggestedRemedy
 Please reproduce the TLV in the 802.3 document, or at the very least circulate with the review package
 Proposed Response Response Status **W**
 -

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Cl 33 SC 3.4a.1 P54 L1 # 67
Diab, Wael Broadcom

Comment Type T Comment Status X

This is not a state diagram

SuggestedRemedy

Please remove or rename figure to indicate example exchange of packets.

Please add a state diagram, preferable the product of a baseline from the L2 ad-hoc

Proposed Response Response Status W

-

Cl 33 SC 3.5.4 P41 L46 # 68
Diab, Wael Broadcom

Comment Type E Comment Status D

Please use subscripts

SuggestedRemedy

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Need to change the RMS, DC and ripple current equation to use subscripts.

See 71

Cl 33 SC 7 P58 L # 69
Diab, Wael Broadcom

Comment Type ER Comment Status D

Please update PICs to reflect Type 1 and Type 2

SuggestedRemedy

Please update PICs

Proposed Response Response Status W

PROPOSED REJECT.

I recommend updating PICs after changes to the normative text are mostly done.

Cl 00 SC P L # 70
Diab, Wael Broadcom

Comment Type E Comment Status D

Im assuming that we will modify Clause 30 as well for management

SuggestedRemedy

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Need specific suggested remedy or editorial instructions. Someone will need to take on the task to edit Clause 30.

Cl 33 SC 3.5.4 P41 L46 # 71
Darshan, Yair Microsemi Corporation

Comment Type E Comment Status D

Draft D0.8

The variables name in lines 40-41 do not match the variables name in the equation

SuggestedRemedy

Change lportdc to lport_dc

Change lportac to lport_ac

Proposed Response Response Status W

PROPOSED ACCEPT.

Also see 68

Cl 33 SC 2.7.1 P17 L2 # 72
Darshan, Yair Microsemi Corporation

Comment Type T Comment Status D

Draft D0.8

Type 2 PSE implementing only type 2 hardware classification is simultaneously indicate its presence and identify Type 2 PD's power requirements.

SuggestedRemedy

Replace ""may"" with ""shall""

Proposed Response Response Status W

PROPOSED REJECT.

What is the PICs statement here? This would be a PD requirement in the PSE section.

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Cl 33 SC figure 33-12a P34 L15 # 73
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

The purpose of class event 3 is to create defined behaviour for type 2 PD when pinged repeatedly by Type 2 PSE.
 There is no need to require that class 3 must consume 40mA.
 It is possible that after two class events the PD will shut off the classification current source due to thermal limitations.

SuggestedRemedy

1. Define class event 3 as follows:
 ""class event 3 is the event when PSE voltage ramps from $V > V_{thm}$ towards V_{on} ""
2. Delete the "" $i=40mA$ "" from Class Event 3.

Proposed Response Response Status W

-

Cl 33 SC 3.5 P40 L17 # 74
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

We require from the PD to support PSE voltage transients less then 50V and down to around 46V.
 If $V_{pse} < 50V$ then $V_{pd} < 41V$

$$V_{pd} = (V_{pse} + (V_{pse}^2 - 4 * R * P_{pd})^{0.5}) / 2.$$

For $P_{pd} = 29.5W$,
 $R = 12.5$ ohms
 V_{pd} is 36V for $V_{pse} = 46.25V$.

In addition we have a concensus that PD input thresholds are as in type 1.

SuggestedRemedy

- Change table 33-12 item 1 from 40V to 36V.
- Change table 33-5 item 2a to 7.5% instead of 7.6%.

Proposed Response Response Status W

-

Cl 33 SC 4.8 P50 L53 # 75
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status D
 Draft D0.8

We need to clearly define that Midspan should provide signal continuity for 1G Midspan as well.

SuggestedRemedy

Change line 53 from ""A Midspan PSE inserted into a channel shall provide continuity for the signal pairs.""

To ""A Midspan PSE inserted into a channel shall provide continuity for the signal pairs for all 4 pairs in 1000BT Midspan device"".

Proposed Response Response Status W

PROPOSED REJECT.

On a gig link, all 4 pairs are the signal pairs. For 10/100, this is only 1,2 and 3,6. People skilled in the art should know the difference already. The sentence is sufficient.

Cl 33 SC 5.9 P53 L36 # 76
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status D
 Draft D0.8

Update a) : If it for PDs only it should be from 36V to 57V.

SuggestedRemedy

Change a) from "" Power classification and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only""

To: ""Power classification and power level in terms of maximum current drain over the operating voltage range, 36V to 57 V, applies for PD only""

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.7.2 P18 L28 # 77
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X
 Draft D0.8:

If PSEs PI voltage must enter to Reset range then PD may lost its indication data

SuggestedRemedy

PSE shall maintain 7V minimum across the PI after classification phase is done and prior to power up.
 PDs should maintain PSE indication data until PD reach to steady state operating mode.
 Other equivalent and implementation independent solutions are OK too.
 (The previous text force using sme kind of memory in PD until PD gets to steady state)

Proposed Response Response Status W
 -

Cl 33 SC Table 33-12 P40 L17-32 # 78
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X
 Draft D0.8:
 Replace this comment and remedy with previous comment sent for draft D0.2:

Table 33-12 items 1 and 4: Need to update numbers

SuggestedRemedy

Item 1: Type 2 PD minimum voltage is $50v - 12.5 * 0.72 * 0.4 / 0.35 = 39.71V$ and not 40V.
 Item 4: Peak operating current at class 4 for type 2 PD:

Considerations:

1. For maximum PD available power.
 The need is with high probability.

$0.72A * 0.4 / 0.35 = 0.823A$. (Same I_{cut}/I_{port} ratio as in 802.3af)

Hence I_{port} peak max is 0.823 for the PD for 50msec max, 5% duty max.

Proposed Response Response Status W
 -

Cl 33 SC 3.1a P32 L13 # 79
 Delveaux, Bill Cisco Systems

Comment Type E Comment Status D
 Lines 13-16 seem redundant.

This basically says to stay a Type 1 PD until you know you are connected to a Type 2 PSE using L2.

This does not need to be said again at this point, or it can be changed to a note if the group decides to leave it. We may also want to consider the same note for the L1 case to be complete.

SuggestedRemedy

Remove lines 13-16

Proposed Response Response Status W
 PROPOSED ACCEPT.

This text is redundant with text on pg 37, line 15. If it is to remain, it should not be normative.

Cl 33 SC 2.7a P20 L1 # 80
 Barrass, Hugh Cisco

Comment Type TR Comment Status D

It does not make sense to include the L2 management function in the PSE and PD subclauses. These subclauses describe the hardware behavior of PSE & PD devices, the management behavior is defined in subclause 33.6. Moving the L2 management description to subclause 33.6 will also remove the unnecessary and confusing repetition of the definition.

SuggestedRemedy

Remove subclauses 33.2.7a and 33.3.4a; move L2 management definition to subclause 33.6.

See attached file for proposed changes. Note that the changes satisfy this and many other comments. The FrameMake source is available on request.

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Group needs to review attached file and approve.

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Cl 33 SC 2.7a P20 L9 # 81
Barrass, Hugh Cisco

Comment Type **TR** Comment Status **D**

The diagram shown is useful but does not meet the requirements of a state machine description.

SuggestedRemedy

Remove subclauses 33.2.7a and 33.3.4a; move L2 management definition to subclause 33.6.

See attached file for proposed changes. Note that the changes satisfy this and many other comments. The FrameMake source is available on request.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Group needs to review attached file and approve.

Cl 33 SC 6.1 P54 L15 # 82
Barrass, Hugh Cisco

Comment Type **TR** Comment Status **D**

There is no management register to indicate the support or to control the use of 2-stage hardware classification.

SuggestedRemedy

Add definitions for register 11 and 12.

See attached file for proposed changes. Note that the changes satisfy this and many other comments. The FrameMake source is available on request.

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Group needs to review attached file and approve.

Cl 33 SC 2.2a P8 L7 # 83
Jetzt, John Avaya

Comment Type **E** Comment Status **D**

The phrase ""This limits"" is misleading in paragraph 2 and 3.

SuggestedRemedy

Paragraph 2:
Change to:
The minimum power the Type 1 PSE may expect to provide to a PD is 15.4 W ...

Paragraph 3:
Change to:
The minimum power the Type 2 PSE may expect to provide to a PD is 36 W ...

Proposed Response Response Status **W**

PROPOSED ACCEPT IN PRINCIPLE.

Cl 33 SC 2.7.2a P17 L41 # 84
Jetzt, John Avaya

Comment Type **E** Comment Status **D**

Table reference is incorrect.

SuggestedRemedy

Change reference to ""Table 33-4a"":
Paragraph 1: twice
Paragraph 2: twice
Paragraph 3: once
Paragraph 3: once

Proposed Response Response Status **W**

PROPOSED ACCEPT.

Cl 33 SC 2.7.2a P18 L23 # 85
Jetzt, John Avaya

Comment Type **E** Comment Status **D**

Reference the Table.

SuggestedRemedy

""... the Vreset range as specified in Table 33-4a, ...""

Proposed Response Response Status **W**

PROPOSED ACCEPT.

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Cl 33 SC 2.7.2a P18 L25 # 86
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Reference the Table.
 SuggestedRemedy
 "... IClass_LIM min, as specified in Table 33-4a, ..."
 "... IMark_LIM min, as specified in Table 33-4a, ..."
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 2.7.2a P18 L30 # 87
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Since "class event" has been defined above, use this term instead of "classification event".
 SuggestedRemedy
 Change "classification event" to "class event" on the lines 30 and 31.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 Class event is also used after. Better to be consistent.
 See comment 91.

Cl 33 SC 2.7.2a P18 L34 # 88
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Enumerate what can be omitted.
 SuggestedRemedy
 "... omit the first mark event, the second class event, and the second mark event ..."
 also in next paragraph, line 39.
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Is this all the text that needs added?

Cl 33 SC 2.7.2a P18 L39 # 89
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Not the "advertised class" but rather the observed class.
 SuggestedRemedy
 "... according to the result of the first class event."
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 The proposed text clarifies the sentence.

Cl 33 SC 2.7.2a P18 L43 # 90
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Amend NOTE.
 SuggestedRemedy
 "NOTE - The result of the first class event and the result of the second class event should agree. If the results do not agree, the behavior of the PD is undefined."
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Semantics: let the group decide the better sentence.

Cl 33 SC 2.7.2a P19 L6 # 91
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Amend parameter names.
 SuggestedRemedy
 Item 1a: Class Event Voltage
 Item 1b: Class Event Current Limitation
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 If comment 87 is accepted this has to be also.

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Cl 33 SC 2.7.2a P20 L1 # 92
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Correct the table number.
 SuggestedRemedy
 ""Insert ... Table 33-4b; ...""
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 2.8 P23 L13 # 93
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Correct parameter name in Table 33-5, Item 1.
 (The title of 33.2.8.1 was changed to Static Output Voltage.)
 SuggestedRemedy
 ""Static output voltage""
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 3.4.2 P36 L50 # 94
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Use complete name of state diagram.
 SuggestedRemedy
 ""... shall conform to the PD Type 2 Classification State diagram in ...""
 Also line 53:
 ""The PD Type 2 Classification State diagram specifies the externally ...""
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 3.4.2 P37 L14 # 95
 Jetzt, John Avaya
 Comment Type E Comment Status D
 First define the PSE Type state variable.
 Clarify the sentence in line 15.
 SuggestedRemedy
 ""The PSE Type state variable is the PSE Type that governs the electrical behavior of the Type 2 PD. Until successful Type 2 hardware classification ... as defined by Table 33-12 of the PD Type identical to the value of its PSE Type state variable.""
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Still think the sentence could use more wordsmithing to make it clear.

Cl 33 SC 3.4.2.1 P37 L40 # 96
 Jetzt, John Avaya
 Comment Type E Comment Status D
 Reference table.
 SuggestedRemedy
 ""... in Table 33-11a.""
 Also in 33.3.4.2.2.
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 2.1 P6 L20 # 97
 Jetzt, John Avaya
 Comment Type T Comment Status D
 Figure 33-4a, Alternatives A and B.
 The Powered End Station should be illustrated to draw power from either set of pairs.
 SuggestedRemedy
 Connect PD to center-taps of all four pairs.
 Proposed Response Response Status W
 PROPOSED ACCEPT.

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.2 P7 L50 # 113
 Jones, Chad Cisco
 Comment Type T Comment Status X
 It does not seem appropriate to delete this text yet. The TF agreed to work out a 2P system first then do the 4P. I'm not sure that only deleting this line is enough to allow 4P.
 SuggestedRemedy
 Undelete the line and we will revisit after 2P is complete.
 Proposed Response Response Status W
 -

Cl 33 SC 2.5.1 P15 L41 # 114
 Jones, Chad Cisco
 Comment Type E Comment Status D
 ""the polarity of Vdetect shall match the polarity of Vport as defined in 33.2.1""
 This should be 33.2.2. We must have missed this in AF.
 SuggestedRemedy
 Change the referred clause to 33.2.2
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 3.2.3 P34 L7 # 115
 Jones, Chad Cisco
 Comment Type E Comment Status X
 Figure 33-12a: This is not drawing in IEEE style. It will need redrawn in the IEEE manner.
 Also want to ask if PD state diagram on pg 33 needs updated?
 SuggestedRemedy
 State Machine AdHoc to make new drawing - hold off on this to encompass all state machines?
 Proposed Response Response Status W
 see 64

Cl 33 SC 3.3 P34 L45 # 116
 Jones, Chad Cisco
 Comment Type E Comment Status D
 '...calculated from the two voltage/current...' Implies that only two measurements are sufficient. This should be 'at least two' to match the text in 33.2.5.1.
 SuggestedRemedy
 change text to: ...calculated from the at least two voltage/current...
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 3.5 P40 L44 # 117
 Jones, Chad Cisco
 Comment Type E Comment Status D
 Units were changed from uF to mF in Item 6.
 SuggestedRemedy
 Change Units in Item 6 to uF
 Proposed Response Response Status W
 PROPOSED ACCEPT.

Cl 33 SC 3.4.1 P36 L9 # 118
 Jones, Chad Cisco
 Comment Type E Comment Status X
 The text makes no statement about Type 1 PDs using Link Layer classification. For sure, manufacturers will do this.
 SuggestedRemedy
 Add the sentence ""A Type 1 PD may optionally choose to implement Type 2 Link Layer classification.""
 Proposed Response Response Status W
 -

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 1.3 P3 L5 # 119
Jones, Chad Cisco

Comment Type T Comment Status X

This drawing needs fixed to include the 1000Mb midspan.

SuggestedRemedy

Add a box coming up from the medium to the PSE to show that the 1000Mb Midspan touches both the medium and the PI.

Proposed Response Response Status W

-

Cl 33 SC 1.3 P5 L1 # 120
Jones, Chad Cisco

Comment Type T Comment Status X

Need drawings that depict 1000Mb endspans or figure 33-4 needs altered to include 4P data transmission in the EndPoint PSE, Alternative A and EndPoint PSE, Alternative B drawings.

SuggestedRemedy

It seems easier to fix the drawings to show 4P data transmission.

Proposed Response Response Status W

-

see 150

Cl 33 SC 2.7.1 P17 L22 # 121
Jones, Chad Cisco

Comment Type T Comment Status X

Missing the legacy function that Type 1 PSEs treat Class 4 PDs as class 0. This is important for the new operation as Type 2 PDs rely on the fact that Type 1 PSEs will classify them as Type 0 and provide 13W.

SuggestedRemedy

Add class 4 - Type 1 - Treat as Class 0 to Table 33-3.

Proposed Response Response Status W

-

Cl 33 SC 3.4.1 P36 L36 # 122
Jones, Chad Cisco

Comment Type T Comment Status X

Missing the legacy function that Type 1 PSEs treat Class 4 PDs as class 0. This is important for the new operation as Type 2 PDs rely on the fact that Type 1 PSEs will classify them as Type 0 and provide 13W.

SuggestedRemedy

add class 4 - type 1 - 0.44W to 12.95W to Table 33-10

Proposed Response Response Status W

-

Cl 33 SC 3.4.2 P37 L36 # 123
Jones, Chad Cisco

Comment Type T Comment Status X

The PD clause is missing the statement that a Type 2 PD will provide external notification when powered by a Type 1 PSE.

SuggestedRemedy

Add the sentence: 'A Type 2 PD that is powered by a Type 1 PSE shall provide external notification to the user signifying that the PD is not running at full power.'

Proposed Response Response Status W

-

Cl 33 SC 2.7.1 P16 L53 # 124
Jones, Chad Cisco

Comment Type T Comment Status X

The statement "'A Type 2 PSE shall implement Type 2 hardware classification'" forces all Type 2 PSEs to implement HW classification. It was agreed that a Type 2 PSE had the option to implement either/or L1/L2 class. This sentence disallows a Type 2 PSE from assuming class 0 and using L2 to move to high power.

SuggestedRemedy

Change "'A Type 2 PSE shall implement Type 2 hardware classification.'" to "'A Type 2 PSE shall implement at least one method of Type 2 classification. Type 2 classifications are Type 2 Hardware classification and Link Layer classification.'"

Proposed Response Response Status W

-

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 3.4.1 P36 L11 # 125
Jones, Chad Cisco

Comment Type T Comment Status X

The statements ""However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3."" and ""Type 2 PDs shall return a Class 4 classification signature in accordance with the maximum power draw..."" forces Type 2 PDs to only draw more than 12.95W. Why is it illegal for me to make a Type 2 PD that is Class 2 then uses LLDP to further refine the power consumption, say down to 5W? If I am forced to advertise Class 4 there will be situations where my PD could be powered by a PSE but won't be because the PSE has more than 7.0W but less than 15.4W left in reserve.

SuggestedRemedy

The text in 33.3.4.1 and 33.3.4.2 needs reworked to reflect this operating condition.

Proposed Response Response Status W

-

Cl 33 SC 2.1 P5 L8 # 150
Schindler, Fred Cisco

Comment Type T Comment Status D

System topology is not shown for 1 GBPS end-points.

SuggestedRemedy

The system topology should be shown for 1 GBPS end-points.

Proposed Response Response Status W

PROPOSED ACCEPT.

See 120

Cl 33 SC 2.7a P20 L3 # 151
Schindler, Fred Cisco

Comment Type T Comment Status X

The whole section needs to be reworked. An IEEE 802.3 state diagram is required.

SuggestedRemedy

Have the task force review the feedback Hugh Barrass provides.

Proposed Response Response Status O

Cl 33 SC 2.2a P8 L8 # 152
Schindler, Fred Cisco

Comment Type TR Comment Status X

All references requiring a PSE to provide 15.4 W minimum do not match the state diagram shown in figure 33-6. Also see p24, item 14.

SuggestedRemedy

All references requiring a PSE to provide 15.4 W minimum need to be changed to match the state diagram shown in figure 33-6.

Proposed Response Response Status O

Cl 33 SC 2.2a P8 L15 # 153
Schindler, Fred Cisco

Comment Type TR Comment Status X

Existing thresholds in table 33-5 set design requirements that are not required for interoperability.

SuggestedRemedy

This specification shall provide requirements to ensure interoperability.

A legacy PD can be powered using PoE plus requirements. For example, a legacy PD is required to draw less than 400 mA (table 33-12, item 4) and a legacy PSE is required to limit current (table 33-5, item 8). If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with no design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits.

Proposed Response Response Status O

Cl 33 SC 2.7.2a P17 L41 # 154
Schindler, Fred Cisco

Comment Type TR Comment Status X

The duration required to ensure reset occurs is not specified.

There are also several typos in this section including a repeat of p18, lines 25-16.

SuggestedRemedy

Add a specification for the reset minimum duration.

If the corrections are not obvious please see me and I will show them to you.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.8 P23 L20 # 155
Schindler, Fred Cisco

Comment Type TR Comment Status X

The existing IEEE specification should not be changed and the definitions for type-1 and type-2 are not clear.

SuggestedRemedy

The Vtran_lo is applicable only to PSEs that provide a minimum 50 V static supply.

The definitions for type-2 and type-1 are related to how each system classifies power. The other requirements, such as supply voltage, fall into place automatically because only a new PD will request power using new power classification mechanisms. A legacy PD that requests power using new mechanism is provided with power that meets its needs too.

Proposed Response Response Status O

Cl 33 SC 2.8.4 P25 L33 # 156
Schindler, Fred Cisco

Comment Type TR Comment Status X

The statements are not clear: is ""a"" or ""b"" required?
Allowing ""b"" to be used breaks interoperability because a PD can draw 400 mA.
Option ""b"" has no time or duty cycle constraint provided. These comments also apply to the new section 33.2.8.4a.

SuggestedRemedy

Allow options ""a"" or ""b.""
Have one statement for duty cycle and time that applies to both ""a"" and ""b"".
Correct the PD section on page 40 item 4 to show that current peaks are scaled with voltage.

The same comments apply to section 33.2.8.4a and table 33-12.

Proposed Response Response Status O

Cl 33 SC 2.8.6 P26 L12 # 157
Schindler, Fred Cisco

Comment Type TR Comment Status X

The text does not explicitly state that this applies to L2 and L1 classification mechanism.

SuggestedRemedy

Include a reference to 33.2.7a (L2 classification).

Proposed Response Response Status O

Cl 33 SC 2.7a P20 L5 # 158
Schindler, Fred Cisco

Comment Type TR Comment Status X

Resolution between L1 and L2 power classification mechanisms is not explicitly stated.

SuggestedRemedy

Indicate in the appropriate area(s) that L2 power values take precedence over L1 power values.

Proposed Response Response Status O

Cl 33 SC 2.8.8 P26 L25 # 159
Schindler, Fred Cisco

Comment Type TR Comment Status X

The specification requires that a port voltage remains above 44 V (Table 33-5, item 1) and that it limits current to 400 mA (Table 33-5, item 5). Both of these can not occur at the same time.

SuggestedRemedy

This specification shall provide requirements to ensure interoperability.

A device that draws more than 400 mA is not interoperable with this specification. The specification should not demand that PSE provide power for noncompliant devices. See the latest Vport ad hoc slides on ""IEEE 802.3 concern"" with PD and PSE interoperability during a PSE dv/dt event.

If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with less design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.8 P23 L49 # 160
Schindler, Fred Cisco

Comment Type TR Comment Status X

The specification requires that a PSE remove power based on an upper ICUT threshold and this level is not required to ensure interoperability or meet the safety specifications, and therefore, forces a design requirement.

SuggestedRemedy

This specification shall provide requirements to ensure interoperability.

A device that draws more than 400 mA is not interoperable with this specification. The specification should not demand that PSE provide power for noncompliant devices. See the latest Vport ad hoc slides on ""IEEE 802.3 concern"" with PD and PSE interoperability during a PSE dv/dt event.

Suggested solution: removing the ICUT maximum threshold. The same solution can be used for all PSE types.

Proposed Response Response Status O

Cl 33 SC 2.8 P24 L6 # 161
Schindler, Fred Cisco

Comment Type TR Comment Status X

The specification requires that a PSE remove power based on an upper Tovld threshold and this level is not required to ensure interoperability or meet the safety specifications, and therefore, forces a design requirement.

SuggestedRemedy

This specification shall provide requirements to ensure interoperability.

If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with less design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits. The same value can be used for all PSE types.

Solution remove the Tovld maximum and use the Vport ad hoc SOA.

Proposed Response Response Status O

Cl 33 SC 2.8 P24 L18 # 162
Schindler, Fred Cisco

Comment Type TR Comment Status X

The specification requires that a PSE remove power based on an upper ILIM threshold and the selected level is not required to ensure interoperability or meet the safety specifications, and therefore, is unnecessarily restrictive.

SuggestedRemedy

This specification shall provide requirements to ensure interoperability.

If a PSE provides current that meets system safe operating (SOA) requirements, IEC 60950, and PD minimum power needs, then safety and interoperability are met with less design requirements imposed. Within the region between PD current needs and SOA current limits, a PSE system selects the design (current limit, current cut-off, and duration) that meets its markets needs. See Vport ad hoc current limit presentations for the latest proposed system current vs time limits. The same value can be used for all PSE types.

Solution remove the ILIM maximum and use the Vport ad hoc SOA. Also do not require that a PSE go into current limit. A minimum current vs time requirement for interoperability is provided in the Vport ad hoc presentations.

Proposed Response Response Status O

Cl 33 SC 2.8.12 P27 L1 # 163
Schindler, Fred Cisco

Comment Type TR Comment Status X

The current imbalance requirements need to be reevaluated for PoE plus levels. In addition, millions of PoE ports are in use with cable lengths significantly less than 80 m. A short cable length increases the current imbalance to levels where transforms can not guaranty the 350uH inductance requirement of IEEE 802.3. Therefore, assumptions made by the IEEE should be re-evaluated.

SuggestedRemedy

A transformer ad hoc should be formed to create system requirements for Ethernet transforms that ensure compliant systems are acceptable to the broader market.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.10.1.2 P28 L30 # 164
Schindler, Fred Cisco

Comment Type TR Comment Status X

The text in table 33-6 is not clear for item 1a. The average value of Vport is less than 57 V, and the peak value is less than 60V.

SuggestedRemedy

Under the max column:
10% of the average value provided within the limits of table 33-5 item 1.

Proposed Response Response Status O

Cl 33 SC 2.10.1.2 P29 L47 # 165
Schindler, Fred Cisco

Comment Type TR Comment Status X

The specification is not consistent for the location of the Cpd_d capacitor. Figure 33-6 indicates either location is ok, but table 33-13 item 3 calls out 0V stimulus for the same capacitance. With 0 V stimuli the diodes will not conduct. Also see p43 line 33.

SuggestedRemedy

The task force needs to determine what is required for Cpd_d in order to me both DC and AC disconnect requirements. It appears that AC disconnect requires Cpd_d on the Ethernet line side of the diodes while DC disconnect works with Cpd_d on either side.

Proposed Response Response Status O

Cl 33 SC 12a P34 L5 # 166
Schindler, Fred Cisco

Comment Type TR Comment Status X

The diagram needs to be redrawn to meet IEEE state diagram requirements.

SuggestedRemedy

Form an ad hoc to create the state diagram.

Proposed Response Response Status O

Cl 33 SC 3.4.1 P36 L24 # 167
Schindler, Fred Cisco

Comment Type TR Comment Status X

Table 33-10 is not clear. Why is a range of maximum stated? Does a class 2 PD need to draw at least 3.84 W?

A type 2 PD should be able to produce all classes.

SuggestedRemedy

See my previous comments on definition of type. Allow a new PD to request the power it needs.

Proposed Response Response Status O

Cl 33 SC 3.5 P40 L17 # 168
Schindler, Fred Cisco

Comment Type TR Comment Status X

Table 33-12, item 1 is provides the minimum PD voltage at ICUT_MIN. Therefore, a type-2 PD would expect 41 V when it draws 29.5W.

SuggestedRemedy

Change the type 2 PD minimum voltage to 41 V.

Proposed Response Response Status O

Cl 33 SC 3.5 P40 L24 # 169
Schindler, Fred Cisco

Comment Type TR Comment Status X

The peak operating current specified in this section is Pport_max/Vport. It is not clear that Pport_max is the power the PD is classified to because the Iport max of table item 4 contradicts this. For example, a class 3 PD can draw 6.49 W and with a 36 V input will draw $6.49/36 = 180$ mA. The value in item 4 states 210 mA.

Also see a related comment on this same parameter. It is also not clear which Iport is being referenced-table 33-12 has items 4 and 5 with the same name.

SuggestedRemedy

The task force needs to review these values and state what ensures interoperability.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 3.5.4 P41 L37 # 170
 Schindler, Fred Cisco
 Comment Type **TR** Comment Status **X**
 Some people in the task force are confused how to calculate duty cycle.
 SuggestedRemedy
 State that duty cycle is calculated using a sliding window with a 1 second width around any level above Pport_max/Vport.
 Proposed Response Response Status

Cl 33 SC 2.7.1 P17 L21 # 171
 Schindler, Fred Cisco
 Comment Type **TR** Comment Status **X**
 A legacy PSE seeing class 4 will provide class 0 power. A new PSE seeing the new hardware classification mechanism and seeing class 4 will provide at least TBD power.
 SuggestedRemedy
 Add text for a legacy PSE and new PSE response as shown above.
 Proposed Response Response Status

Cl 33 SC 4.1 P44 L17 # 172
 Schindler, Fred Cisco
 Comment Type **TR** Comment Status **X**
 We should be using the IEEE 802.3 clause 33 that was modified to reinstate DC high pot testing created during the IEEE 802.3au efforts.
 SuggestedRemedy
 Use the work accepted in IEEE 802.3au see http://grouper.ieee.org/groups/802/3/poep_study/public/may05/law_1_0505.pdf.
 Proposed Response Response Status

Cl 33 SC 4.4 P46 L25 # 173
 Schindler, Fred Cisco
 Comment Type **TR** Comment Status **X**
 This specification is not consistent with its common mode noise measurement requirements. Clause 33 is for a PSE specifies a range of 1 MHz to 100 MHz. Other clauses are for a MDI signal pairs and have no concept of measurement BW.
 Testing during clause 33 development ensured data integrity with the constraints imposed. Reducing the BW of existing clause common mode measurements should not reduce the compliance of legacy systems. Requiring PSE to meet other clauses below 1 MHz places an unnecessary cost burden on the system.
 SuggestedRemedy
 Modify other clauses or place a statement in clause 33 that allows the Ethernet MDI to use the clause 33 common mode requirements whether PoE power is present or not.
 Proposed Response Response Status

Cl 33 SC 3.5.4 P41 L46 # 195
 Darshan, Yair Microsemi Corporation
 Comment Type **E** Comment Status **X**
 Draft D0.8
 The variables name in lines 40-41 do not match the variables name in the equation
 SuggestedRemedy
 Change lportdc to lport_dc
 Change lportac to lport_ac
 Proposed Response Response Status

Cl 33 SC 3.5 P40 L44 # 196
 Darshan, Yair Microsemi Corporation
 Comment Type **E** Comment Status **X**
 PD minimum capacitance should be 5uF and not 5mF
 SuggestedRemedy
 Change to 5uF as in original document.
 Proposed Response Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.7.1 P17 L2 # 197
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

Type 2 PSE implementing only type 2 hardware classification is simultaneously indicate its presence and identify Type 2 PD's power requirements.

SuggestedRemedy

Replace ""may"" with ""shall""

Proposed Response Response Status O

Cl 33 SC figure 33-12a P34 L15 # 198
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

The purpose of class event 3 is to create defined behaviour for type 2 PD when pinged repeatedly by Type 2 PSE.
 There is no need to require that class 3 must consume 40mA.
 It is possible that after two class events the PD will shut off the classification current source due to thermal limitations.

SuggestedRemedy

1. Define class event 3 as follows:
 ""class event 3 is the event when PSE voltage ramps from $V > V_{thm}$ towards V_{on} ""
2. Delete the "" $i=40mA$ "" from Class Event 3.

Proposed Response Response Status O

Cl 33 SC 3.5 P40 L17 # 199
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

We requires from the PD to support PSE voltage trnsients less then 50V and down to around 46V.
 If $V_{pse} < 50V$ then $V_{pd} < 41V$

$$V_{pd} = (V_{pse} + (V_{pse}^2 - 4 * R * P_{pd})^{0.5}) / 2.$$

For $P_{pd} = 29.5W$,
 $R = 12.5$ ohms
 V_{pd} is 36V for $V_{pse} = 46.25V$.

In addition we have a concensus that PD input thresholds are as in type 1.

SuggestedRemedy

Change table 33-12 item 1 from 40V to 36V.
 Change table 33-5 item 2a to 7.5% instead of 7.6%.

Proposed Response Response Status O

Cl 33 SC 4.8 P50 L53 # 200
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

We need to clearly define that Midspan should provide signal continuity for 1G Midspan as well.

SuggestedRemedy

Change line 53 from ""A Midspan PSE inserted into a channel shall provide continuity for the signal pairs.""

To ""A Midspan PSE inserted into a channel shall provide continuity for the signal pairs for all 4 pairs in 1000BT Midspan device"".

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 5.9 P53 L36 # 201
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Draft D0.8

Update a) : If it for PDs only it should be from 36V to 57V.

SuggestedRemedy

Change a) from "" Power classification and power level in terms of maximum current drain over the operating voltage range, 44V to 57 V, applies for PD only""

To: ""Power classification and power level in terms of maximum current drain over the operating voltage range, 36V to 57 V, applies for PD only""

Proposed Response Response Status O

Cl 33 SC 2.1 P6 L6 # 202
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status D

Figure 33-4a:

1. The data transformer in Midspan is one way to combine power with data. Other implementations are possible.

2. According to 802.3af spec. the PD should have provisions to be able to get power from either pairs. See figure 33-4.

SuggestedRemedy

1. Replace the data transformer in the Midspan with a black box which indicates implementation independent data data and power interface. See attached drawing.

2. Fix the PD part in 33-4a by copying the PD part from 33-4.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Not sure it is necessary to change the data xfmr. This is only an informative illustration. Those skilled in the art will know that there are other options.

Cl 33 SC 2.8 P24 L20 # 203
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X

Classification time T_{pd}c for type 1 and 2 PSE's are different.

SuggestedRemedy

Split item 20 in table 33-5 for type 1 and type 2 PSEs:

Add the following data for type 2 PSE:

T_{pd}c min. = 12msec for PSE using layer 2 which uses only single finger.

T_{pd}c max.= 84msec for PSE using two fingers at max timing values.

Ad the following note in the additional information column: ""T_{pd}c does'nt include V_{class} and mark tr,tf timing values which are derived from PD current load being used and system capacitance at the classification phase.""

Proposed Response Response Status O

Cl 33 SC 2.7.2 P18 L28 # 204
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

Drafr D0.8:

If PSEs PI voltage must enters to Reset range then PD may lost its indication data

SuggestedRemedy

PSE shall maintain 7V minimum across the PI after classification phase is done and prior to power up.

PDs should maintain PSE's indication data until PD reach to steady state operating mode.

Other equivalent and implementation independent solutions are OK too.

(The previous text force using some kind of memory in PD until PD gets to steady state)

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC Table 33-12 P40 L1732 # 205
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

Draft D0.8:
 Replace this comment and remedy with previous coment sent for draft D0.2:

Table 33-12 items 1 and 4: Need to update numbers

SuggestedRemedy

Item 1: Type 2 PD minimum voltage is 50v-12.5*0.72*0.4/0.35=39.71V and not 40V.

Item 4: Peak operating current at class 4 for type 2 PD:

Considerations:

- For maximum PD available power.
 The need is with high proability.

0.72A*0.4/0.35 = 0.823A. (Same Icut/Iport ratio as in 802.3af)

Hence Iport peak max is 0.823 for the PD for 50msec max, 5% duty max.

Proposed Response Response Status O

Cl 33 SC 3.5.4 P41 L46 # 206
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

Text is missing for type 2 PD.
 The rms and dc value of Iport should be defined in similar way as in type 1 PD.

SuggestedRemedy

Change lines 48-49 as follows:
 From ""The maximum IPort_dc and IPort_rms values for all operating VPort range shall be defined by the following equation: IPort_max [mA] =12950/VPort.""

To ""The maximum IPort_dc and IPort_rms values for all operating VPort range shall be defined by the following equation:
 for type 1 PD: IPort_max [mA] =12950/VPort A.
 for type 2 PD: IPort_max [mA] =29500/VPort A.

Proposed Response Response Status O

Cl 99 SC P1 L1 # 219
 Law, David 3Com

Comment Type E Comment Status D

While the front matter is not within scope of any ballot please consider the following comments.

- Add a TM symbol after IEEE 802.3at on its first instance in the top right.
- Add the text '(Amendment to IEEE Std 802.3(tm)-200X)' below standard designation in top right.
- Add a TM symbol after IEEE 802.3at on its second instance upper left.
- Change 'Draft: IEEE P802.3at ...' to read 'IEEE P802.3at ...'
- Change 'IEEE Standard ...' to read 'Draft standard ...'
- Correct the title to match the PAR - this reads 'Amendment: DTE Power via the MDI Enhancements'. It probably would be okay to spell out DTE even though the PAR doesn't - but need to delete the leading 'Enhanced'.
- Change 'Sponsor' to read 'Prepared by the'.
- Move the text 'This draft ...' to after 'IEEE Computer Society'.

[9] Update the boilerplate text to that found in the 2007 style manual, this reads 'This document is an unapproved draft of a proposed IEEE Standard. As such, this document is subject to change. USE AT YOUR OWN RISK! Because this is an unapproved draft, this document must not be utilized for any conformance/compliance purposes. Permission is hereby granted for IEEE Standards Committee participants to reproduce this document for purposes of international standardization consideration. Prior to adoption of this document, in whole or in part, by another standards development organization, permission must first be obtained from the IEEE Standards Activities Department. Other entities seeking permission to reproduce this document, in whole or in part, must obtain permission from the IEEE Standards Activities Department.'

- Add line numbers to front matter.
- Add an draft expiration date.
- While the style manual states that lower case roman numerals should be used for the front matter please change to arabic numerals so that the page number match the pdf page number.

See [http://standards.ieee.org/guides/style/2007_Style_Manual.pdf#Page=42] as well as IEEE 802.3ay draft.

SuggestedRemedy

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.7.1 P33 L1 # 226
 Law, David 3Com
 Comment Type ER Comment Status X
 The text describing the need for Type 2 hardware classification to be mandatory is a duplication of the text in 33.2.7 (page 32, line 31).
 SuggestedRemedy
 Delete the text found on lines 1 through 4.
 Proposed Response Response Status O

Cl 33 SC 3.5.2 P57 L26 # 227
 Law, David 3Com
 Comment Type ER Comment Status X
 Please follow the correct format for equations define in the IEEE Style guide [http://standards.ieee.org/guides/style/2007_Style_Manual.pdf#Page=29]. Additional formatting information can be found at [<http://www.ieee802.org/3/tools/editorial/requirements/scc14.html>].

In addition for these specific equations it is not clear that the measurement using 20 Ohms for type 1 and 12.5 Ohms for Type 2 are mandatory. If they are, as I suspect they are, they should be shall statements.

SuggestedRemedy

This formatting needs to be carried on the entire draft or there is the possibility that SCC14 may try to force these changes during sponsor ballot and RevCom submittal - SCC14 is a mandatory coordination [<http://standards.ieee.org/faqs/coord.html>].

In this particular case the equation should be changed as follows:

[1] The text 'where:' followed by a list of variables with their definition should be provided.

[2] The letter symbols for physical quantities, mathematical variables, indices and general functions (as opposed to mathematical functions), are always printed in italic. In this case P, V and I should be italic. Subscripts and superscripts follow the same rules. Symbols for physical quantities, mathematical variables, indices and general functions are printed in italic. Therefore in this case 'Port' should be in upright font as it is not a symbol for a variable.

To address the measurement specification issue the resistances should be included in shall statements. This subclause would therefore read:

The specification for PPort in Table 33-12 shall apply for the input power averaged over 1 second. For a Type 1 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 20 W in series. For a Type 2 PD PPort shall be measured when the PD is fed by 44 V to 57 V with 12.5 W in series. PPort is defined as:

$$P_{Port} = V_{Port} \times I_{Port}$$

where

PPort is the input average power
 VPort is the input voltage
 IPort is the input current, either DC or RMS

See the file P802p3at_sub_33p3p5p2.FM supplied with comment file for full formatting example.

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Proposed Response Response Status

Cl 00 SC P L # 228

Law, David 3Com

Comment Type ER Comment Status D

Something seems to have gone wrong with the fonts throughout the draft. The font used for headers should be Arial and for text Times New Roman. For special symbols see the latest special symbols table.

SuggestedRemedy

Use correct fonts.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

David to help editor set correct fonts.

Cl 33 SC 2 P19 L31 # 229

Law, David 3Com

Comment Type T Comment Status X

It is not correct to state that all PSEs have to classify the PD. A Type 1 PD can still, optimally, choose not to do this.

SuggestedRemedy

Change '.. classify the PD ..' to read '.. optionally classify the PD ..'.

Proposed Response Response Status

Cl 33 SC 2.1 P5 L1 # 230

Law, David 3Com

Comment Type T Comment Status X

The drawing of the PD is not correct as it doesn't show that all PDs must be capable of accepting power on both Alternative A and Alternative B.

SuggestedRemedy

Replace PD in figure with the one in the file P802p3at_fig_33d4a.FM supplied with comment file.

Proposed Response Response Status W

find other comments like this

Cl 33 SC 2.7.1 P33 L16 # 231

Law, David 3Com

Comment Type T Comment Status X

There are Type 1 and Type 2 PSEs, Type 1 and Type 2 PDs, and there is Type 1 and Type 2 hardware classification. It is therefore unclear what the Type values in the 'Usage' column in Table 33-3 is in reference to. It looks like it is meant to refer to PSE type but Type 1 isn't correct in 0 to 3 as classification is optional, it is also silent on class 4 for a Type 1.

SuggestedRemedy

Consider removing 'Usage' column.

Proposed Response Response Status

Cl 33 SC 2.3.6 P27 L41 # 232

Law, David 3Com

Comment Type T Comment Status X

See previous comment on default behaviour, a Type 1 should default to Class 0, a Type 2 to Class 4.

SuggestedRemedy

Change the text 'Class 0 is returned if an invalid classification signature is detected.' to read 'If an invalid classification signature is detected Class 0 is returned by a Type 1 PSE, Class 4 is returned by a Type 2 PSE.'

Proposed Response Response Status

Cl 33 SC 2.7.2a P34 L35 # 233

Law, David 3Com

Comment Type T Comment Status X

Make it clear what classification a PD should have from a single class even that returns Class 4. The text currently says it should be treated as a Type 1 PD, but doesn't say of what class. I believe the PD should be classified as Class 0.

SuggestedRemedy

Suggest that the text 'In this case, the Type 2 PSE shall assume it is powering a Type 1 PD until successful link layer classification is performed.' be changed to read 'In this case, the Type 2 PSE shall classify the PD as Class 1'.

Proposed Response Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.1 P19 L1 # 234
 Law, David 3Com

Comment Type TR Comment Status X

The text states that 'Midspan PSEs shall use Alternative B when used in 10BASE-T or 100BASE-TX systems'. It then states that 'Midspan PSEs may support either Alternative A or B, or both when used in 1000BASE-T systems'. There is no definition of what a 10BASE-T, 100BASE-T or 1000BASE-T 'system' is, so in the following I will assume that simply it means that the link is operating with that type of PHY at each end.

Many ports these days are 10/100/1000BASE-T capable. Based on this, take the case of a 10/100/1000BASE-T non-PSE switch port that is connected to a Midspan. The Midspan connected to this port will have to be a 1000BASE-T capable Midspan or the link will never be able to operate at 1000BASE-T. The port however may not actually be operating at 1000BASE-T so this would seem to force the Midspan to be Alternative B to meet the mandatory requirement for 10BASE-T and 100BASE-T operation. In fact unless you can guarantee that the link the 1000BASE-T Midspan is connected in will only ever operate at 1000BASE-T, which I do not believe the Midspan has any way to force, the Midspan will have to be Alternative B.

The option of being able to build an Alternative A Midspan therefore seem unusable.

SuggestedRemedy

Either (i) mandate that all Midspans have to be Alternative B or (ii) allow 10BASE-T and 100BASE-T Midspans to be Alternative A as well as Alternative B. I suggest the second option on the basis that if it has been proved that 1000BASE-T Alternative A Midspans can be built while maintaining the link segment requirements they should be permitted for 10BASE-T and 100BASE-T operation as well. If this has not been proved then my first option has to be used.

Proposed Response Response Status

Cl 33 SC 1.3 P3 L6 # 235
 Law, David 3Com

Comment Type TR Comment Status X

Figure 33-3 needs updated, it is only applicable to 10BASE-T and 100BASE-T operation as it shows two pairs of the four pairs being source from the PHY and two pairs of the four pairs being sourced by the PSE. In the case of 1000BASE-T four pairs are sourced by the PHY.

In addition the figure title states that it illustrates 'relationship to the physical interface circuitry' yet the physical interface circuitry its shown.

SuggestedRemedy

See suggested new figure in FrameMaker file P802p3at_fig_33d3.FM supplied with comment file.

Proposed Response Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.2a P24 L3 # 236
 Law, David 3Com

Comment Type TR Comment Status X

The text states that 'Type 1 PSEs may optionally implement Type 1 hardware classification.' It then states that 'This limits the minimum power the Type 1 PSE may expect to provide to a PD 15.4 W'.

[a] I don't understand the 'This limits ..' text, I didn't think it was the classification that limits the power, I thought that was only optionally to do so based on classification, if calcification took place, which in itself is also optional for a Type 1 PSE (see 33.2.8.6). The limit of 15.4W is just simply the limit for a Type 1 PSE.

[b] While I understand that the 15.4W is a minimum value for item 14 in Table 33-5, I believe here it is a maximum value. If you have a Type 1 PSE the maximum power you can expect to draw from it is 15.4W. If you try to draw more power the PSE is permitted to consider this an overcurrent condition (Table 33-5, item 8, ICUT overcurrent range, minimum 15400/Vport) and if so, after a delay of TOVLD would have to remove power.

[c] The power 15.4W isn't what a Type 1 PSE 'expect to provide to a PD', instead it is the power sourced at the PI of the PSE - a portion of this power is dissipated in the cabling and doesn't reach the PD.

[d] I believe similar comments to [a], [b] and [c] are also true for Type 2 PSEs.

[e] I'm not too sure if it is here that we should be defining what classification methods can be used. For example the current text doesn't actually say that Type 2 classification can't be used for a Type 1 PSE, only that Type 1 classification can optionally be used. Regardless the 'may' and 'shall' statements made here are a duplication of statements made in subclause 33.2.7 (page 32, lines 27 through 33) and so should not be included here.

[f] On a similar note the text says that a Type 2 PSE may optionally implement link layer classification, but is silent if a Type 1 PSE may do so. Since it is permitted I assume it can do so, I don't remember a motion prohibiting it. Again however any restrictions on the use of link layer classification belongs in subclause 33.2.7a 'Link layer classification'.

[g] I think the text 'Table 33-5 specifies the electrical characteristics of Type 1 and Type 2 PSEs. When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE.' should be moved to somewhere a lot closer to Table 33-5 to make sure it isn't missed.

[h] I don't believe that 'A Type 2 PSE satisfies all requirements of a Type 1 PSE, whereas a Type 1 PSE does not necessarily meet the requirements of a Type 2 PSE.'. One of the requirements of a Type 1 PSE is that it uses Type 1 classification if it uses any classification, a Type 2 PSE would not do that. Isn't the point actually that a Type 2 PSE can support all PDs that a Type 1 PSE supports whereas a Type 1 PSE may not be able to support all PDs a Type 2 PSE supports.

SuggestedRemedy

Suggest that:

[1] Duplicate requirements are removed so that subclause 33.2.2a reads:

33.2.2a PSE types

Two types of PSE are defined - Type 1 and Type 2.

Type 1 PSE:

A type of PSE that can supply a maximum of 15.4W at the PI.

Type 2 PSE:

A type of PSE that can supply a maximum of 36W at the PI.

Note - A Type 2 PSE can support all PDs that a Type 1 PSE supports whereas a Type 1 PSE may not be able to support all PDs a Type 2 PSE supports.

[2] The text 'When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the electrical requirements of a Type 1 PSE.' should be added to the end of the first paragraph of 33.2.8 'Power Supply output'.

Proposed Response

Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

CI 33 SC 2.7 P32 L25 # 237
 Law, David 3Com

Comment Type TR Comment Status X

[a] It is difficult to follow the various different types of classification we now have and there is no overall introduction to guide the reader to what options there are and what features each option provides. There should be a broad introduction to all types of classification, and introduction to each specific type of classification then finally the details of the operation.

[b] Subclause 33.2.7 PSE Hardware classification of PDs' currently states that 'A PSE may remove power to a PD that violates the maximum power required for its advertised class.' which implies this only applies to hardware classification and that if a PD violates the maximum power it advertised through Link Layer classification it isn't permitted to do this. I don't believe this is correct and it is just as valid to do this for Link Layer classification. This text should therefore be moved so that it applies to all classification methods. See also other comment on this text.

SuggestedRemedy

Suggest that:

[1] Subclause 33.2.7 become an introductory clause that reads:

33.2.7 PSE classification of PDs

The ability of a PSE to classify a PD allows features such as load management to be implemented. There are two forms of classification, hardware classification and optional link layer classification. Hardware classification allows a PSE to classify a PD into one of a limited number of granular classes, this classification occurs once after a PSE successfully completes detection of a PD. Link layer classification allows a more granular classification that the initial hardware classification, this classification occurs continuously and provides the ability for the PD classification to change.

A PSE may remove power from a PD that violates the maximum power it has advertised it requires. This maximum power is initially derived from the advertised class during hardware classification and then, if implemented, subsequently updated by link layer classification.

[2] A new subclause 33.2.7.1a be inserted that reads:

33.2.7.1 PSE hardware classification of PDs

There are two types of hardware classification dependant of the PSE type, Type 1 hardware classification and Type 2 hardware classification.

A Type 1 PSE may optionally perform hardware classification. If a Type 1 PSE does perform hardware classification it shall use Type 1 hardware classification (see 33.2.7.2). If a Type 1 PSE does not classify the PD using hardware classification, then the Type 1 PSE shall assign the PD to Class 0.

A Type 2 PSE shall perform hardware classification and shall use Type 2 hardware

classification (see 33.2.7.2a). This is to ensure that a Type 2 PSE implementing only hardware classification can indicate its presence and identify the Type 2 PD's power requirements.

A successful hardware classification of a PD requires:

- a) Successful PD detection, and subsequently,
- b) Successful Type 1 or Type 2 Class 0-4 hardware classification.

The PSE hardware classification circuit should have adequate stability to prevent oscillation when connected to a PD.

Proposed Response Response Status O

CI 33 SC 2.7 P32 L28 # 238
 Law, David 3Com

Comment Type TR Comment Status X

On the long standing basis that we should be conservative on what we send but liberal on what we receive I think we should state what should be done if classification fails for some reason for both a Type 1 PSE and a Type 2 PSE.

In IEEE Std 802.3-2005 we state 'If a PSE successfully completes detection of a PD, and the PSE does not classify the PD in Class 1, 2, 3, or 4, then the PSE shall assign the PD to Class 0.' Now this text does not state the reason why the PSE does not classify the PD so this seems to apply to [a] a PSE that doesn't perform classification and [b] a PSE that does perform classification but when the classification cycle occurs the values return do not match a value. I believe this is confirmed by the State Diagram (figure 33-6) which states in the do_classification function that definition (subclause 33.2.3.6) that 'Class 0 is returned if an invalid classification signature is detected'.

One approach would seem to be to apply the same approach to IEEE P802.3at, if hardware classification fails regardless of Type treat the PD as a class 0. There is however one edge case if a Type 2 PD has a fault such that a PSE cannot detect it as a Type 2 yet it is still capable of detecting a Type 2 PSE. In this case the PSE would treat it as Class 0 and possibly limit it to 15.4W while the PD having detected a Type 2 PSE will operate as if 36W is available. Based on this I guess the default has to be Class 0 for Type 1 and Class 4 for a Type 2.

SuggestedRemedy

Change the text to read 'If a PSE successfully completes detection of a PD, but the PSE fails to classify the PD as a Class 1, 2, 3, or 4 using hardware classification, then the a Type 1 PSE shall assign the PD to Class 0 a Type 2 PSE shall assign the PD to be a Class 4.'

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.7a.2 P37 L9 # 239
 Law, David 3Com

Comment Type TR Comment Status X

Subclause 33.2.7.2a Type 2 hardware classification permits a Type 2 PSE to perform a single classification if it supports link layer classification. It however then requires that a PD that is classified as Class 4 is treated as a Type 1 PD until link layer classification is performed. I assume the link layer classification is then allowed to increase the power up to the Type 2 PD levels.

Based on the above, if a communications failure causes the PSE to revert to the initial hardware classification, in this case a PD that has increase its power through link layer classification it would have its power allocation cut back in the PSE to the Type 1 maximum. Since the PD may have no idea this is happening it may continue to draw the additional power it though it still had allocated - this in turn could cause the PSE to shut off the PD since it is now exceeding its 'requested' power.

SuggestedRemedy

Change the text so that in event of loss of communications the allocated power will remain at whatever level the last link layer classification was.

Proposed Response Response Status O

Cl 33 SC 2.7.2 P17 L37 # 240
 Darshan, Yair Microsemi Corporation

Comment Type E Comment Status X

33.2.7.2a appears twice. ("Insert sections 33.2.7.2a, 33.2.7a; Table 33'4a:")

SuggestedRemedy

Editor to clarify

Proposed Response Response Status O

Cl 33 SC 2.8 P23 L50 # 241
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X

Table 33-5 item 8:
 Replace TBD with number.

SuggestedRemedy

$I_{cut_max} = 0.72A * 0.4A / 0.35A = 0.823A$ (in order to keep the same 802.3af ratio)

In addition, we need to scan the draft and use the same term Icut instead Iovld or vise versa. (Icut is Iovld)

Proposed Response Response Status O

Cl 33 SC 2.8 P24 L11 # 242
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X

Table 33-5 item 11.

Type 1 and Type 2 PSEs may have different TLIM_MIN and TLIM_MAX.

SuggestedRemedy

Split item 11 to type 1 and type 2 PSE.
 Updated numbers/curves will be supplied by the Vport ad hoc.

Proposed Response Response Status O

Cl 33 SC 2.8 P24 L13 # 243
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X

Table 33-5 item 12:
 Add test condition for Tr. It is not clear how to measure it as PSE alone.

SuggestedRemedy

To add test condition: "At minimum capacitive load of $I_{port_transien} * 15\text{usec} / 44V = 5.3\mu\text{F}$ $I_{port_transient} = 20A$ at the time range of 15usec. value came from the Vport ad hoc in earlier version, it might be changed to 50A which will result with larger minimum test capacitance. (Total PSE and PD Capacitance is required for the test).

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.8 P24 L33 # 244
 Darshan, Yair Microsemi Corporation
 Comment Type T Comment Status X
 Table 33-5 item 20:
 Different classification max time for type 1 and type 2 PSEs
 SuggestedRemedy
 Split item 20 to type 1 and type 2 PSEs
 Proposed Response Response Status O

Cl 33 SC 2.8.5 P26 L4 # 245
 Darshan, Yair Microsemi Corporation
 Comment Type T Comment Status X
 There is no definition of the requirements for ILIM between 0V to 10V.
 The proposal below was part of maintenance request 1162.
 SuggestedRemedy
 Change 33.2.8.5 item e from:
 e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA.
 See Figures 33C.4, 33C.6.
 To:
 e) During startup, for PI voltages between 10V and 30V, the minimum IINRUSH requirement is 60mA.
 During startup, for PI voltages between 0V and 10V, the max IINRUSH requirement is as specified by Table 33-5, item 10.
 See Figures 33C.4, 33C.6 and 33C.6.1.
 Proposed Response Response Status O

Cl 33C SC 1.7 P85 L6 # 246
 Darshan, Yair Microsemi Corporation
 Comment Type T Comment Status X
 We need to update this part for supporting tests for foldback current limit tests in more general way as done for the startup mode.
 (Comments from the maintenance group per MR # 1162.)

SuggestedRemedy
 Change the following in Annex 33C clause 33C.1.7:
 1. In Figure 33C.7 upper part: add a box labeled "variable load" in series to S1
 2. Replace test procedure PSE-7 item 3 text from:
 ""3) Verify that Iport is within the limits shown in Figure 33C.4""
 With ""3) Change the variable load in order to verify that Iport is within the limits of Figures 33C.4 and 33C.6.1. Please note that the variable load type (resistive, constant voltage or other) depends on different PSE implementations.""
 Clause 33C.1.4 PSE-4:
 Change item 3 in PSE 4 from ""Verify that ..in Figure 33C.4"" to ""Verify that ..in Figures 33C.4 and 33C.6.1""
 Change the note in the last two sentences in clause 33C.1.4 after item 6 in PSE-4:
 From: ""Test setupÓÓÓÓexpected per Figure 33C.4.""
 To: ""Test setupÓÓÓÓexpected per Figure 33C.4 and 33C.6.1.""

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.3.4 P9 L24 # 247
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 The definition for ""error_condition"" is not satisfied.

SuggestedRemedy

Change definition from:
 ""A variable indicating the status of implementation-specific fault conditions that require the PSE not to source power..""

To
 ""A variable indicating the status of implementation-specific fault conditions or other system faults that prevents meeting Table 33-5 that require the PSE not to source power.."":

Proposed Response Response Status O

Cl 33 SC 2.7.2 P18 L44 # 248
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 ""Undefined"" is not clear enough in this case.

SuggestedRemedy

To add ..""and subject to system decision""

Proposed Response Response Status O

Cl 33 SC 2.7.2 P18 L23 # 249
 Darshan, Yair Microsemi Corporation

Comment Type T Comment Status X
 Potential problem:
 When PSE is at Reset range especial when it is in Vrest_high then at 31V indication data is lost since PD has not started yet and captured the PSE type.

SuggestedRemedy

If PSE successfully done with the 2 fingers classification it will stay at 7V min until power up and steady state operation.
 Reset will hapen only after PSE issued Vreset_low.

Proposed Response Response Status O

Cl 33 SC 2.8 P24 L10 # 250
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X
 Table 33-5 item 10:
 Replace TBDs with numberS.

SuggestedRemedy

ILIM_MAX for the long term horizontal curve segment of the short circuit curve:

ILIM_MAX=0.72*0.45A/0.35A=0.925. Abit higher value is possible per Vport_ad hoc findings.

ILIM_MIN=ICUT_MAX + margin to allow charging Cpd when PSE generates dv/dt AND PD load is at Icut_max.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

CI 33 SC 2.8.8 P26 L35 # 251
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

The specification allows foldback current limit implementations in startup mode as defined by 33.2.8.5.
 MR request 1162 material and maintenance group attached drawing shows that the intent of the specification was to allow the same implementations during short circuit condition as well. However items d and e of 33.2.8.5 was not copied to 33.2.8.8 as should have done.

SuggestedRemedy

1. Move drawing 33C.4 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
2. Move drawing 33C.6 or its updated version as a result of the Vport ad-hoc work to the normative section as it was in the early drafts of the IEEE802.3af.
3. Add drawing 33C.6.1 to 33.2.8.8

4. Replace the following text:

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:

- a) Max value of the PI current during short circuit condition.
 - b) Max value applies for any DC input voltage up to the maximum voltage as specified in item 1 of Table 33-5.
 - c) Measurement to be taken after 1ms to ignore initial transients.
- See Figure 33C.4 and Figure 33C.6.

With the proposed text: (items d and e are additions to previous text)

The power shall be removed from the PI within TLIM, as specified in Table 33-5, under the following conditions:

- a) Max value of the PI current during short circuit condition.
 - b) Max value applies for any DC output voltage up to the maximum voltage as specified in item 1 of Table 33-5.
 - c) Measurement to be taken after 1ms to ignore initial transients.
 - d) During short circuit condition, for PI voltages above 30V, the ILIM requirement is as specified in Table 33-5, item 10.
 - e) During short circuit condition, for PI voltages between 10V and 30V, the minimum ILIM requirement is 60mA as long as system decides to keep the port ON, and the maximum requirement is as specified in Table 33-5, item 10.
- During short circuit condition, for PI voltages between 0V and 10V, the minimum ILIM requirement is 0mA and the maximum requirement is as specified in Table 33-5, item 10.
 See Figures 33C.4, 33C.6 and 33C.6.1."

5. Add the following notes after 33.2.8.8-e:

Notes:

1. Items d and e in 33.2.8.8 allows implementation of foldback current limit type in which ILIM requirement is decreased if Vport is

decreased below pre specified value.

2. Short circuit condition definition in IEEE802.3af is a case in which the port voltages is dropped below normal operating voltages as defined by table 33-5 items 1 and 2 due too load fault conditions that exceeds table 33-5 item 8""

6. Add the following note text after 33.2.8.5-e:

Note: items d and e in 33.2.8.5 allows implementation of foldback current limit type in which linrush requirement is decreased if Vport is decreased below pre specified value.

Foldback current limit is optional in the standard.

IMPACT ON EXISTING NETWORKS:

No impact. It is optional.

Proposed Response Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.8.9 P26 L39 # 252
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

33.2.8.9 text is true for the case that system (PSE and PD) are within their normal voltage operating range however it is not clear from the text. It is clear from figure 33C.4 and 33C.6 which are located in the informative section.

SuggestedRemedy

Replace 33.2.8.9 text :

""If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33'5. See Figure 33C.4 and Figure 33C.6.""

With:

For PI voltages above Vport_lim as defined by table 33-5 item TBD, If a short circuit condition is detected, power removal from the PI shall begin within TLIM and be complete by TOff, as specified in Table 33'5. See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1""

For PI voltages below Vport_lim as defined by table 33-5 item TBD, If a short circuit condition is detected, power removal from the PI may begin at any time of t<TLIM and be complete by TOff, as specified in Table 33'5. See Figure 33C.4, Figure 33C.6. and Figure 33C.6.1""

Proposed Response Response Status

Cl 33 SC 2.5 P26 L2 # 253
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

The 30V value in 33.2.5 items d) and e) and other related parts of this specification can be modify for enhanced flexibility.

SuggestedRemedy

Suggested that Vport_lim will (as defined in other comments) be changed from Vport_lim=30V to:

Option 1 (from Vpd_OFF starting point, the preffered option):

Vport_LIM at PSE side for Type 1 PSE: 30V minimum, 38V max.
 Vport_LIM at PSE side for Type 2 PSE: 30V minimum, 40.28V max.

Rational

Vpse = Vpd + Cable Voltage loss
 PD is definitely OFF at 30V.
 Cable loss is 0.4*20R=8V for Type 1.
 Cable loss is 0.72*0.4A/0.35A*12.5=10.28V for Type 2.

Option 2(from minimum PD operating voltage starting point):

Vport_LIM at PSE side for Type 1 PSE: 30V minimum, <44V max.
 Vport_LIM at PSE side for Type 2 PSE: 30V minimum, 46.28V max.
 (Taking in account that port must be on for voltage transient duration of up to 250us for 7% below 50V)

Rational

Vpse = Vpd + Cable Voltage Drop
 PD must work at 36V.
 Cable loss is 0.4*20R=8V for Type 1.
 Cable loss is 0.72*0.4A/0.35A*12.5=10.28V for Type 2.

Proposed Response Response Status

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

CI 33 SC Table 33-12 P40 L1732 # 254
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X
 Table 33-12 items 1 and 4: Need to update numbers

SuggestedRemedy

Item 1: Type 2 PD minimum voltage is 50v-12.5*0.72*0.4/0.35=39.71V and not 40V.

Item 4: Peak operating current at class 4 for type 2 PD:

Considerations:

- For maximum PD available power).
 The need is with high probability.

$0.72A * 0.4 / 0.35 = 0.823A$. (Same I_{cut}/I_{port} ratio as in 802.3af)

Regarding the issue of supporting PSE current transient due to dv/dt simultaneously with PD peak current=823mA when PSE is using constant current limit near I_{cut_max} so net charging current is zero, the following options are suggested:

Option 1:

To define that $PSE\ ILIM_MIN = PSE'S\ I_{cut_max} + Margin$.
 The margin is the current required to charge C_{pd} (<50mA).

Option 2:

The support of PSE dv/dt is implementation specific.
 Rational:

1. It is enough to define that PSE is required to support current transients due to PSE dv/dt up to 7V at a slew rate of TBD. At this point it is depended only at the PSE how to implement this support. The PD is not a player that need to be defined. It is already defined by $C_{pd}=180\mu F$ border line.

2. If PSE choose to implement energy based current limit, then it will work within the 2A peak and 3msec time as suggested by the V_{port_ad} hoc.

3. If PSE choose to use constant current limit, it will choose the right ILIM and TLIM pairs to support this scenario.

4. There is no issue with PD load transient current due to the fact that per the concept of type 1 PD which is suggested for type 2 PD, the max peak current at the PD is I_{cut_max} and it is limited to 50msec, 5% duty cycle max.

5. There is no added cost as was proven in 802.3af:

5.1 The max. average current is always 720mA (350mA in 802.3af)

5.2 The max. RMS current is 720mA rms. (350mA in 802.3af)

Hence no additional resistive loss in the system.

5.3 As a result the total average power is always 29.5W max. (12.95W in 802.3af)

5.3.1 The specification is explicitly define that the total PD input power shall not exceed P_{port_max} 12.95/(29.5W) average over 1sec.

Proposed Response Response Status O

CI 33 SC 2.3.4 P9 L22 # 255
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

During ""Short Circuit"" Condition i.e. when PSE and PD are no longer at their operating voltage range, there is no technical need to keep PSE port on for TLIM.

It creates many problems such:

- Prevents meeting item 21 in table 33-5, Ted (Time delay between consecutive start ups).
- Excessive heat.

See more details in MR #1167.

SuggestedRemedy

To allow the PSE to turn the port to OFF mode when $V_{port} <$ at any $t < TLIM_MIN$.

Remedy steps:

1) Add new variable option_vport30 to 33.2.3.4. It will be an optional variable.

option_vport30

This variable is indicating If PSE port voltage is out of operating range during normal operating mode.

Values:

False: V_{port} is above $V_{port_LIM} = TBD1$ for Type 1 PSE, TBD2 for type 2 PSE
 True: V_{port} is below $V_{port_LIM} = TBD1$ for Type 1 PSE, TBD2 for type 2 PSE

2) Add to table 33-5 new parameter V_{port_LIM} for type 1 and type 2 PSE.

Type 1 PSE values: 30V min TBD1 max.

Type 2 PSE values: 30V min TBD2 max.

3) Add the following text to 33.2.8.8 after item e. Items d and e are reserved for maintenance request 1162).

""f) During short circuit condition, for PI voltages below V_{port_LIM} the PSE may turn to IDLE state at any time $t < TLIM_MIN$. ""

4) Change state diagram (figure 33-6) per the attached drawing.

Using this optional variable in the state diagram will fix the problem by

changing the inputs to ERROR_DELAY_SHORT state

from: $tlim_timer_done$

to: $!lim_timer_done + !lim_timer_done * option_vport30 * power_applied$)

Effect on legacy equipment: NONE since the variable is optional.

Proposed Response Response Status O

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

SORT ORDER: Comment ID

Comment ID # 255

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IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2.7.2 P18 L39 # 256
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

Replace ""shall"" with ""may""

SuggestedRemedy

It should be ""may ommit"" not ""shall"" to simplify classification circuits of type 2. (in any case if PD advertize class 0-3 then PD can't take more then advertized current although PSE is type 2 i.e. all parties PSE and PDs knows all required info.)

Proposed Response Response Status O

Cl 33 SC 2.8 P23 L22 # 257
 Darshan, Yair Microsemi Corporation

Comment Type TR Comment Status X

Draft D0.2: Table 33-5 item 2b.

We had an error in the ""transient voltage"" motion.
 We can't allow voltage above 60Vp as indicated by:
 1) SELV definitions
 2) Table 33-6 item 3b

See additional data in attached presentation.

SuggestedRemedy

Delete 33-5 item 2b.
 Correct last motion as poposed by Vport_ad hoc at the last phone conference.

Proposed Response Response Status O

Cl 33 SC 33.2.9 P43 L20 # 258
 Law, David 3Com

Comment Type T Comment Status X

A Type 2 PSE has to provide hardware classification (see 33.2.7). Due to this the only case where hardware classification will not occur is a Type 1 PSE where hardware classification is optional.

SuggestedRemedy

Change the text '.. a PSE does not provide either of the hardware classification functions specified in ..' to read '.. a Type 1 PSE does not provide the optional Type 1 hardware classification specified in ..'.

Proposed Response Response Status O

Cl 33 SC 33.3.4.2 P53 L14 # 259
 Law, David 3Com

Comment Type T Comment Status X

There are actually two types of classification. [1] A PSE's classification of a PD. [2] A PD's classification of the PSE. The text seems to call all this PD hardware classification and while it is that mechanism that is used by the PD to classify the PSE I think we need to make that distinction clear in the text. Does the text 'Once a PD has been powered by a Type 2 PSE' imply that the PD has to detect that the current sourced by the PSE has exceeded the maximum for a Type 1 PSE - although even that doesn't guarantee it is Type 2 PSE power. The only real test that is available is that a Type 2 hardware classification or link layer classification has completed.

SuggestedRemedy

Perfrom the following change: [a] Delete the first sentence of the third paragraph of subclause 33.3.4.2. Text currently reads 'Until successful Type 2 hardware classification or link layer classification has completed, a Type 2 PD's PSE Type state variable is set to Type 1.'. [b] Delete subclause 33.3.4.2.2. [c] Insert new subclause 33.3.4a, renumber as necessary. The content of this new subclause should cover the areas in [a] and [b] as well as clarify the text. 33.3.4a PSE type classification A Type 2 PD shall classify the PSE Type as either Type 1 or Type 2. The default value of PSE Type shall be Type 1. After a successful Type 2 hardware classification or link layer classification has completed the PSE Type shall be set to Type 2. The PD shall reset the PSE Type to Type 1 when the voltage at the PI is less than or equal to VReset_lo max. Once a Type 2 hardware classification or link layer classification has completed a Type 2 PD shall reset the PSE Type to Type 1 if the voltage at the PI is less than or equal to VReset_hi min.

Proposed Response Response Status O

Cl 33 SC 33.3.4a P53 L52 # 260
 Law, David 3Com

Comment Type T Comment Status X

What about Type 1 PDs - I see no reason what they shouldn't also optionally support link layer classification - if for example they wish to support more guarantee power management. I however agree that a Type 1 PD that supports link layer management shall support TIA 1057.

SuggestedRemedy

Change the text 'A type 2 PD ..' to read 'Type 2 PDs, as well as Type 1 PDs that optionally implement link layer management, shall support ..'.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 33.2.9 P43 L26 # 261
 Law, David 3Com

Comment Type T Comment Status X

The text states that '.. and the mechanism for obtaining that additional information, is beyond the scope of this standard ..'. I do not believe that is true anymore due to the link layer classification protocol.

SuggestedRemedy

Reword to acknowledge link layer classification.

Proposed Response Response Status O

Cl 33 SC 33.3.1 P47 L41 # 262
 Law, David 3Com

Comment Type TR Comment Status X

I do not believe there has been any vote to permit powering a PD simultaneously through Mode A and Mode B.

SuggestedRemedy

Removed the change and restore the text to read 'specifically not allowed by' until a vote has been taken to make this change.

Proposed Response Response Status O

Cl 33 SC 33.4.1 P60 L4 # 263
 Law, David 3Com

Comment Type TR Comment Status X

Subclause 33.4.1 and its subclauses do not contain the updated text from IEEE Std 802.3-2005/Cor1-2006 DTE Power via MDI Isolation corrigendum.

SuggestedRemedy

Update this subclause with the text from IEEE Std 802.3-2005/Cor1-2006.

Proposed Response Response Status O

Cl 33 SC 3.1 P31 L41 # 264
 McCormack, Michael Texas Instruments

Comment Type TR Comment Status X

The struck through and replacement text was not agreed by the committee in a vote. This is a major issue for cost and complexity of future PDs. There are numerous IP claims against four pair where none of the filing / patent holders have disclosed terms or promised no enforcement.

SuggestedRemedy

Remove the new text, replace the original.

Proposed Response Response Status O

Cl 33 SC 2.1 P6 L10 # 265
 McCormack, Michael Texas Instruments

Comment Type E Comment Status X

Both drawing of Figure 33-4a show transformers while other DC blocking yet AC blocking technologies may be suitable.

SuggestedRemedy

Replace windings with some form of black box which indicates DC blocking.

Proposed Response Response Status O

Cl 33 SC 2.3.1 P8 L30 # 266
 McCormack, Michael Texas Instruments

Comment Type E Comment Status X

The word "applicable" is vague

SuggestedRemedy

Strike the word, the tables are clear on the different types of PSEs.

Proposed Response Response Status O

IEEE P802.3at D0.2 DTE Power via MDI Enhancements comments

Cl 33 SC 2 P3 L31 # 267
 McCormack, Michael Texas Instruments

Comment Type **T** Comment Status **X**

The word "optionally" can not be stricken, there are legacy PSEs that will not classify.

SuggestedRemedy
 Restore "optionally"

Proposed Response Response Status **O**

Cl 33 SC 2.2 P7 L50 # 268
 McCormack, Michael Texas Instruments

Comment Type **TR** Comment Status **X**

The sentence prohibiting four pair has been struck trough. I do not recall a vote to make this change. This is a major issue for compatibility and cost to the end customers. There are numerous IP claims against four pair where none of the filing / patent holders have disclosed terms or promised no enforcement.

SuggestedRemedy
 Replace the prohibition

Proposed Response Response Status **O**

Cl 33 SC 2.2a P8 L11 # 269
 McCormack, Michael Texas Instruments

Comment Type **TR** Comment Status **X**

I do not beleive that Type 2 PSEs are required to support Type 2 hardware classifications. I beleive we ahve previosuly voted that the type of classification for Endspan PSEs is a choice of hardware or Layer 2.

SuggestedRemedy
 Replace the first sentence with: "Type 2 PSEs shall implement classification. Type 2 PSEs may optionally implement Type 2 hardware classisification."

Proposed Response Response Status **O**