33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

33.2 Power sourcing equipment

33.3 Powered devices

33.3.1 PD state diagram

33.4 Additional electrical specifications

33.5 Environmental

33.6 Management function requirements

~~Management of the PSE is optional. If the PSE is instantiated in the same physical package as a PHY and a Clause 22 MII or a Clause 35 GMII is physically implemented, then management access shall be via the MII Management interface. Where no physical embodiment of the MII or GMII exists and management is supported, equivalent management capability shall be provided.~~

Management of the PSE and PD is optional. If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO) then the management access shall use the PSE register definitions shown in 33.6.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30.

Additional control and classification functions are supported using management frames. These management frames are defined using IEEE 802.1AB protocol (LLDP). PDs that require more than 12.95W shall support control and classification using management frames, these functions are optional for all other devices. The management control frame operation is described in 33.6.2.

33.6.1 PSE registers

A PSE shall use register address 11 for its control and register address 12 for its status functions. The full set of management registers is listed in Table 22–6.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.6.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–1. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 33–1—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:~~4~~5	Reserved	Ignore when read	RO
11.4	Enable 2 stage classification	1 = 2 stage classification enabled 0 = 2 stage classification disabled	R/W
11.3:2	Pair Control	(11.3) (11.2) 1 1 = Reserved 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

33.6.1.1.1 Reserved bits (11.15:~~4~~5)

Bits 11.15:~~4~~5 are reserved for future standardization. They shall not be affected by writes and shall return a value of ‘0’ when read. To ensure compatibility with future use of reserved bits and registers, the management entity should write to reserved bits with a value of ‘0’ and ignore reserved bits on read.

33.6.1.1.2 Enable Two Stage Classification (11.4)

Bit 11.4 controls 2 stage classification as specified in 33.x.x. A PSE that indicates support for 2 stage classification in register 12.13 may also provide the option of disabling 2 stage classification through this bit. A PSE that does not support 2 stage classification shall ignore writes to this bit and shall return a value of ‘0’ when read. A PSE that does supports 2 stage classification but does not allow the function to be disabled shall ignore writes to this bit and shall return a value of ‘1’ when read.

The 2 stage classification function shall be enabled by setting bit 11.4 to logic one and disabled by setting bit 11.4 to logic zero.

33.6.1.1.3 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as ‘01’, bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as ‘10’, bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to ‘01’ shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to ‘10’ shall force the PSE to use only PSE Pinout Alternative B.

If bit 12.0 is ‘1’, writing to these register bits shall set mr_pse_alternative to the corresponding value: ‘01’ = A and ‘10’ = B. The combinations ‘00’ and ‘11’ for bits 11.3:2 are reserved and will never be assigned.

Reading bits 11.3:2 will return an unambiguous result of ‘01’ or ‘10’ that may be used to determine the presence of the PSE Control register.

33.6.1.1.4 PSE enable (11.1:0)

The PSE function shall be disabled by setting bits 11.1 to logic zero and 11.0 to logic zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a logic zero and 11.0 to a logic one. When bit 11.1 is a logic one, and bit 11.0 is a logic zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

Writing to these register bits shall set mr_pse_enable to the corresponding value: ‘00’ = disable, ‘01’ = enable and ‘10’ = force power. The combination ‘11’ for bits 11.1:0 has been reserved for future use.

CAUTION—Test mode may damage connected non-PD, legacy, twisted pair Ethernet devices, or other non-Ethernet devices, especially in split application wiring schemes.

33.6.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–2.

33.6.1.2.1 Reserved bits (12.15:~~13~~14)

Bits 12.15:~~13~~14 are reserved for future standardization. They shall not be affected by writes and shall return a value of ‘0’ when read. To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of ‘0’ and ignore reserved bits on read.

33.6.1.2.2 Two Stage Classification Supported(12.13)

When read as a logic one, bit 12.13 indicates the PSE supports 2 stage classification as defined in 33.x.x.x. When read as a logic zero, bit 12.13 indicates that the PSE lacks support for 2 stage classification. If supported, the function may be enabled or disabled through the Enable Two Stage Classification bit (11.4).

33.6.1.2.3 Power Denied (12.12)

When read as a logic one, bit 12.12 indicates that power has been denied. This bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) enters the state ‘POWER_DENIED’. The Power Denied bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.4 Valid Signature (12.11)

When read as a logic one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to ‘1’ when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.5 Invalid Signature (12.10)

When read as a logic one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) enters the state ‘SIGNATURE_INVALID’. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.6.1.

Table 33–2—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15:~~13~~14	Reserved	Ignore when read	RO
12.13	Two Stage Classification Supported	1 = PSE supports 2 stage classification 0 = PSE does not support 2 stage classification	RO
12.12	Power Denied	1 = Power has been denied 0 = Power has not been denied	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Implementation specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE Pinout Alternative fixed	RO

[a]RO = Read Only, LH = Latched High

33.6.1.2.6 Short Circuit (12.9)

When read as a logic one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) enters the state ‘ERROR_DELAY_SHORT’. The Short Circuit bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.7 Overload (12.8)

When read as a logic one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) enters the state ‘ERROR_DELAY_OVER’. The Overload bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.8 MPS Absent (12.7)

When read as a logic one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to ‘1’ when the PSE state diagram (Figure 33–6) transitions directly from the state POWER_ON to IDLE due to tpmdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.6.1.

33.6.1.2.9 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.6 and 33.2.7. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting Delivering power. The combinations ‘101’, ‘110’ and ‘111’ for bits 12.6:4 have been reserved for future use.

33.6.1.2.10 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as ‘000’, bits 12.3:1 indicate that the PSE state diagram (Figure 33–6) is in the state DISABLED. When read as ‘010’, bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as ‘011’, bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as ‘100’, bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as ‘101’, bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as ‘001’, bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations ‘111’ and ‘110’ for bits 12.3:1 have been reserved for future use.

33.6.1.2.11 Pair Control Ability (12.0)

When read as a logic one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a logic zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.6.2 Power Management Frames

Layer 2 frames are used to support extended control and status exchange between PSEs and PDs that support the function. These frames are based on the IEEE 802.1AB protocol (LLDP). Implementations that support power management using LLDP shall comply with all mandatory parts of IEEE 802.1AB. Implementations that support power management using LLDP shall support the minimum status Type, Length, Value (TLV) fields defined in 33.6.2.1. Implementations may also support the stateful control TLVs defined in 33.6.2.2 and additional status TLVs defined in 33.6.2.3.

The parameters used by the TLVs are defined in 33.6.3. Implementations that support stateful control TLVs shall use the control state machine is defined in 33.6.4. Sample frames that meet the format requirements are shown in Annex 33F (Informative).

A device implementing link layer classification shall send power management Protocol Data Units (PDUs) and process PDUs received from the remote device at least once every 30s. Each power management PDU shall contain the minimum status TLV. If the implementation supports dynamic power management using

stateful control TLVs then each power management PDU shall contain the stateful control TLV. Any power management PDU may contain the additional status TLV.

33.6.2.1 Minimum Status TLV definition

The minimum status TLV definition follows the format defined in ANSI/TIA-1057 for Media Endpoint Discovery. The fields of the minimum status TLV are shown in Table 33-x. Further details of this definition may

Table 33–3—Minimum Status TLV

Byte	Name	Description
1	TLV type	127 (7 bits) - organizationally specific type
2	TLV length	7 (9 bits) - length of information string
3-5	OUI	00-12-BB - TIA OUI
6	Subtype	04 - Power status subtype
7	Power type/source/priority	Bits 7:6 power type; Bits 5:4 power source; Bits 3:0 power priority
8-9	Power value	0 - 102.3 Watts

be found in ANSI/TIA-1057, Clause 10.2.4.

33.6.2.2 Stateful Control TLV definition

The stateful control TLV definition uses the organizationally specific type with the IEEE 802.3 OUI. The fields of the stateful control TLV are shown in Table 33-x. .

33.6.2.3 Additional Status TLV definition

The additional status TLV definition uses the organizationally specific type with the IEEE 802.3 OUI. The fields of the additional status TLV are shown in Table 33-x. .

33.6.3 TLV parameter definitions

The parameters called out in Tables 33-x, 33-x and 33-x are defined as follows:

33.6.3.1 Power type/source/priority

This consists of one eight bit field made up as follows:

Bits 7:6 power type: 11 = Reserved; 10 = Reserved; 01 = PD device; 00 = PSE device

Bits 5:4 power source (for PSE type devices): 11 = Reserved; 10 = Backup source, power conservation mode; 01 = Primary power source; 00 = Unknown

Bits 5:4 power source (for PD type devices): 11 = PSE and local; 10 = Local; 01 = PSE; 00 = Unknown

Table 33–4—Stateful Control TLV

Byte	Name	Description
1	TLV type	127 (7 bits) - organizationally specific type
2	TLV length	TBD (9 bits) - length of information string
3-5	OUI	00-12-0F - IEEE 802.3 OUI
6	Subtype	05 - PoE stateful control subtype
7	Requested power type/ source/priority	Defined in the same way as actual power mode, see 33.6.3.1
8-9	Requested power value	Defined in the same way as actual power mode, 33.6.3.2
10	Acknowledge	00 - not part of acknowledge cycle 01 - acknowledge 02 - non-acknowledge
	TBD	TBD

Table 33–5—Additional Status TLV

Byte	Name	Description
1	TLV type	127 (7 bits) - organizationally specific type
2	TLV length	TBD (9 bits) - length of information string
3-5	OUI	00-12-0F - IEEE 802.3 OUI
6	Subtype	06 - PoE additional status subtype
	TBD	TBD
	TBD	TBD

Bits 3:0 power priority: 0000 = unknown; 0001 = critical; 0010 = high; 0010 = low; 0011 - 1111 = reserved.

33.6.3.2 Power value

This is a sixteen bit number corresponding to the power requirement of the PD in its actual state or the power allocated by the PSE for the PD in its actual state. The power value is expressed in Watts, each bit representing 0.1W resulting in a range from 0.1W to 102.3W.

33.6.3.3 Acknowledge

This byte shall be set to 00 unless the state machine enters the REMOTE ACK or REMOTE NACK states. Following entry into the REMOTE ACK state the device shall send a PDU with this byte set to 01; following entry into the REMOTE NACK state the device shall send a PDU with this byte set to 02.

33.6.3.4 Other parameters TBD

Other parameters will be defined after adoption by the Task Force.

33.6.4 Power Control state machine

The general state change procedure is shown if FIG-nn (Insert diagram of operation).

33.6.4.1 State change procedure across a link

If the local device is in the running state and a remote device changes to the requesting state, the local device observes the remote device's requestedPower objects. The local device changes to an acknowledge state or a non-acknowledge state depending on acceptance of the remote device's requested change.

If the local device changes to the acknowledge state, it then changes its local copy of the remote device's actualPower object to match the remote device's requestedPower object. The local device then sends a PDU reflecting its new settings.

If the local device is in the running state and it wishes to change to a new power mode, it may only do so if the remote device's most recent PDU reported that the remote device is in the running state. To change to a new power mode, the local device sets its local requestedPower object and changes to the requesting state. The local device then sends a PDU reflecting its requested power mode.

If the remote device changes to the acknowledge state in response to the mode change request from the local device, the local device updates its local actual power objects and changes to the running state. The local device then sends a PDU reflecting its new settings.

If the remote device changes to the non-acknowledge state in response to the mode change request from the local device, the local device does not change its operating power mode and changes back to the running state. The local device then sends a PDU reflecting its return to the running state.

In the event of a PDU collision (e.g. the local device is in a requesting state and the remote device changes to a requesting state), the local device does not change its operating power mode. The local device instead changes back to the running state and sends a PDU reflecting its return to the running state. If the local device is a PSE it may restart the request to change after TBD, if the local device is a PD it may restart the request to change after TBD.

After powerup, the initial state of the local device uses the Type 1 or Type 2 hardware classification as the first actual power mode.

In the event of a loss of communication, the PD's reported Type 1 or Type 2 hardware classification has precedence. If the local device does not receive a PDU from the remote device for TBD, it assumes loss of communication and reverts to the reported Type 1 or Type 2 hardware classification.

State definitions require that each request must be acknowledged or denied before returning to running state. The requestor does not deassert the request until it receives an acknowledge or non-acknowledge. The partner responds to a request as soon as it is seen. The requestor may persist or vacillate after a non-acknowledge. To persist, it reasserts its request after a TBD delay. It may decide to not persist.

33.6.4.2 Local power control state machine.

33.6.4.3 The state machine shown in Fig-nn applies to PSE and PD devices that use stateful power management.

Initialize power mode: power type; source; priority initialize to preferred value. Power value initializes according to result of hardware classification.

Update power mode: power value; type; source; priority change to requested values (sent or received as appropriate).

Loss of communication: if no PDU is received for TBD, the state machine shall transition to the INITIALIZE state.

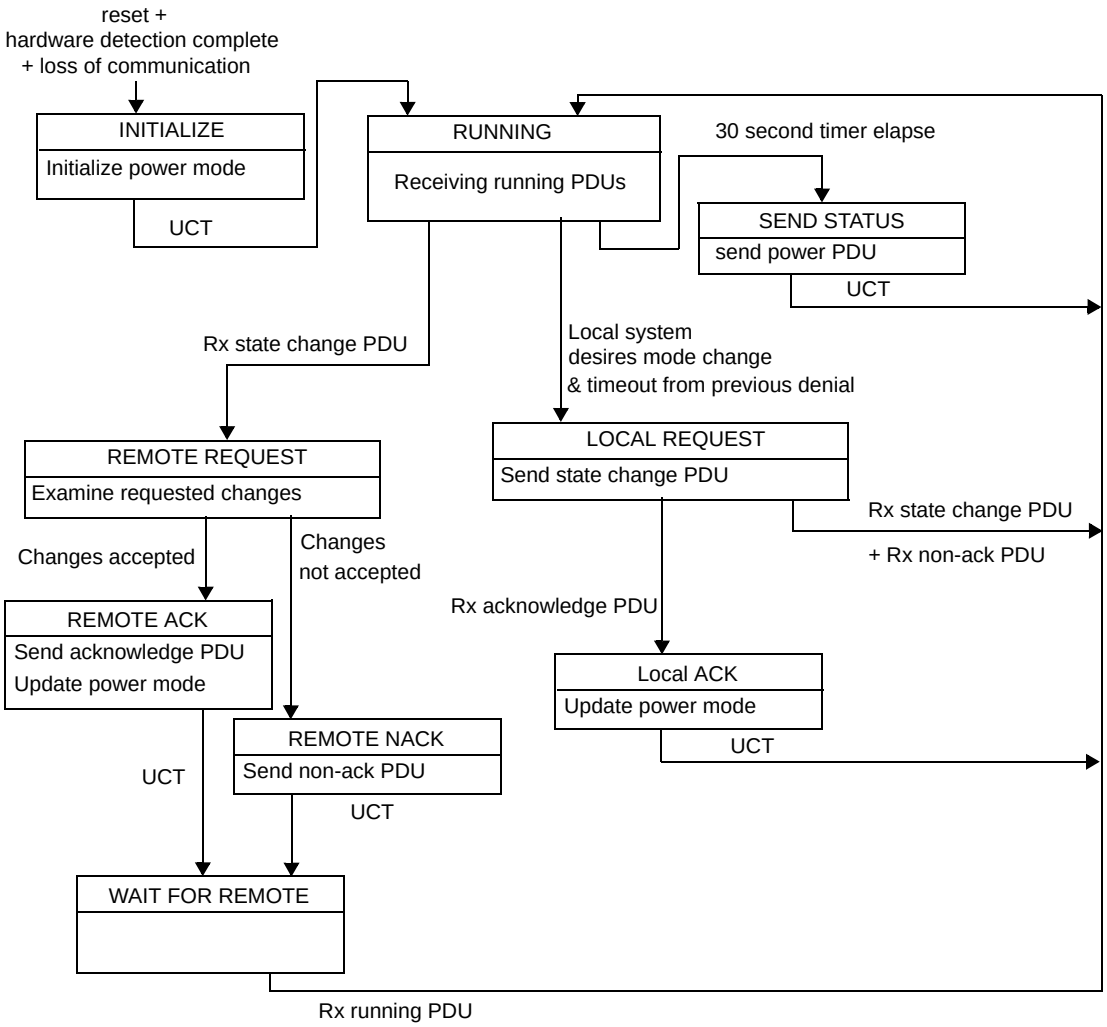

Figure 33–6—Power control state machine

33.6.4.4

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