Considerations on the Placement of Parity Blocks

Frank J. Effenberger
Raymond W.K. Leung
Dongyu Geng
Dongning Feng

Huawei Technologies Co. Ltd

FEC Requirements

- According to the survey made in May 2007 (3av_0705_parruck_1.pdf).
  - FEC redundancy should less than 15%.
  - FEC codeword size can be made between 2-4k bits, i.e. 30-60 blocks.

Number of Parity Blocks Required

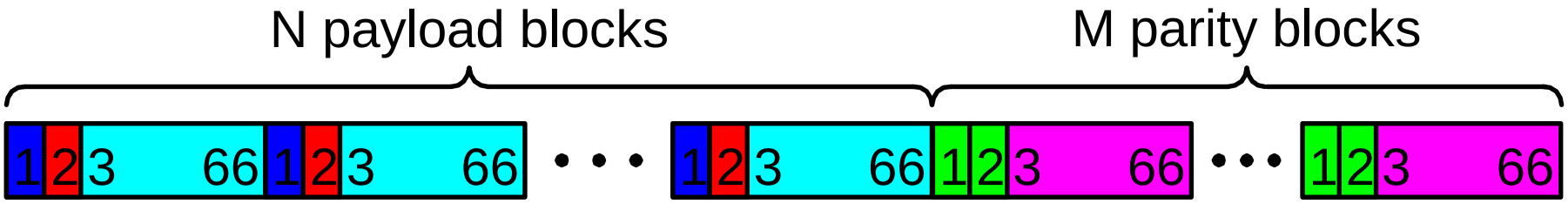
FEC Codeword Size (payload blocks + parity blocks)	Parity blocks		
	7% overhead	13% overhead	15% overhead
30	~ 2	~ 4	4 – 5
35	2 – 3	4 – 5	5 – 6
40	2 – 3	~ 5	~ 6
45	~ 3	~ 6	~ 7
50	3 – 4	6 – 7	7 – 8
55	~ 4	~ 7	8 – 9
60	~ 4	~ 8	~ 9

Number of Parity Blocks Required (cont.)

FEC Codeword Size (payload blocks + parity blocks)	FEC overhead (%)				
	3 Parity Blocks	4 Parity Blocks	5 Parity Blocks	6 Parity Blocks	7 Parity Blocks
30	**9.86%**	**13.16%**	16.45%	19.75%	23.06%
35	**8.45%**	**11.27%**	**14.10%**	16.92%	19.75%
40	**7.39%**	**9.86%**	**12.33%**	**14.80%**	17.28%
45	**6.57%**	**8.76%**	**10.96%**	**13.15%**	15.35%
50	**5.91%**	**7.89%**	**9.86%**	**11.84%**	**13.81%**
55	**5.38%**	**7.17%**	**8.96%**	**10.76%**	**12.56%**
60	**4.93%**	**6.57%**	**8.22%**	**9.86%**	**11.51%**

$$\text{FEC overhead}\,(\%) = \frac{\text{no. of parity block} \times 64}{\text{no. of payload block} \times 65 + \text{no. of parity block} \times 64} \times 100\%$$

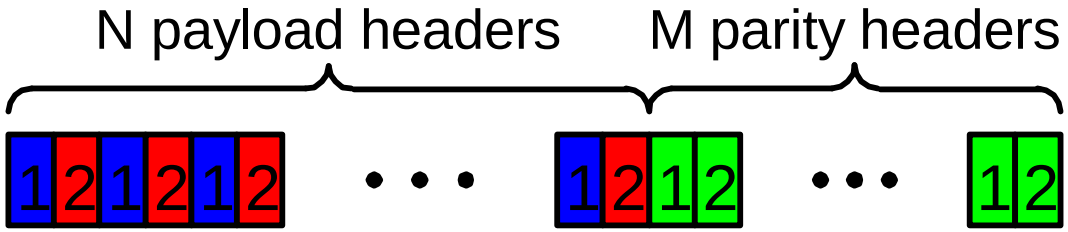
Frame Pattern



Sync header of payload block, either 01 or 10

Sync header of parity block, either 00 or 11

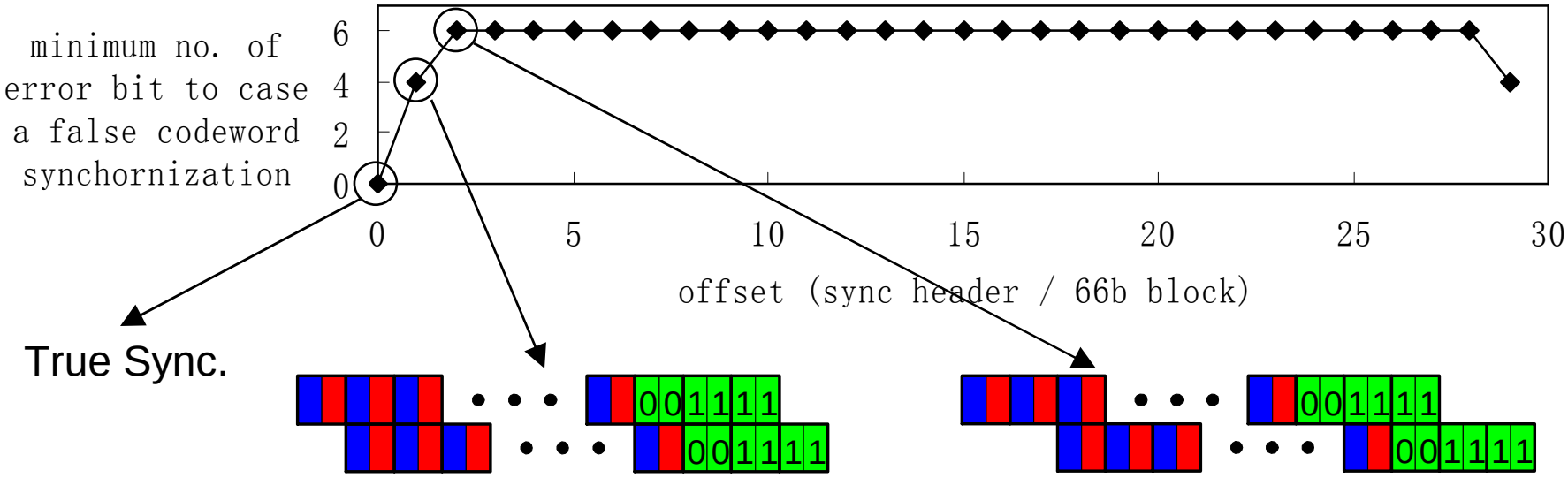
Assuming correct block alignment, we have



False Codeword Synchronization

Example 1:

Payload block N = 27; parity block M = 3; parity header pattern = {00, 11, 11}; and overhead = 9.86%.



min. no. of error bit required to case a false codeword sync.

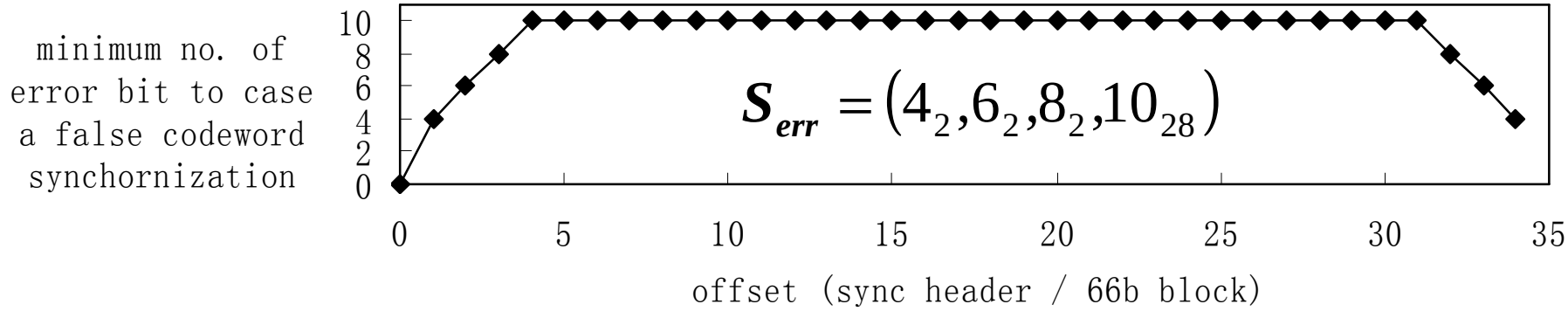
$$\text{Error Bit Spectrum } \boldsymbol{S}_{err} \equiv \left(\left(4 \right)_{\left(2 \right)}, 6_{\ 27} \right)$$

no. of event

False Codeword Synchronization (cont.)

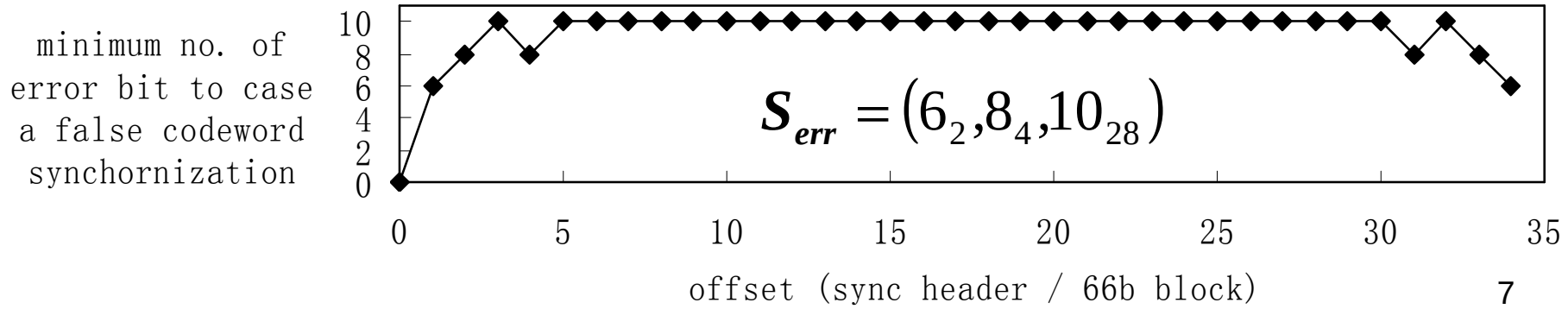
Example 2a:

Payload block N = 30; parity block M = 5; parity header pattern = {00, 11, 11, 11, 11}; and overhead = 14.10%.



Example 2b:

Payload block N = 30; parity block M = 5; parity header pattern = {00, 11, 11, 11, 00}; and overhead = 14.10%.



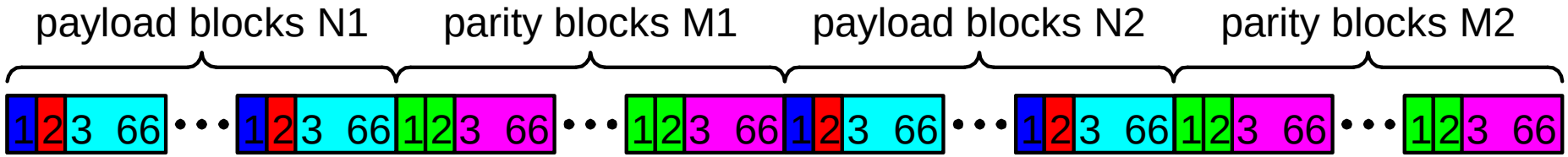
False Codeword Synchronization (cont.)

With payload block N = 30 and parity block M = 5, the following parity header patterns have the same error bit spectrum $\boldsymbol{S}_{err}$ = (6_2, 8_4, 10_{28}):

{ 11, 00, 11, 00, 00 }; { 00, 11, 11, 00, 00 }; { 11, 00, 00, 11, 00 }; { 11, 11, 00, 11, 00 }; { 00, 00, 11, 11, 00 }; { 11, 00, 11, 11, 00 }; { 00, 11, 11, 11, 00 }; { 11, 00, 00, 00, 11 }; { 00, 11, 00, 00, 11 }; { 11, 11, 00, 00, 11 }; { 00, 00, 11, 00, 11 }; { 00, 11, 11, 00, 11 }; { 11, 00, 00, 11, 11 }; and { 00, 11, 00, 11, 11 }.

The false codeword locking probability is dominated by the minimum value in $\boldsymbol{S}_{err}$ = (**6**$_2$, 8_4, 10_{28}) and the number of occurrence of this minimum value, i.e. $\boldsymbol{S}_{err}$ = ($6_{\mathbf{2}}$, 8_4, 10_{28}).

Frame Pattern with Separated Placement of Parity Blocks



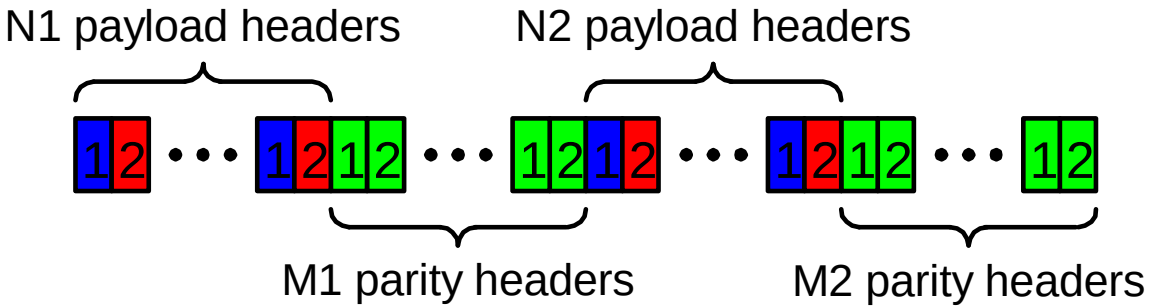
Sync header of payload block, either 01 or 10

Sync header of parity block, either 00 or 11

Total no. of payload blocks in one FEC codeword = N1 + N2.

Total no. of parity blocks in one FEC codeword = M1 + M2.

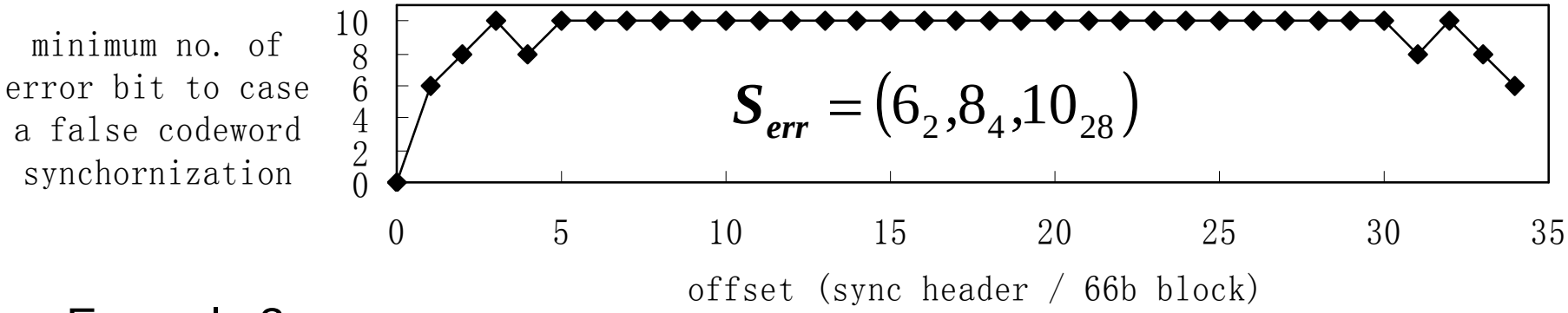
Assuming correct block alignment, we have



False Codeword Sync. with Separated Placement

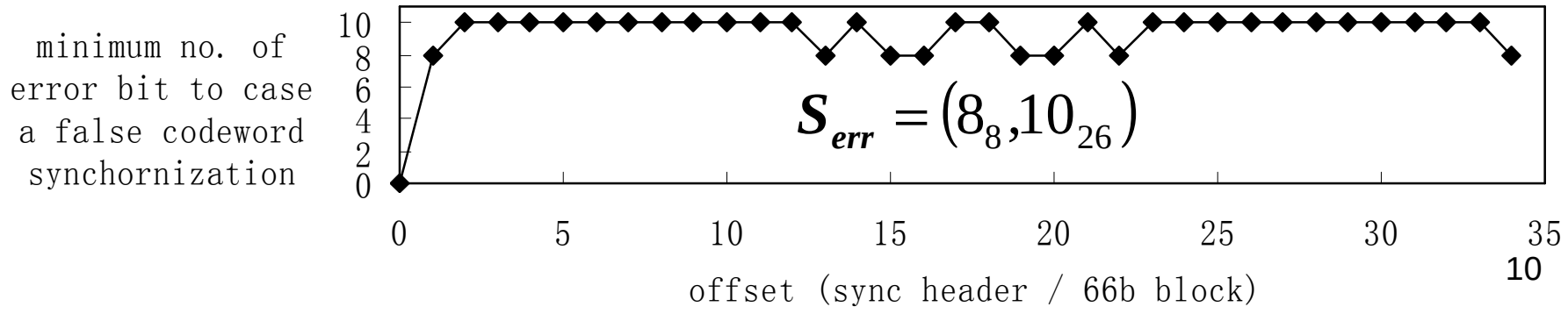
Example 2b (page 7):

Payload block N = 30; parity block M = 5; parity header pattern = {00, 11, 11, 11, 00}; and overhead = 14.10%.



Example 3a:

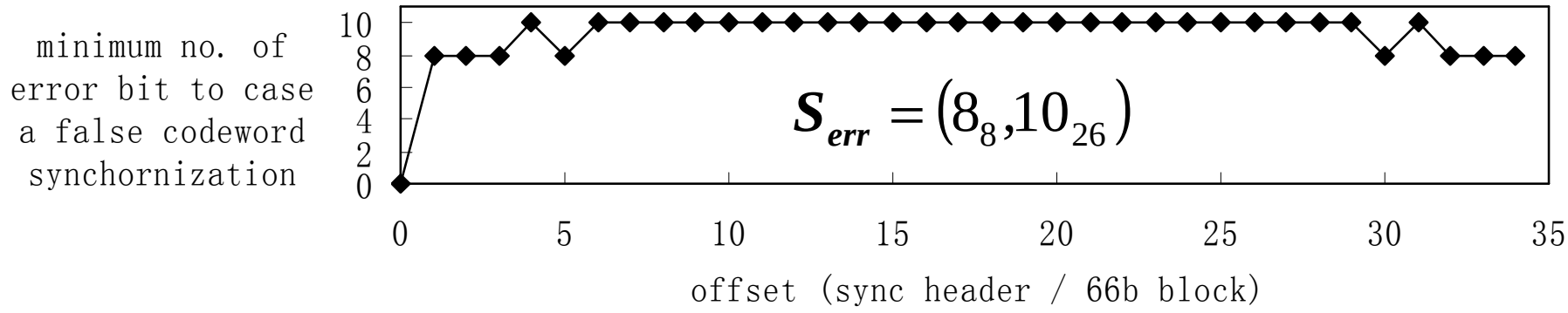
Payload block (N1, N2) = (12,18); parity block (M1, M2) = (3, 2); parity header pattern = { {00, 11, 11}, {11, 00} }; and overhead = 14.10%.



False Codeword Sync. with Separated Placement (cont.)

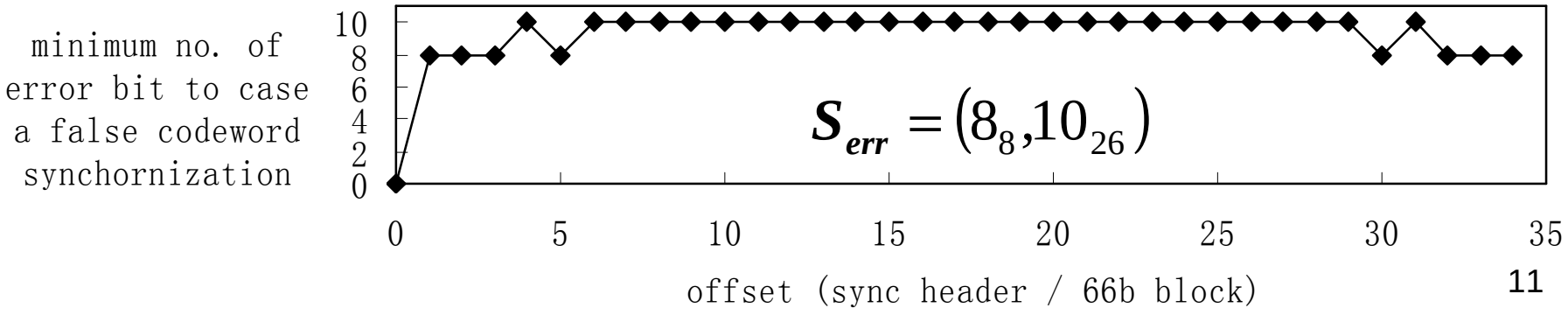
Example 3b:

Payload block (N1, N2) = (29, 1); parity block (M1, M2) = (2, 3); parity header pattern = { {00, 11}, {11, 11, 00} }; and overhead = 14.10%.



Example 3c:

Payload block (N1, N2) = (29,1); parity block (M1, M2) = (1, 4); parity header pattern = { {00}, {00, 11, 11, 00} }; and overhead = 14.10%.



Recommended Header Pattern for Parity Blocks

- Parity block M = 3:
  - –Parity header pattern = {00, 11, 11}.
- Parity block M = 4:
  - –Parity header pattern = {00, 11, 11, 00}.
- Parity block M >= 5:
  - –Besides a good sync headers' pattern, a proper placement of sync headers (page 9) in the FEC frame can further lower the false locking probability.

Conclusion

Separated placement of the parity blocks in a FEC frame has the following advantages:

- increase the minimum number of error bit to case a false codeword synchronization;
- no increase in complexity;
- no change of the current frame structure including line code, FEC, etc.

Thank You!

(Backup slides follow)

False Locking Probability

False locking probability based on the fast codeword algorithm (page 12 of 3av_0701_effenberger_1.pdf) is as follows,

$$\text{P\_false-lock} = \max\left\{2^{C_{block}\times K}, \text{BER}^{E_{bit}\times K}\right\}$$

number of 66-bit blocks in a FEC codeword

number of parity sync header error bits to case a false lock

$2^{C_{block} \times K}$ vs $\mathrm{BER}^{E_{bit} \times K}$

- Area
  - dominated by $\mathrm{BER}^{E_{bit} \times K}$
- Area
  - dominated by $2^{C_{block} \times K}$