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Burst-CDR performance under high BER

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Outline

1. Background
2. Possible issue
3. Modeling and estimation
4. Discussions
5. Conclusion

1. Background

(1) Tolerance to high BER condition is required on the receive side of PON interface.
(because of optical power budget)

(2) BER tolerance is required to achieve the best FEC gain.

(3) About delimiter and block framing, performances of synchronization already have been considered. (3av_0701_effenberger_1.pdf etc…)

(4) However, it was not discussed about the performance of PMA layer : Clock Data Recovery.

(5) Thus, we should consider about CDR, especially upstream.
(as issued by 3av_0703_takizawa_1.pdf)

2. Possible issue

(1) The questions are :

“ Can the Burst CDR lock-in under the condition of high BER ? ”,
“ Are there any penalties concerned with burst CDR ? “.

(2) The BER in this investigation is higher than 1.0E-4.

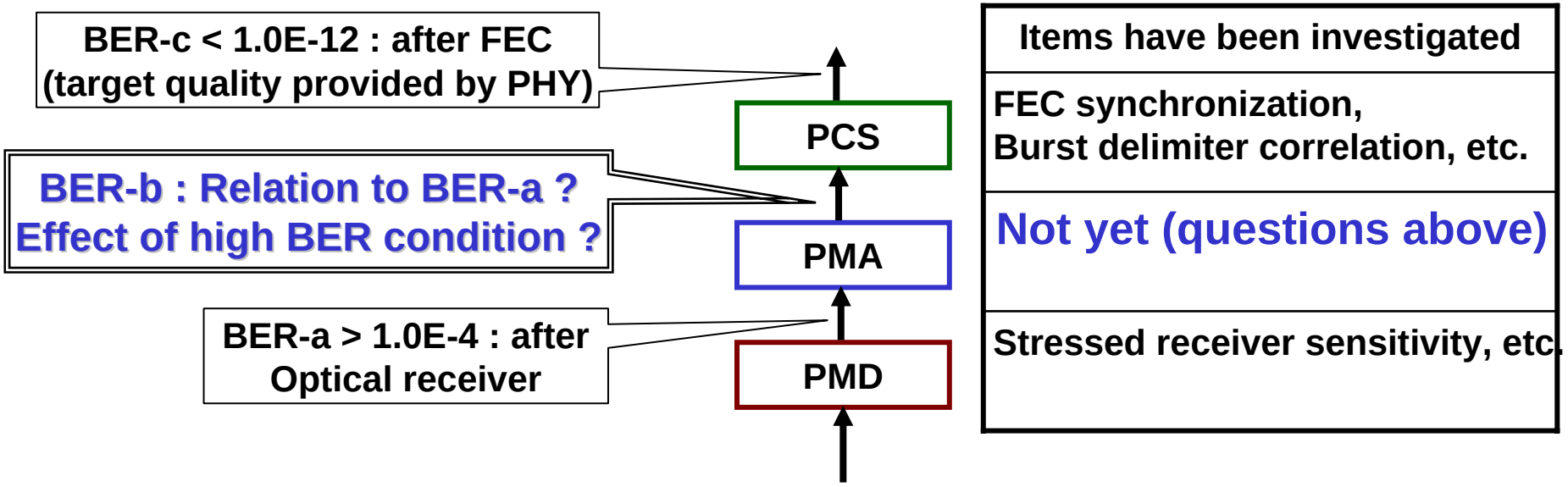

Figure1. Status of investigation about tolerance to stressed signal in each sub-layer of PHY

3. Modeling and estimation

(1) Modeling：Using burst-CDR for 1G-EPON (figure 2).

(2) Preconditions：

a. The stressed waveforms under an identical BER are the same for both 1G and 10G.

b. It is possible to use the architecture and circuit characteristics of 1G-CDR for 10G-CDR.

(3) Results of test：

a. The BER of burst CDR output was worse than one of OPT-Rx output. The penalty was about 1.4–1.7 times.

b. There was not a remarkable increase of penalty in high BER such as 1.0E-2.

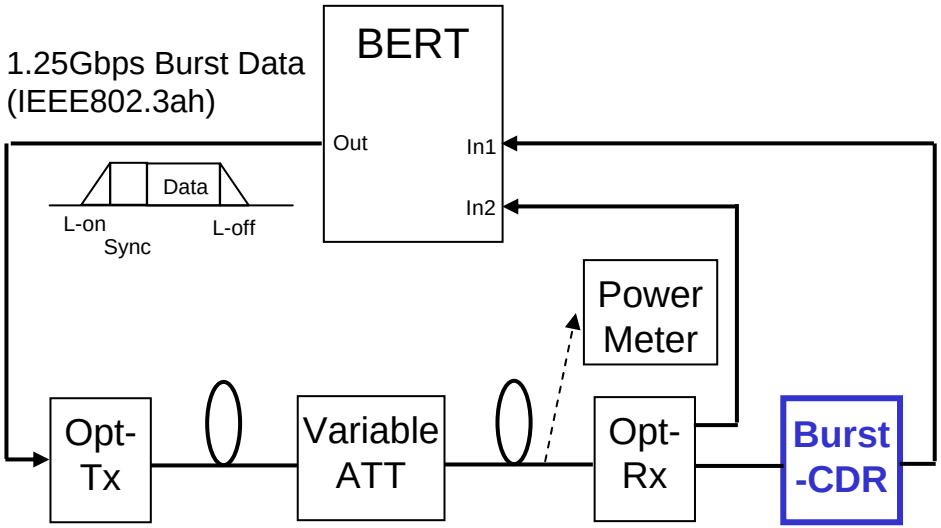

Figure2. Test set-up for the high BER tolerance

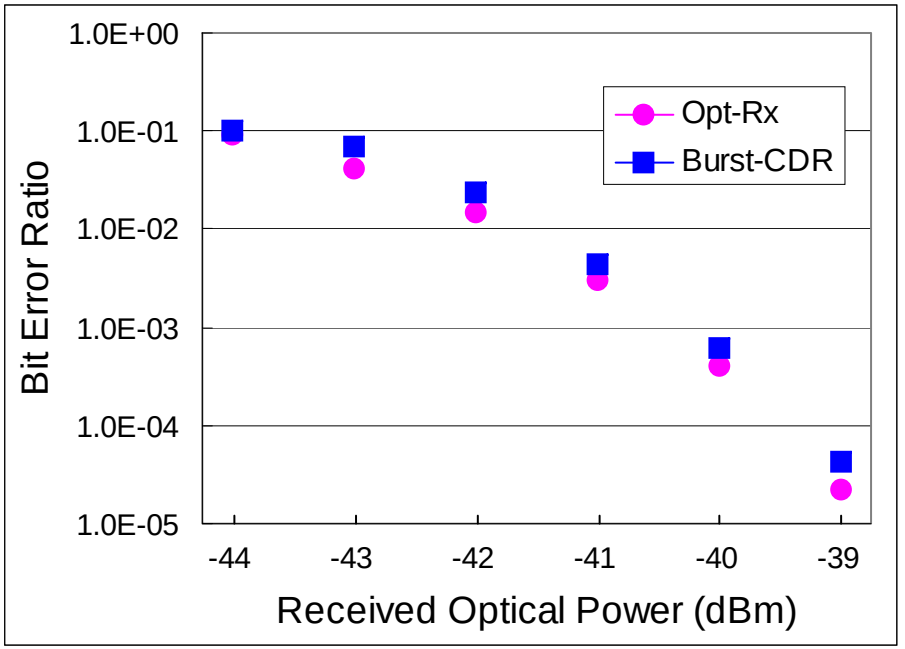

Figure3. BER characteristics of burst receiver (test results of 1G-EPON)

4. Discussions

(1) The burst CDR for 1GEPON can lock-in under the condition of high BER in accordance with the test results shown in the previous page.

(2) This supports the idea that 10G-CDR will also work under the high BER such as 1.0E-2.

(3) BER is worsen through the burst-CDR.

(4) The penalty depends on the sensitivity of bit decision in each CDR circuit. The value should be specified but it is under the investigation (for further study). The effect of CDR circuit should be concerned somewhere.

For instance, it is specified as 0.4dB additional margin for the stressed sensitivity in IEEE802.3 10GBASE-L receive characteristics (Note-e of table 52-13).

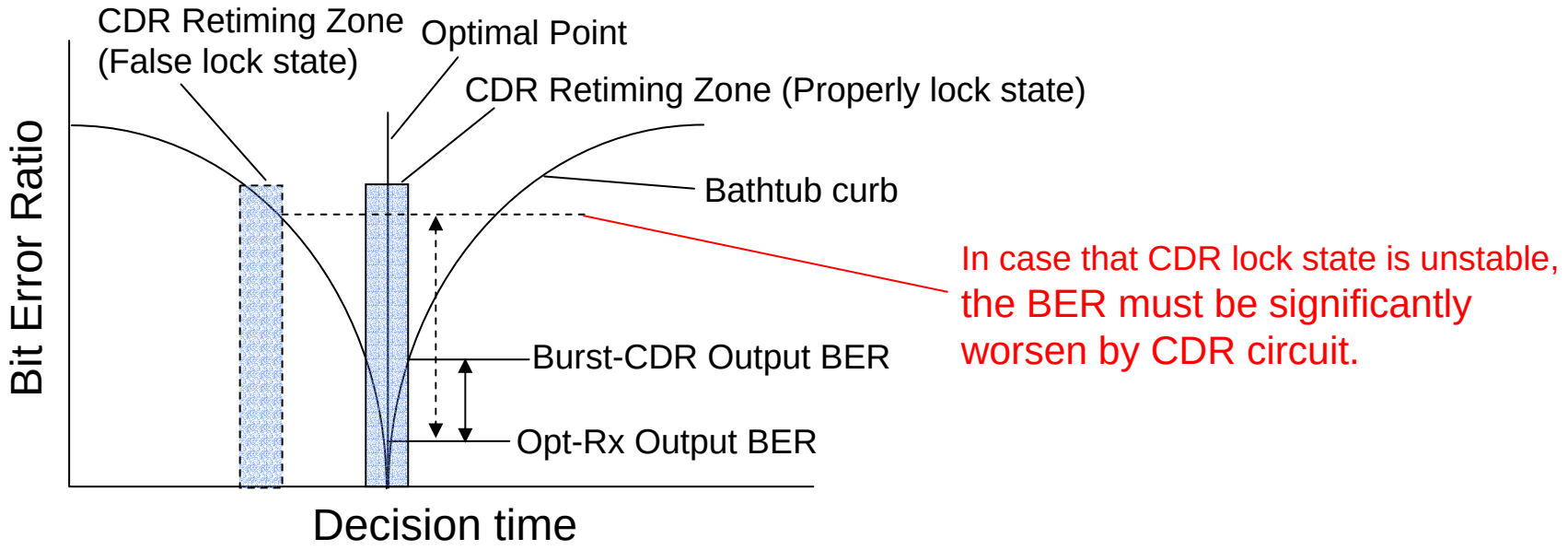

Figure4. Factors of degradation about bit decision characteristics in burst-CDR under a high BER. (analysis using the "Bathtub curb")

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5. Conclusion

(1) The test results of CDR for 1GEPON show that the CDR for 10GEPON can lock-in under the condition of high BER.

(2) BER is worsen through the burst-CDR.
The penalty should be specified somewhere.

(For instance, the effect is included as additional margin of stressed sensitivity in 10GBASE-L receive characteristics.)

The value is for further study.