Timing Considerations for 10GEPON Burst Receiver

IEEE 802.3av
November 2007
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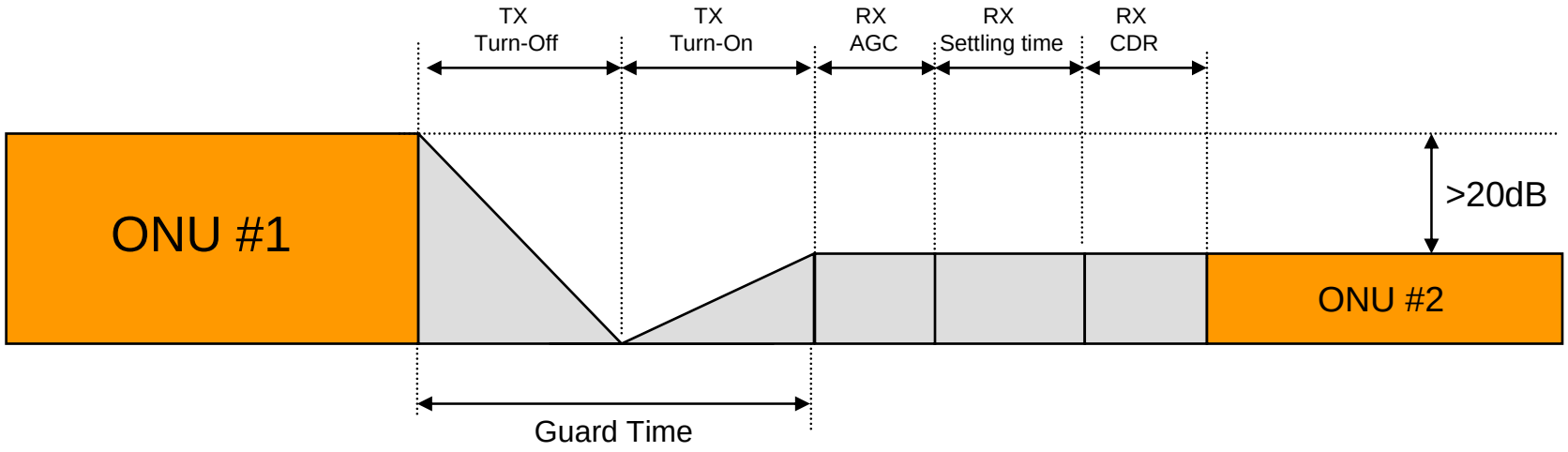
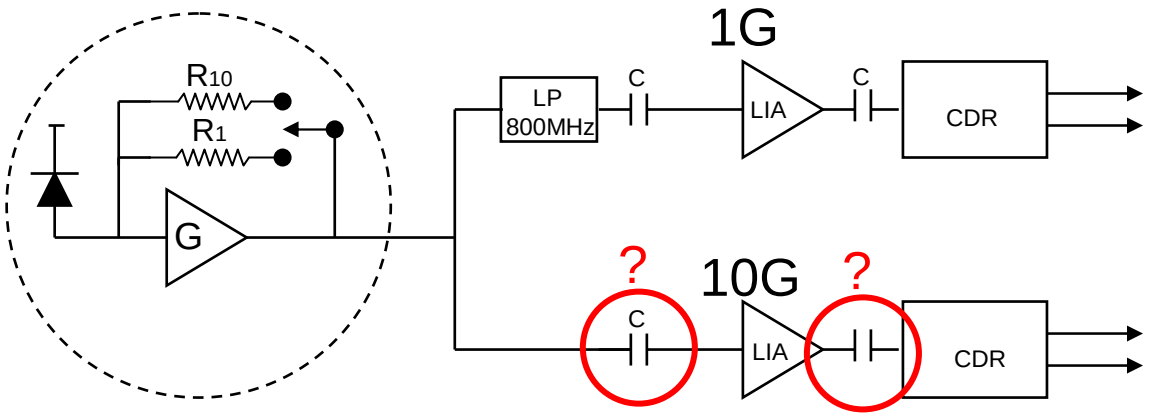
Outline

- Burst Mode Receiver Timing
- Settling Time
- AC DC coupling
- Summary

Burst Receiver Timing





Additional functions of Guard Time in mixed 10G/1G uplink

In a mixed 1G and 10G Uplink, the Guard time must enable the following functions that are not present on a 1G uplink:

- Adjusting the APD Adaptive Bias
- Adjusting the TIA gain to compensate for a change in data rate

Working with "Non-Optimized" APD

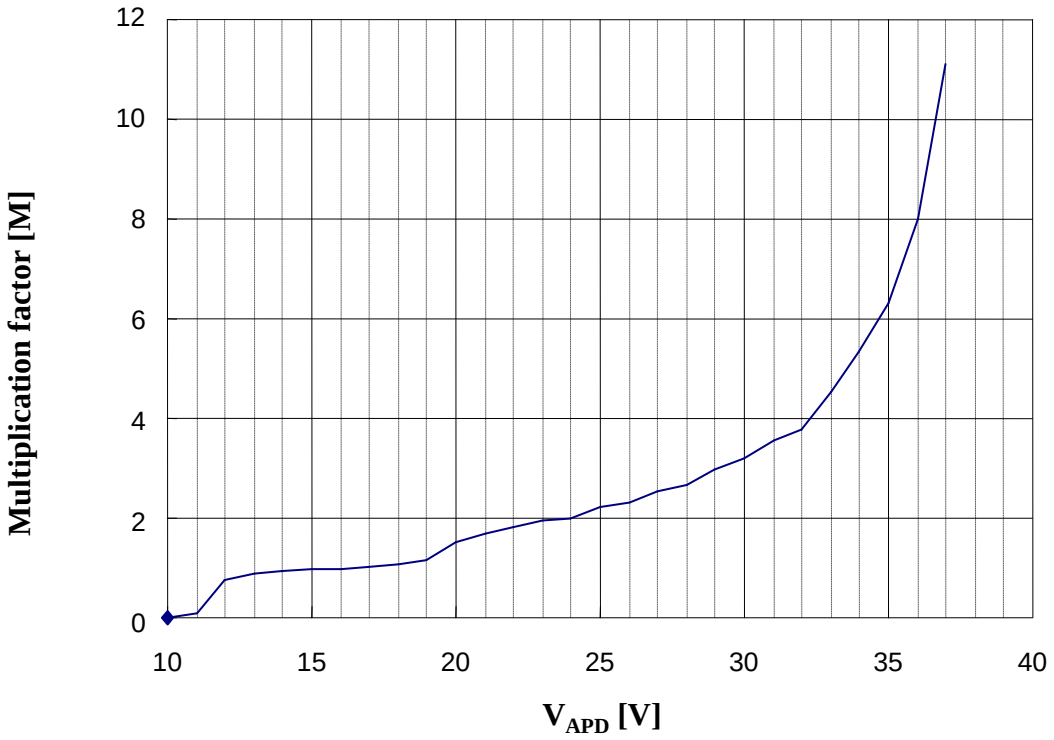
- Dual rate receiver has an optimized APD for 10G ***only***, this leads to performance degradation in GEPON
- APD gain varies as a function of the reverse bias
- Noise penalty

$$\frac{S/N(m)}{S/N(m_0)} = \frac{r^2(1+x/2)}{r^{2+x}+x/2}$$

Where:
m = non-optimum gain
m_0 = optimum gain
x ~ 0.5
$r = m/m_0$

- Non-optimized Gain could cause ***1dB*** Penalty and could be solved by ***Adaptive Bias***
- Adaptive Bias changing could be long time – µs

Multiplication Factor vs. APD Bias



TIA – Settling Time

- To support Dynamic Range, AGC Time constant should be much greater (~10x) than the worst-case CID
  - CID is 64bits (64/66)
  - AGC time constant should be 640bits → 64ns

- In transition to/from 1G and 10G, there is (assuming serial design) additional overhead needed for dynamically selecting the appropriate resistor : *roughly 10ns*

- Total TIA Settling Time: 64ns + 10ns = *74ns*

Burst Receiver – AC or DC Coupled?

AC

- AC coupling significantly simplifies the design of the Analog Front End
- Two major problems using conventional AC coupling
  - Guard Time and power variations between bursts can lead large DC offset
  - Long Threshold Acquisition time – Line Code dependent
- GEPON (8B/10B) allows using of short time constant AC coupled
- Capacitor coupling size is linearly to CID
- CID worse case grows to 128 from 64 due to FEC

DC

- DC coupled receiver quickly extracts the decision threshold
- Needs to deal with DC Cancellation mechanism

LIA Settling Time – AC Coupled

AC Coupled

- The coupling capacitor value is dominant in LIA Settling Time

$$C = \frac{7.8 * N * t_w}{R} = \frac{7.8 * 64 * 100\,ps}{50} = 1nF$$

$$\tau = R * C = 50 * 1nF = 50ns$$

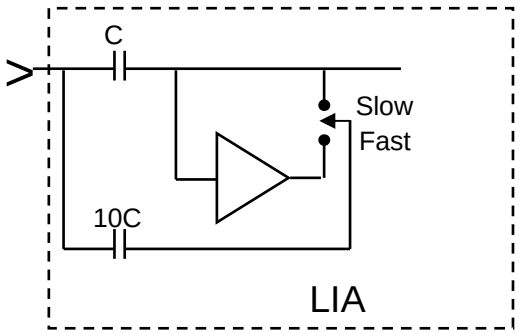
- At least 5τ to maintain Dynamic Range

$$50ns * 5 = 250ns$$

LIA Settling Time – DC Coupled

- ***DC Coupled***
  - Threshold Acquisition time could be short by adding “DC loop” inside the LIA
  - “DC loop” avoids 5τ “wait” for LIA stabilization
  - Settling Time can be reduced to 25ns

An example



CDR

- Typical CDRs (AC-coupled) are not suitable for burst traffic due to the inherent long lock time
- PLL Lock Time is about 25ns, regardless AC or DC coupled
- In AC Coupled
  - Time constant is long as the LIA

Summary

- Minimum values for guard time and sync time upper bound parameters were presented

- 1G-EPON should remain AC coupled

- Further study required to determine if 10GEPON should be AC or DC coupled

  - DC coupling is generally used in “Burst mode”-type applications
  - AC coupling ICs (TIA, LIA and CDR) are “off the shelf” components. DC ICs have a more complex design
  - AC coupling results in longer threshold acquisition times than DC

- APD Adaptive Bias should be considered