PCS Modes for PMD Testing: Pseudo-random test mode

Jeff Mandin
Valentin Ossman

PMC-Sierra

IEEE 802.3av
Atlanta
Nov 2007

Agenda

1. Overview of PCS test pattern modes
2. Description of basic 10G Pseudo-random Test Pattern mode
3. Adjustments to Pseudo-random Test Pattern mode for 10GEPON PCS
4. Straw Poll + motion

Background

1. Several *test pattern modes* are defined for 10GBASE-R:

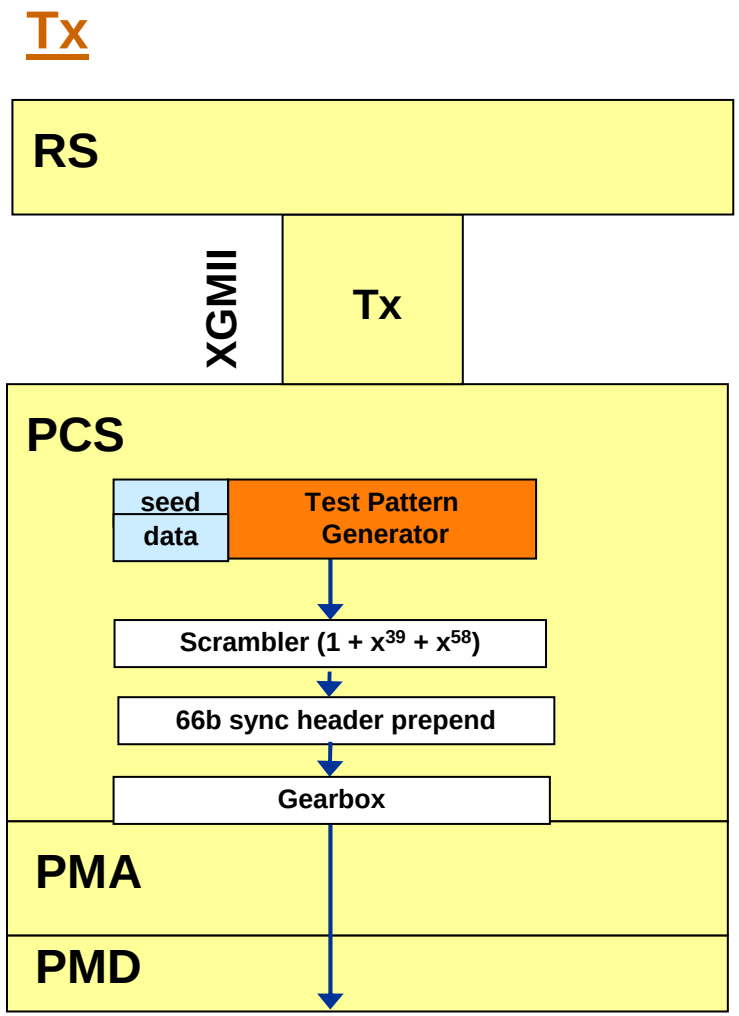
   a) **Pseudo-random test pattern**
   b) **Square-wave test pattern**
   c) **PRBS31 test pattern** (implementation in 10GBASE-R is *optional*)

2. These modes are also present in 802.3ap/an and are (broadly-speaking) desirable in 10GEPON as similar testing methodologies are applicable. However, 10GEPON FEC framing may necessitate some adjustments to their definition.

3. When test pattern mode has been activated (via MDIO), an ONU or OLT is required to generate or process a particular known data pattern instead of user data (typically in conjunction with some specialized test equipment).

   - This enables a uniform approach to conformance testing of the PMD layer

Pseudo-random Test Pattern Mode (Transmit Direction)

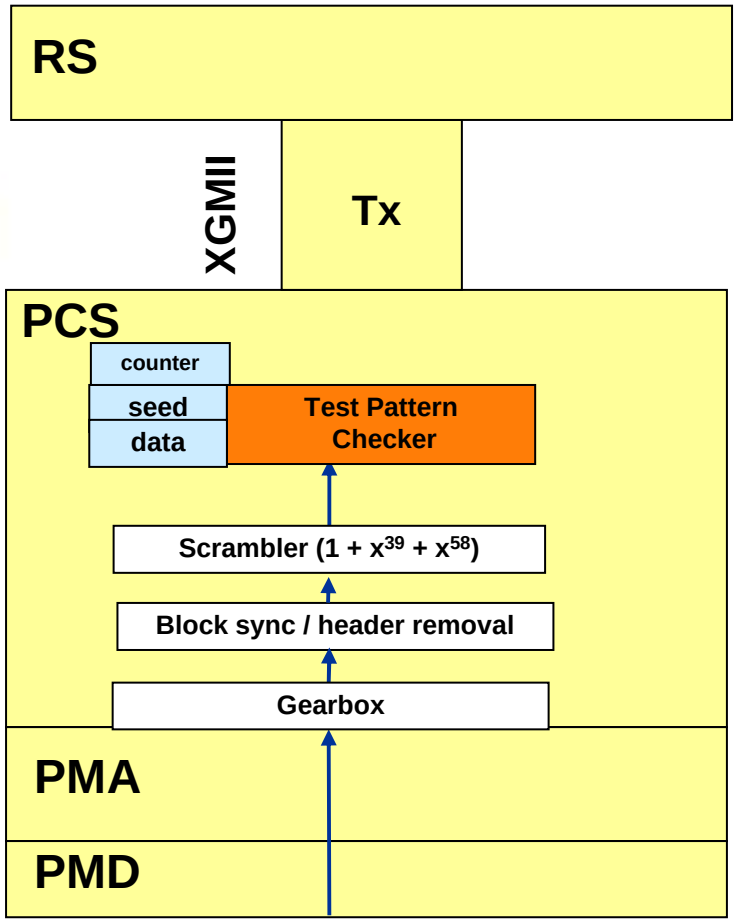


The test patterns are generated by utilizing the regular scrambler and framing mechanisms of 10G:

- Particular scrambler seeds are configured via MDIO
- The input data (either “all 0s” or “Local Fault” and configured via MDIO) is generated locally within the Tx PCS for the duration of Pseudo-random test pattern mode
- Scrambler output (ie. the pseudo-random pattern data) is carried in 66b blocks (with regular sync headers)

Pseudo-random Test Pattern Mode (Receive Direction)

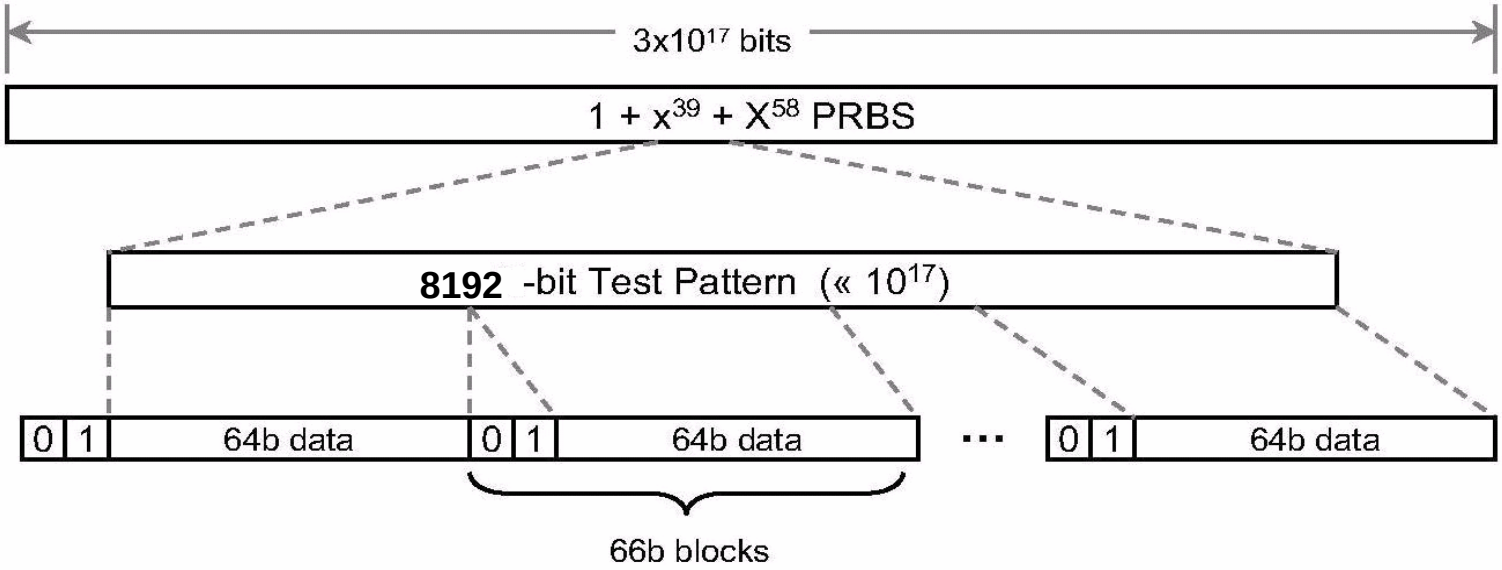
Rx



The test pattern data is received by the *Checker* function via the regular synchronization, framing, and scrambler mechanisms of Serial 10G:

- Scrambler seeds and data are configured via MDIO to match those of the transmitting equipment
- 66bit block alignment is obtained with the usual header-based state machine.
- The received descrambled data is compared to the result expected according to the configured seeds
- Counter records the number of erroneous data blocks and is typically read via MDIO by a test application

Pseudo-random test pattern – data stream



Special Data Patterns for PMD conformance testing

- Two fixed test patterns are defined (called *1* and *2* – *clause 52.9.1.1*) – each of the patterns uses 4 seeds in a sequence and is thus 33792 (== *4 * 8192*) bits long
  - *Pattern 1* is intended to simulate typical scrambled data
  - *Pattern 2* was selected to include bit sequences that are "stressful" to a receiver due to:
    a) Long Run-length
    b) Transition density
    c) Baseline wander

Setups for PMD conformance and related testing

Clause 52.9 defines PMD conformance tests which include pseudo-random test mode. The UNH PMD conformance tests are based on this clause. *Similar tests will be needed for 10GEPON*.

1. Transmitter tests
   - Device-under-test generates pseudo-random test pattern, which is measured by test equipment and evaluated for OMA, ER, other parameters

2. Stressed receiver test (52.9.9)
   - Intended to measure and verify BER performance of the analog receiver
   - Device-under-test receives *Pattern 2* after signal conditioning and imposition of sinusoidal jitter
   - Receiving PCS measures resulting BER by comparing the descrambled 66b blocks with the expected pattern (52.9.9.3)

Adjustments for 10GEPON: Parity blocks / burst mode

1. The 10GEPON pseudo-random test pattern should include FEC parity blocks (inserted by the FEC layer beneath the tx scrambler as with regular data)

   a) In the case where the ONU is the receiver, the ONU's PCS performs block synchronization using the regular 10GEPON sync state machine

   b) Though parity blocks arrive at the ONU or OLT receiver, while in test pattern mode the 66b blocks must (by default at least) not be corrected.
      - So that the test pattern checker can determine the raw BER as required in "stressed receiver"-type tests.

2. The pseudo-random test pattern received on the upstream by the OLT must begin with the 10GEPON burst preamble and 66b delimiter

   a) With existing test equipment, the preamble/delimiter can be generally be configured manually

How do Parity Blocks Impact the *Pattern* Characteristics?

a) *Pattern 1* is supposed to resemble “typical” data traffic. With parity blocks present, it resembles typical 10GEPON data traffic.

b) Impact on *Pattern 2* “stressful” characteristics should be minimal:

- Maximum run-length not affected due to presence of sync headers
- Extremes in running disparity would be affected only if parity blocks happened to have biased disparity in the direction opposite to the data.
  - Can verify after FEC selection

Some Possible Additional Features

1. We observed that typical PMD tests are interested in the uncorrected BER. But the BER of the FEC-corrected received data stream is useful also.

   - It seems simple and reasonable to provide a mode of pseudo-random test pattern mode operation which performs the FEC correction.

   - This would be configured through an MDIO register.

2. For flexibility, the ONU PCS should be configurable (by MDIO register) to transmit the burst preamble/delimiter at the beginning of the cyclic pseudo-random test pattern transmission.

Summary

1. Pseudo-random test pattern mode is useful for evaluation of 10GEPON PMD conformance

2. FEC parity should be included in the 10GEPON test pattern

3. 10GEPON Burst Preamble and delimiter must be prepended to the test pattern data when an OLT receiver is being tested.

Alternative approach: Skip FEC and burst mode

An alternative approach is adapt the pseudo-random test pattern generator of 10GBASE-R as it is:

1. While in test pattern mode:
    1. Skip transmitter insertion of FEC blocks
    2. Receiver does not expect FEC blocks or burst preamble
2. Simple, and uses the 10G test pattern sequences

1. Disadvantages:
    1. Separate non-10GEPON PCS synchronization state machine implementations are required in both OLT and ONU exclusively for support of test pattern mode
    2. Burst mode receiver at OLT is not properly tested

Straw Poll 1

1. 10GEPON should support pseudo-random test pattern mode with:

    a) Transmitter insertion of Parity blocks to the test pattern
    b) Requirement for prepending of 10GEPON burst preamble/delimiter at upstream receiver

    _____

2. 10GEPON should support pseudo-random test pattern mode as in 10GBASE-R and implement special sync state machines

    _____

3. Something Different _____

Straw Poll 2

10GEPON should support pseudo-random test pattern mode with the additional features (FEC-Corrected BER, Burst Preamble transmit) described on slide 11

Y ____

N ____

A ____